

82S115 4K-Bit TTL Bipolar PROM (512 × 8)

**Military
Bipolar Memory Products**

Product Specification

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the 3-State output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the bit drivers will be controlled solely by \overline{CE}_1 and \overline{CE}_2 lines.

In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the out-

put if the chip is enabled, and causes outputs to go to the Hi-Z State if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

FEATURES

- Address access time: 90ns max
- Input loading: -150 μ A max
- On-chip storage latches
- Schottky clamped
- Fully TTL compatible
- Outputs: 3-State

APPLICATIONS

- Microprogramming
- Hardware algorithms
- Character generation
- Control store
- Sequential controllers

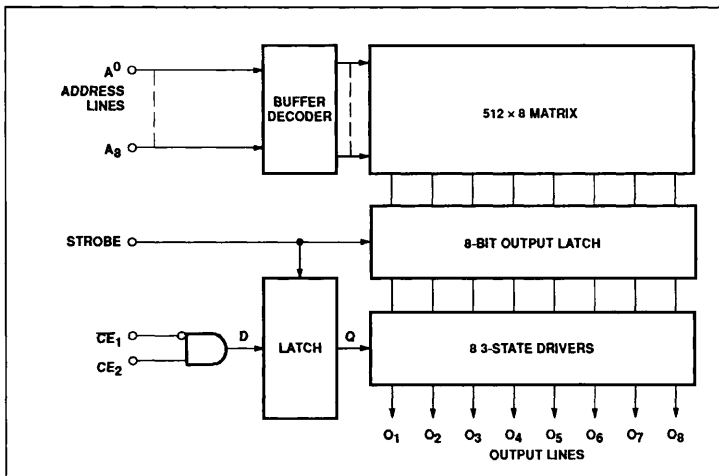
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual In-Line 600mil-wide	82S115/BJA
24-Pin Ceramic FlatPack	82S115/BYA

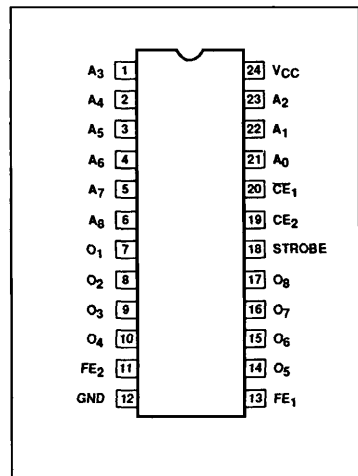
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I, V_O	Input voltage	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	$^{\circ}C$
T_{STG}	Storage temperature range	-65 to +150	$^{\circ}C$

BLOCK DIAGRAM



PIN CONFIGURATION



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DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS ⁵	LIMITS			UNIT
			Min	Typ ⁸	Max	
Input voltage						
V _{IL}	Low	V _{CC} = 4.5V, I _I = -18mA	2.0		0.8	V
V _{IH}	High				-0.8	V
V _{IK}	Clamp				-1.2	V
Output voltage						
V _{OL}	Low	CE ₁ = Low, CE ₂ = High I _O = 9.6mA	2.4	0.4	0.5	V
V _{OH}	High	V _{CC} = 4.5V, I _O = -2mA			V	
Input current⁵						
I _{IL}	Low	V _{CC} = 5.5V V _I = 0.45V			-150	μA
I _{IH}	High	V _I = 5.5V			50	μA
Output current⁵						
I _{OZ}	Hi-Z State	V _{CC} = 5.5V CE ₁ = High or CE ₂ = Low, V _O = 5.5V CE ₁ = High or CE ₂ = Low, V _O = 0.5V			100	μA
I _{OS}	Short circuit ¹	CE ₁ = Low, CE ₂ = High, V _O = 0V, High stored			-15	-85
Supply current						
CE ₁		CE ₁ = High, CE ₂ = Low V _{CC} = 5.5V		130	185	mA
CE ₂						
I _{CC}						
Capacitance⁹						
C _{IN}	Input	CE ₁ = High or CE ₂ = Low, V _{CC} = 5.0V V _I = 2.0V			5	pF
C _{OUT}	Output				V _O = 2.0V	8

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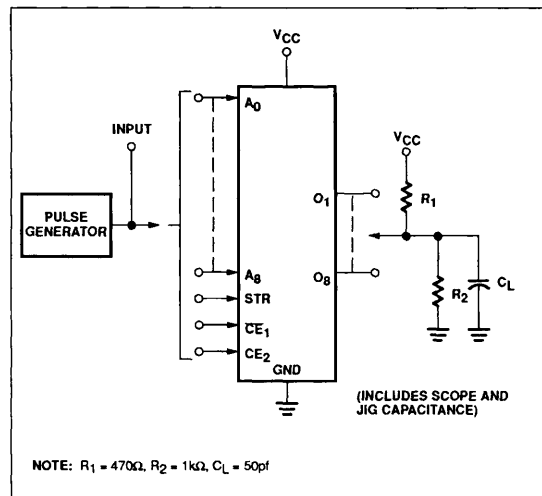
AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT	
					Min	Typ ⁸	Max		
t _{AA}	Access time ⁶	Output	Address	Latched or transparent		40		90	ns
t _{CE}						20		50	
t _{CD}	Disable time	Output	Chip disable	Latched or transparent		20		55	ns
t _{CDH}	Setup time	Output	Chip enable	Latched Read only ^{3,4}	50				
t _{CDL}									
t _{ADH}	Hold time	Address	Strobe	Latched Read only ^{3,4}	5	0			
t _{SW}	Strobe pulse width			Latched Read only ^{3,4}	40	15			ns
t _{SL}	Strobe latch time			Latched Read only ^{3,4}	90	35			ns
t _{DL}	Strobe delatch time			Latched Read only ^{3,4}			45		ns

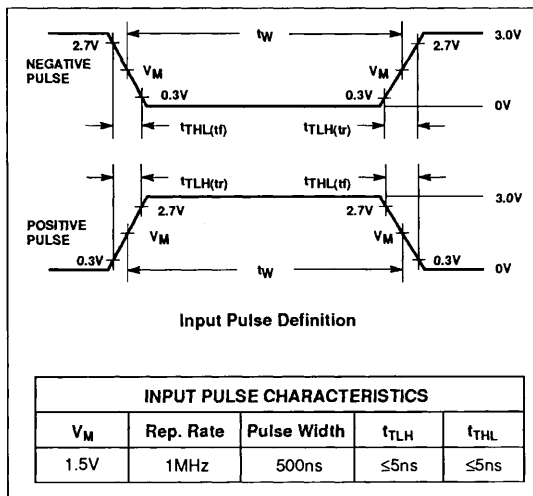
NOTES:

- No more than one output should be grounded at the same time and strobe should be disabled Strobe is in the High state.
- If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or High impedance state after it has been enabled.
- In latched Read Mode data from any selected address will be held on the output when Strobe is lowered only when Strobe is raised will new location data be transferred and chip enable conditions be stored. the new data will appear on the outputs if the chip enable conditions enable the outputs.
- During operation the fusing pins FE₁ and FE₂ may be grounded or left floating.
- Positive current is defined as into the terminal referenced.
- Tested at an address cycle time of 1μs.
- Areas shown by crosshatch are latched data from previous address.
- Typical values are at V_{CC} = 5V, T_A = 25°C.
- Guaranteed, but not tested.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



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TIMING DIAGRAMS

