Integrated Device Technology, Inc.

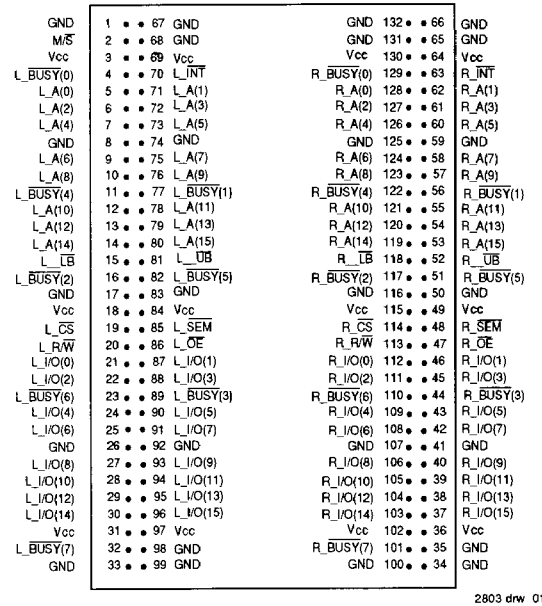
64K x 16
32K x 16
CMOS DUAL-PORT
STATIC RAM MODULE

PRELIMINARY
IDT7MB1006
IDT7MB1008

FEATURES

- High density 1M/512K CMOS dual-port static RAM module
- Fast access times: 25ns (max.)
- Fully asynchronous read/write operation from either port
- Easy to expand data bus width to 32 bits or more using the master/slave function
- Separate upper and lower byte control
- On-chip port arbitration logic
- $\overline{INT}$ flag for port-to-port communication and $\overline{BUSY}$ flag for maintaining data coherency
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted PQFP (plastic quad flatpack) components on a 132-pin FR-4 QIP (Quad In-line Package)
- Single 5V (±10%) power supply
- Input/outputs directly TTL compatible

PIN CONFIGURATION (1)



2803 drw 01

QIP
TOP VIEW

NOTES:
1. For the IDT7MB1008 (32K x 16) version, Pins 53 & 80 must be connected to GND for proper operation of the module.

DESCRIPTION:

The IDT7MB1006/1008 is a 64K x 16/32K x 16 high-speed CMOS dual-port static RAM module constructed on a multi-layer epoxy laminate (FR-4) substrate using eight IDT7025 (8K x 16) dual-port RAMs or depopulated using only four IDT7025 dual-port RAMs. The IDT7MB1006/1008 module is designed to be used as stand-alone dual-port RAM or as a combination master/slave dual-port RAM for 32-bit or wide word systems. Using the IDT master/slave approach in such system applications results in full-speed, error-free operation without the need for additional discrete logic.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{SEM}$ and $\overline{INT}$. $\overline{BUSY}$ flags are provided to maintain data coherency between ports.

The IDT7MB1006/1008 module is packaged on a FR-4 132-pin QIP (Quad In-line Package) with dimensions of only 3.51" x 1.61" x 0.31". Maximum access times as fast as 25ns are available over the commercial temperature range.

All inputs and outputs of the IDT7MB1006/1008 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

PIN NAMES

Left Port	Right Port	Description
L_A (0–15)	R_A (0–15)	Address Inputs
L_I/O (0–15)	R_I/O (0–15)	Data Inputs/Outputs
L_R/$\overline{W}$	R_R/$\overline{W}$	Read/Write Enables
L_$\overline{CS}$	R_$\overline{CS}$	Chip Select
L_$\overline{OE}$	R_$\overline{OE}$	Output Enable
L_$\overline{BUSY}$ (0–7)	R_$\overline{BUSY}$ (0–7)	Busy Flags
L_$\overline{INT}$	R_$\overline{INT}$	Interrupt Flag
L_$\overline{SEM}$	R_$\overline{SEM}$	Semaphore Control
M/$\overline{S}$		Master/Slave Control
Vcc		Power
GND		Ground

2803 tbl 01

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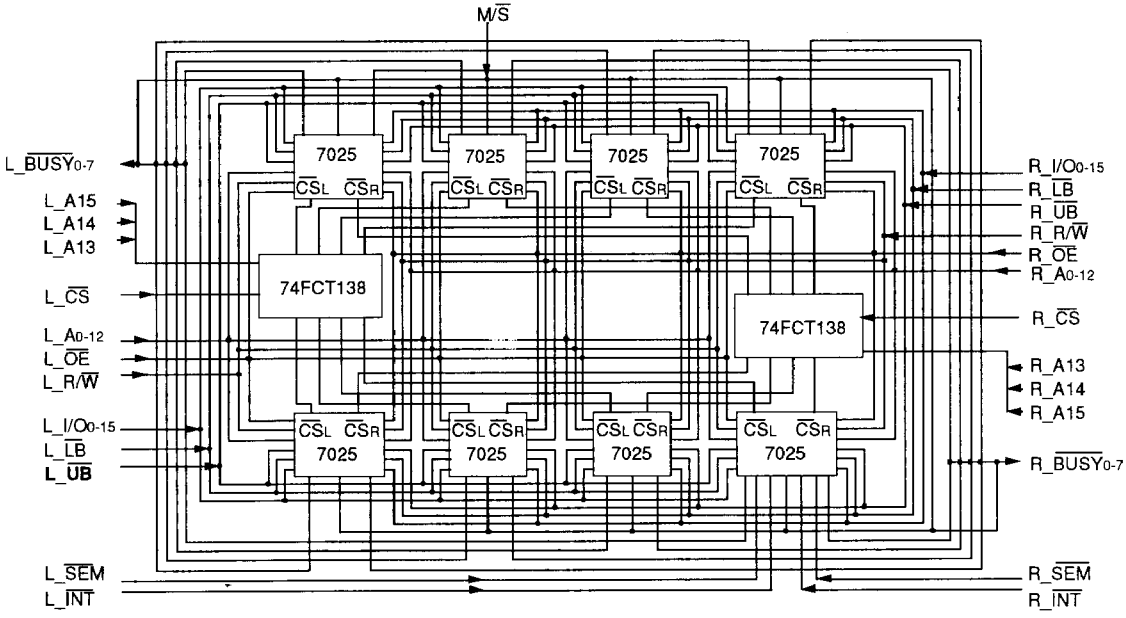
1-8-1

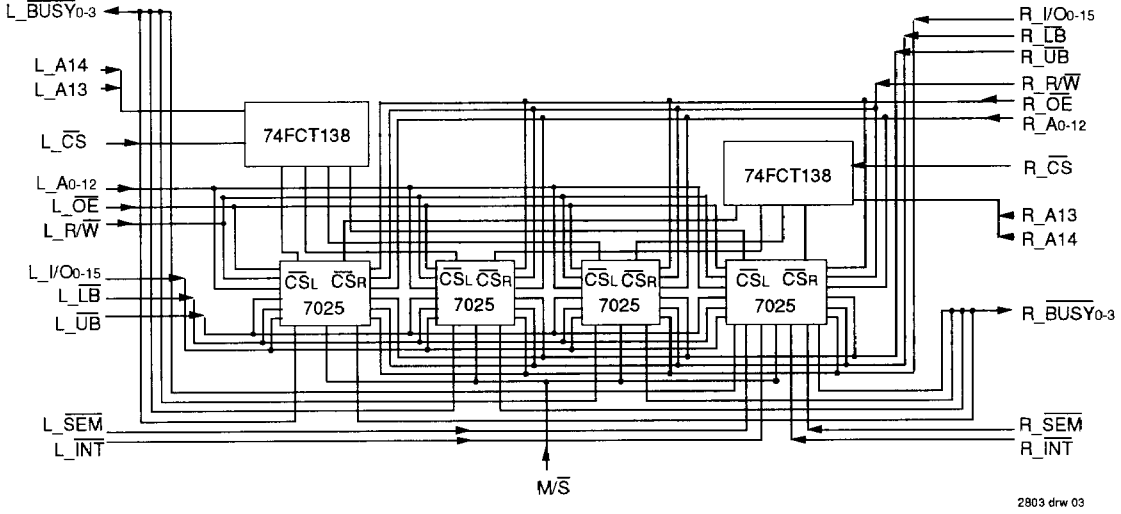
FUNCTIONAL BLOCK DIAGRAM

7MB1006



2803 drw 02

7MB1008



2803 drw 03

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7-5-2

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to + 70°C	0V	5.0V± 10%

2803 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	-	6.0	V
VIL	Input Low Voltage	-0.5(1)	-	0.8	V

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.

2803 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE:

2803 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	7MB1006/8 Max.	Unit
CIN1	Input Capacitance ($\overline{CS}$, $\overline{BUSY}$, $\overline{SEM}$, $\overline{INT}$)	VIN = 0V	15/15	pF
CIN2	Input Capacitance (Data, Address, All Other Controls)	VIN = 0V	100/60	pF
COUT	Output Capacitance (Data)	VOUT = 0V	100/ 60	pF

NOTE:

2803 tbl 05

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(Vcc=5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1006 Min.	IDT7MB1006 Max.	IDT7MB1008 Min.	IDT7MB1008 Max.	Unit
ICC2	Dynamic Operating Current (Both Ports Active)	Vcc = Max., $\overline{CS}$ ≤ VIL, $\overline{SEM}$ ≥ VIH Outputs Open, f = fMAX	—	960	—	680	mA
ICC1	Dynamic Operating Current (One Port Active)	Vcc = Max., L_$\overline{CS}$ or R_$\overline{CS}$ ≥ VIH, Outputs Open, f = fMAX	—	760	—	480	mA
ISB1	Standby Supply Current (TTL Levels)	Vcc = Max., L_$\overline{CS}$ and R_$\overline{CS}$ ≥ VIH Outputs Open, f = fMAX L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ Vcc - 0.2V	—	565	—	285	mA
ISB2	Full Standby Supply Current (CMOS Levels)	L_$\overline{CS}$ and R_$\overline{CS}$ ≥ Vcc - 0.2V VIN > Vcc - 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ Vcc - 0.2V	—	125	—	65	mA

2803 tbl 06

7-8-3

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MB1006 Min.	IDT7MB1006 Max.	IDT7MB1008 Min.	IDT7MB1008 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address & Other Controls)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	80	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data,$\overline{CS}$,$\overline{BUSY}$,$\overline{SEM}$,$\overline{INT}$)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	80	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	2.4	—	V

2803 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2803 tbl 08

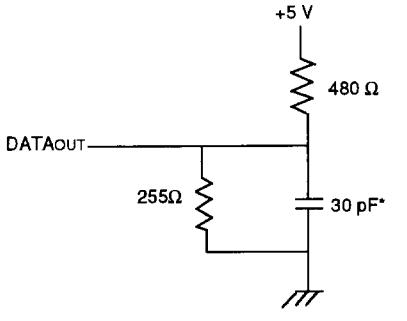

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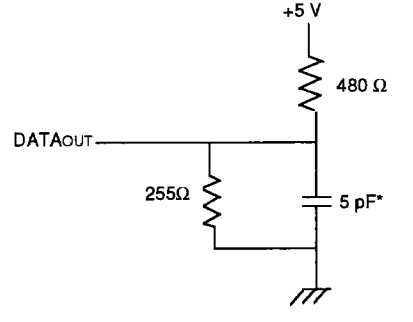
Figure 1. Output Load



2803 drw 05

Figure 2. Output Load
(for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

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7-8-4

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MB1006SxxK or 7MB1008SxxK								
		-25[5]		-30[5]		-35		-40		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	40	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	—	35	—	40	ns
t_{OE}	Output Enable Access Time	—	13	—	15	—	20	—	25	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	3	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	3	—	3	—	3	—	3	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	12	—	12	—	15	—	15	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	ns
t_{CW}[2]	Chip Select to End of Write	20	—	25	—	30	—	35	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	35	—	ns
t_{AS1}[3]	Address Set-up to Write Pulse Time	5	—	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}[4]	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	ns
t_{DH}[4]	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{WHZ}[1]	Write Disable to Output in High Z	—	18	—	20	—	20	—	20	ns
t_{OW}[1, 4]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	13	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	13	—	15	—	15	—	ns

2803 tbl 09

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1}= 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.
5. Preliminary specifications only.

7-8-5

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MB1006SxxK or 7MB1008SxxK						Unit
		-50		-65		-80		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	50	—	65	—	80	—	ns
t_{AA}	Address Access Time	—	50	—	65	—	80	ns
t_{ACS}(2)	Chip Select Access Time	—	50	—	65	—	80	ns
t_{OE}	Output Enable Access Time	—	30	—	35	—	40	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	25	—	30	—	35	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	3	—	3	—	3	—	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Disable to Power Down Time	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	20	—	20	—	ns
t_{WC}	Write Cycle Time	50	—	65	—	80	—	ns
t_{CW}(2)	Chip Select to End of Write	40	—	50	—	55	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	55	—	ns
t_{AS1}(3)	Address Set-up to Write Pulse Time	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	ns
t_{WR}(4)	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	35	—	40	—	45	—	ns
t_{DH}(4)	Data Hold Time	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	25	—	30	—	35	ns
t_{WHZ}[1]	Write Disable to Output in High Z	—	25	—	30	—	35	ns
t_{OW}(1, 4)	Output Active from End of Write	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	15	—	15	—	15	—	ns

2803 tbl 10

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1} = 0 if R/$\overline{W}$ is asserted low simultaneously with or after the $\overline{CS}$ low transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.

7

7-8-6

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	-25[11]		-30[11]		-35		-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ Cycle - MASTER MODE[3]										
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	25	—	30	—	35	—	40	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	25	—	30	—	35	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	20	—	25	—	30	—	35	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	20	—	25	—	30	—	30	ns
t_{APS}[6]	Arbitration Priority Set-up Time	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	Note 9	—	Note 9	—	Note 9	—	Note 9	ns
$\overline{BUSY}$ Cycle - Slave Mode[4]										
t_{WB}[7]	Write to $\overline{BUSY}$ Input	0	—	0	—	0	—	0	—	ns
t_{WH}[8]	Write Hold After $\overline{BUSY}$	15	—	20	—	25	—	25	—	ns
Port-to-Port Delay Timing										
t_{WDD}[5]	Write Pulse to Data Delay	—	50	—	55	—	60	—	65	ns
t_{DDD}[5]	Write Data Valid to Read Data Valid	—	35	—	40	—	45	—	50	ns
Interrupt Timing										
t_{AS}[10]	Address Set-up Time	5	—	5	—	5	—	5	—	ns
t_{WR}[10]	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	20	—	25	—	30	—	35	ns
t_{INR}	Interrupt Reset Time	—	20	—	25	—	30	—	35	ns

2803 tbl 11

NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual), or t_{DDD} - t_{WP} (actual).
10. If $\overline{CS}$ is used to control interrupt, then t_{AS}=0 and t_{WR}= 5ns.
11. Preliminary specifications only.

7-8-7

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	-50		-65		-80		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ Cycle - MASTER MODE[3]								
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	50	—	55	—	55	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	45	—	45	—	45	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	45	—	50	—	55	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Select	—	40	—	45	—	45	ns
t_{APS}[6]	Arbitration Priority Set-up Time	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	Note 9	—	Note 9	—	Note 9	ns
$\overline{BUSY}$ Cycle - Slave Mode[4]								
t_{WB}[7]	Write to $\overline{BUSY}$ Input	0	—	0	—	0	—	ns
t_{WH}[8]	Write Hold After $\overline{BUSY}$	25	—	30	—	30	—	ns
Port-to-Port Delay Timing								
t_{WDD}[5]	Write Pulse to Data Delay	—	70	—	85	—	95	ns
t_{DDD}[5]	Write Data Valid to Read Data Valid	—	55	—	70	—	80	ns
Interrupt Timing								
t_{AS}[10]	Address Set-up Time	5	—	5	—	5	—	ns
t_{WR}[10]	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	45	—	45	—	55	ns
t_{INR}	Interrupt Reset Time	—	45	—	45	—	55	ns

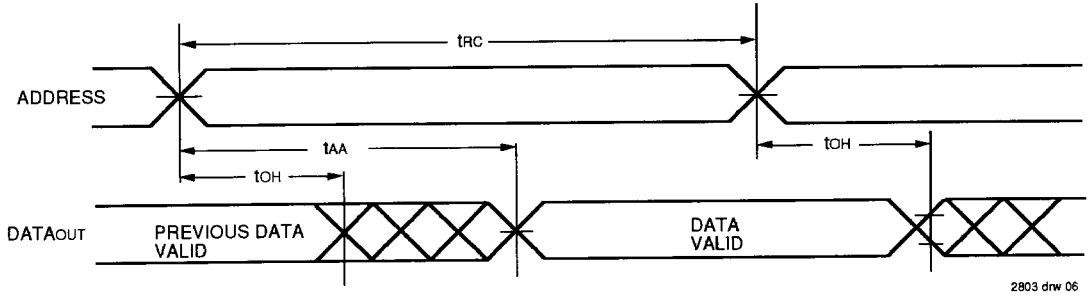
NOTES:

2803 tbl 12

1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \geq V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \leq V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. t_{BDD} is a calculated parameter and is the greater of 0, t_{WDD} - t_{WP} (actual), or t_{DDD} - t_{WP} (actual).
10. If $\overline{CS}$ is used to control interrupt, then t_{AS}=0 and t_{WR}= 5ns.

7

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)[1,2,4]



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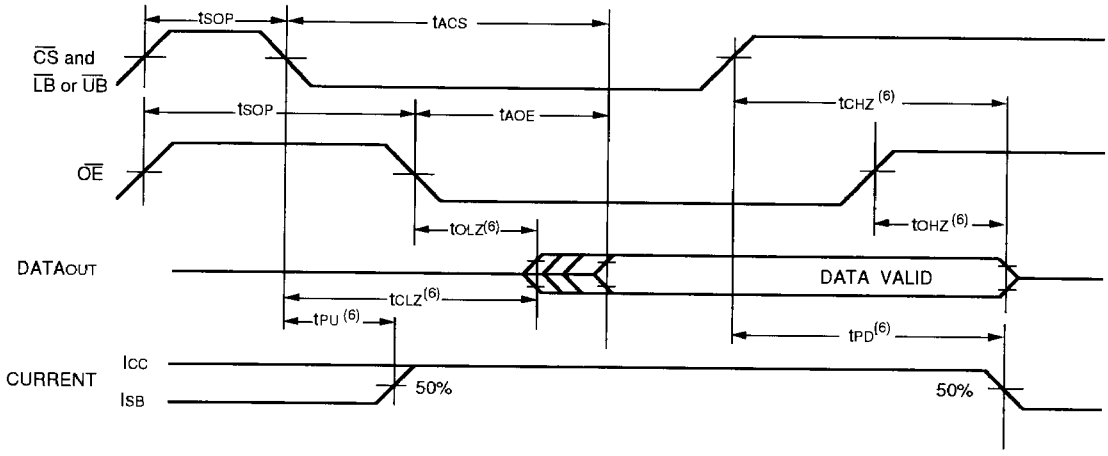
7-8-8

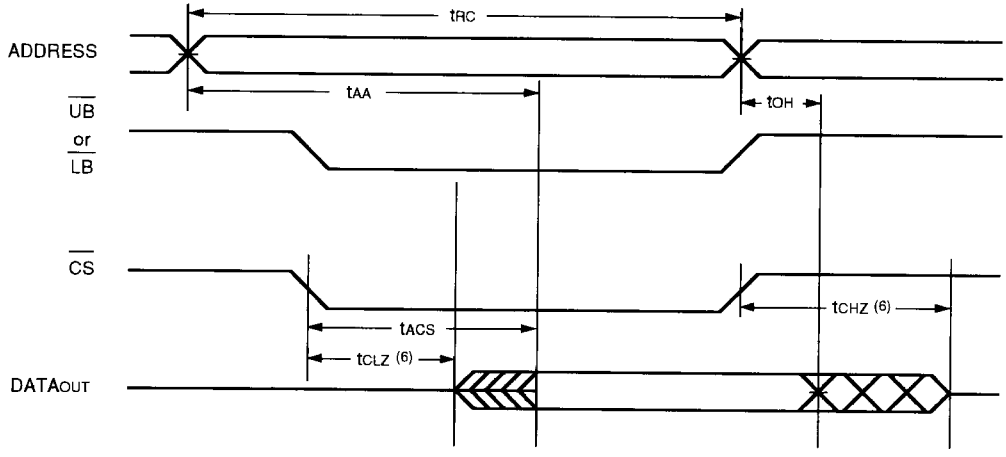
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)(1,3,5)



2803 drw 07

NOTES:
1. R/W is High for Read Cycles
2. Device is continuously enabled. CS = Low. UB or LB = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with CS transition low.
4. OE = Low.
5. To access RAM, CS = Low, UB or LB = Low, SEM = H. To access semaphore, CS = H and SEM = Low.
6. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 3 (UB OR LB CONTROLLED TIMING)(1,3,4,5)

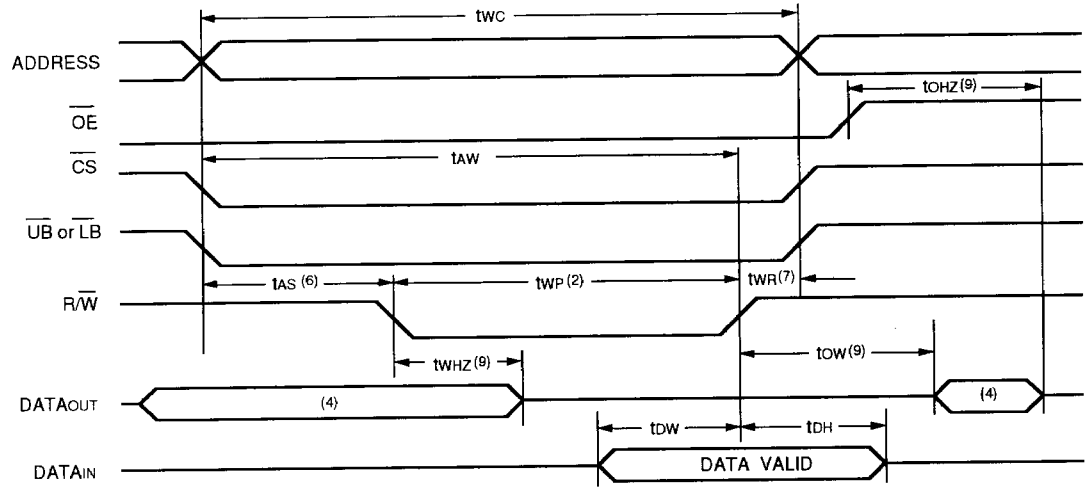


2803 drw 08

NOTES:
1. R/W is High for Read Cycles
2. Device is continuously enabled. CS = Low. UB or LB = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with CS transition low.
4. OE = Low.
5. To access RAM, CS = Low UB or LB = Low, SEM = H. To access semaphore, CS = H and SEM = Low.
6. This parameter is guaranteed by design but not tested.

7-8-9

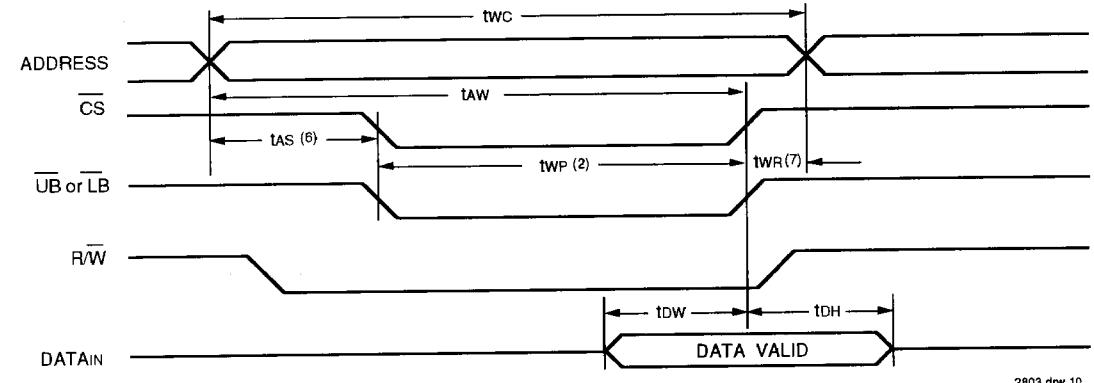
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,3,5,8)



2803 drw 09

NOTES:
1. R/$\overline{W}$ is High for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = Low. $\overline{UB}$ or $\overline{LB}$ = Low. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = Low.
5. To access RAM, $\overline{CS}$ = Low, $\overline{UB}$ or $\overline{LB}$ = Low, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = H and $\overline{SEM}$ = Low.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING)(1,3,5,8)

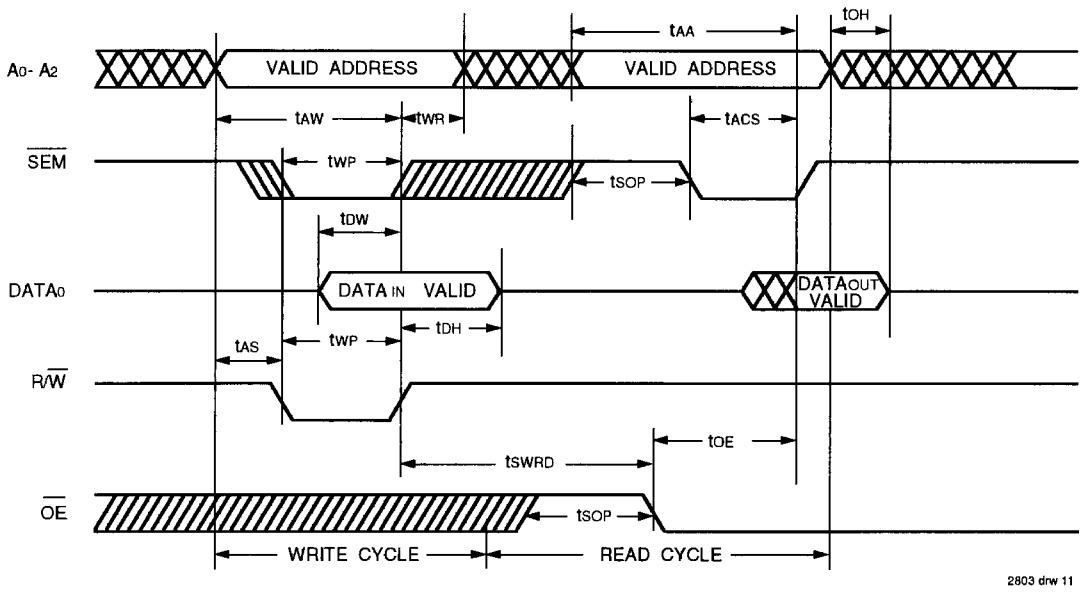


2803 drw 10

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a Low $\overline{UB}$ or $\overline{LB}$ and a Low $\overline{CS}$ and a Low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. This parameter is guaranteed by design but not tested.

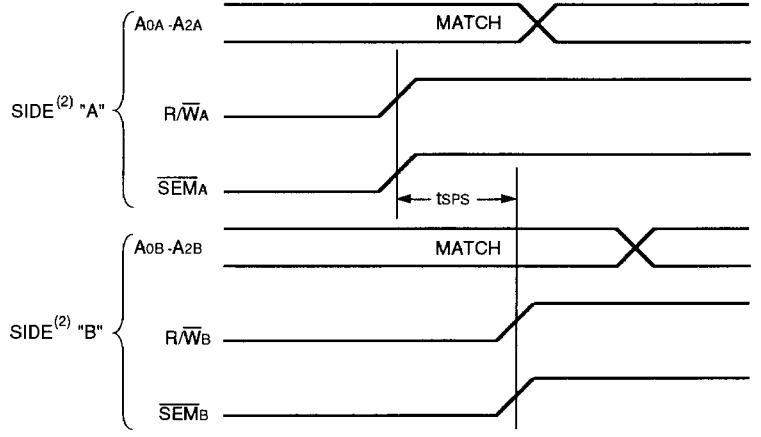
7-8-10

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)[1]



NOTE:
1. $\overline{CS}$ = High for the duration of the above timing (both write and read cycle).

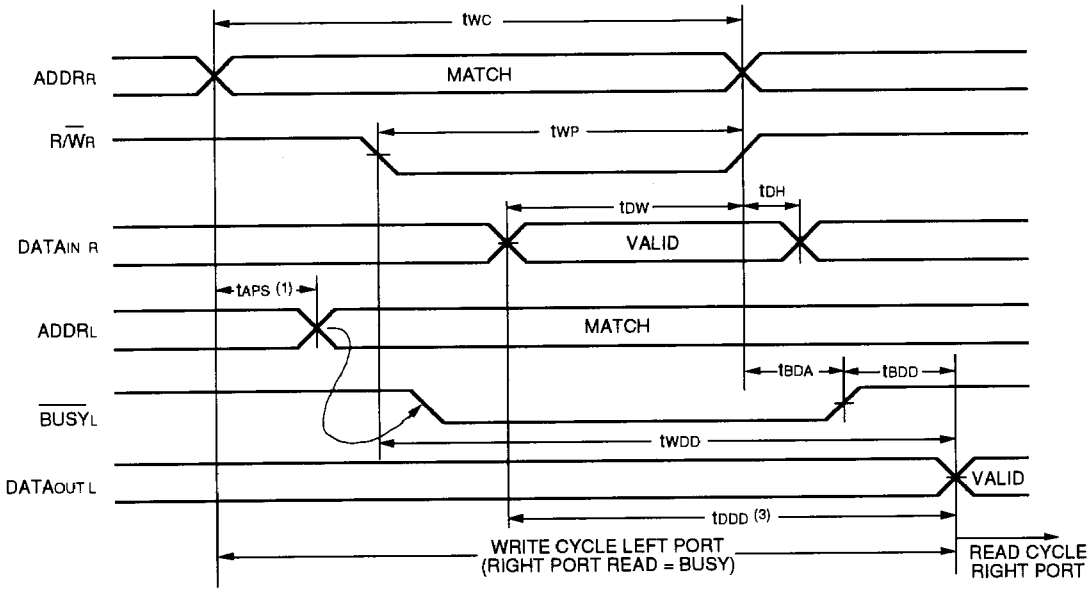
TIMING WAVEFORM OF SEMAPHORE CONTENTION[1,3,4]



NOTES:
1. D_{0R} = D_{0L} = Low, L_$\overline{CS}$ = R_$\overline{CS}$ = High. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going High to R/$\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

1-8-11

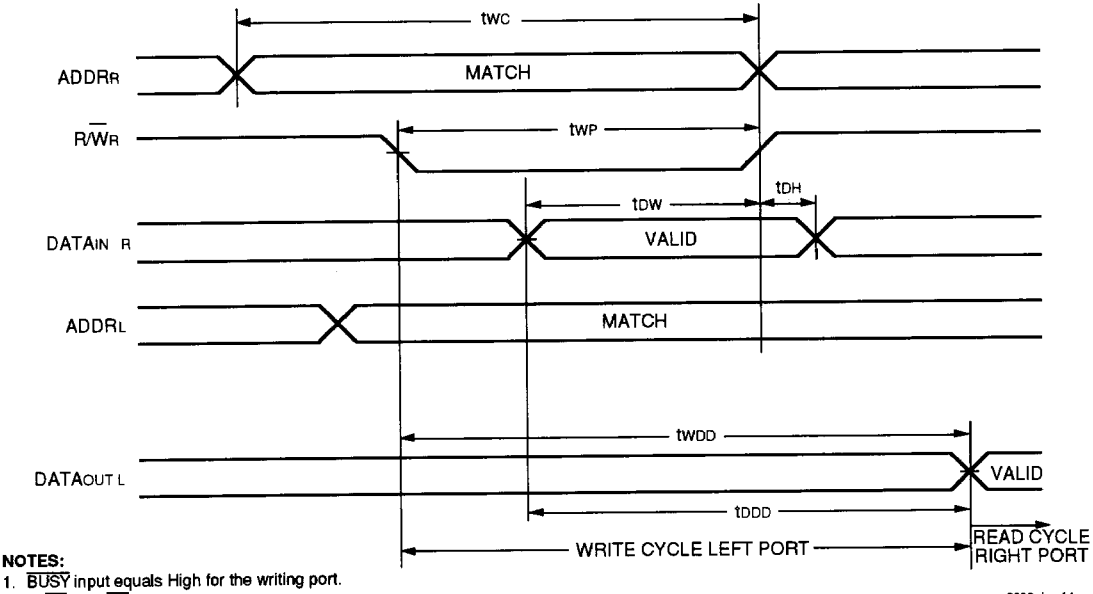
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (M/$\overline{S}$ ≥ VIH)(2)



NOTES:
1. To ensure that the earlier of the two ports wins.
2. L_$\overline{CS}$ = R_$\overline{CS}$ = Low
3. $\overline{OE}$ = Low for the reading port.

2803 drw 13

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY (M/$\overline{S}$ ≤ VIL)(1,2)



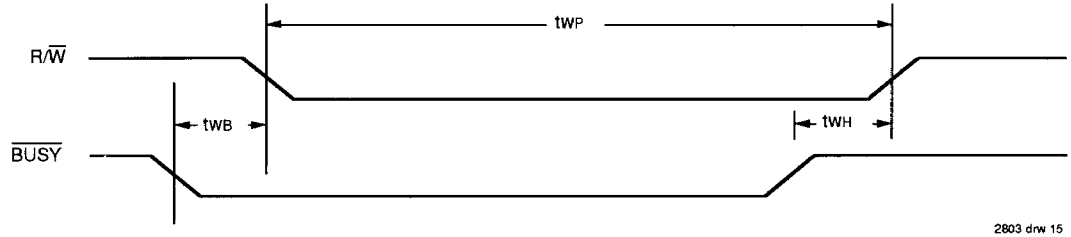
NOTES:
1. $\overline{BUSY}$ input equals High for the writing port.
2. L_$\overline{CS}$ = R_$\overline{CS}$ = Low

2803 drw 14

7

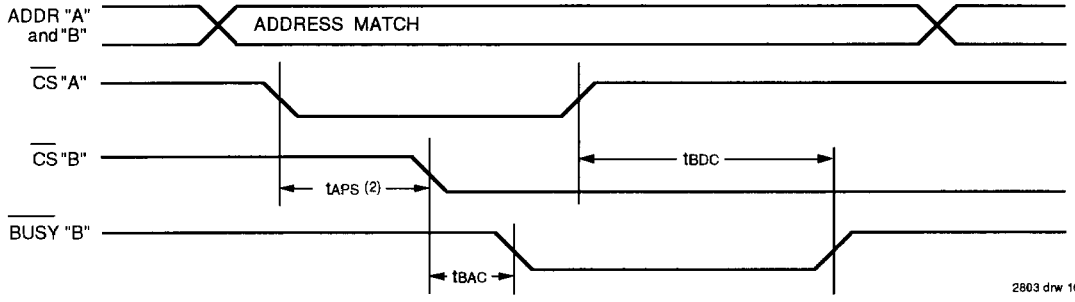
7-8-12

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (M/$\overline{S}$ ≤ VIL)



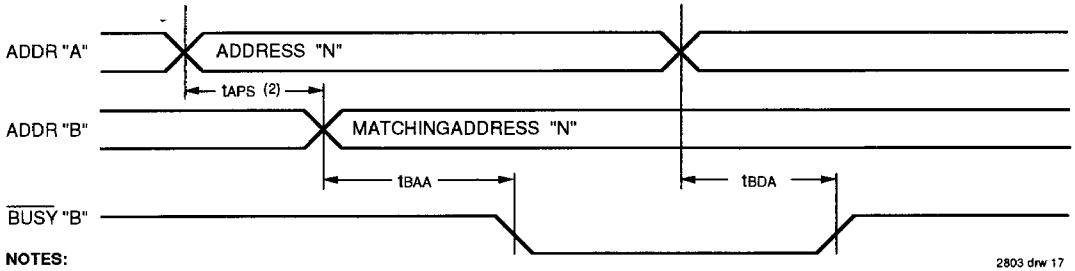
2803 drw 15

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CS}$ TIMING(1)



2803 drw 16

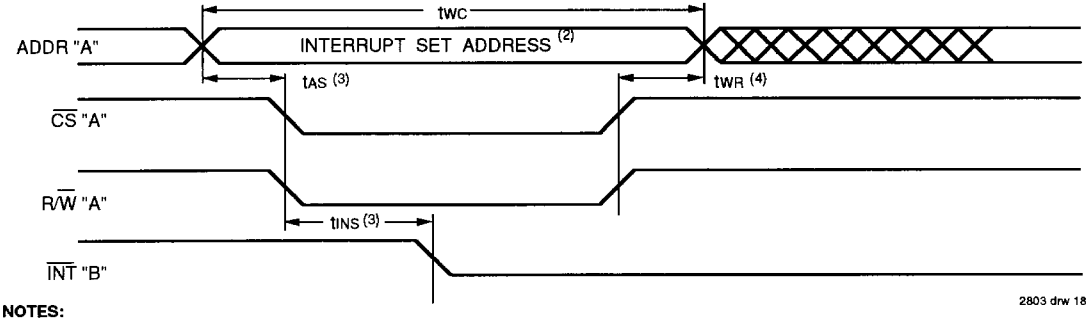
WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)



2803 drw 17

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

WAVEFORM OF INTERRUPT TIMING(1)

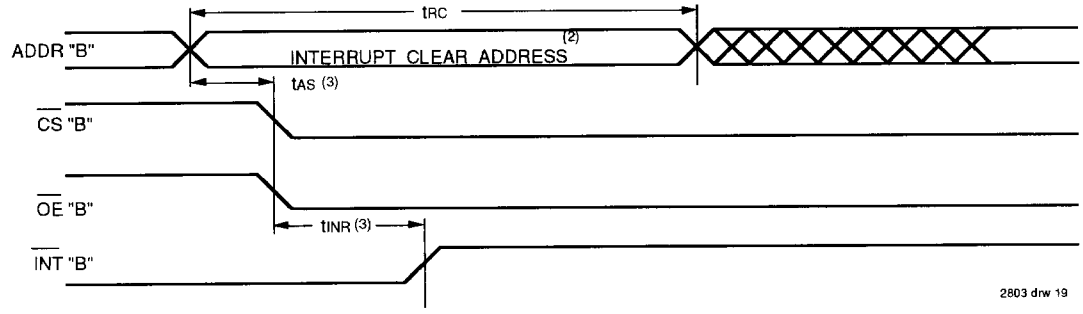


2803 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See InterruptTruth Table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable is de-asserted first.

7-8-13

WAVEFORM OF INTERRUPT TIMING(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See InterruptTruth Table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable is de-asserted first.

TRUTH TABLE I: NON-CONTENTION READ/WRITE CONTROL(1, 2, 3)

Inputs(1)						Outputs		
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8 - I/O15	I/O0 - I/O7	Mode
H	X	X	X	X	H	Hi-Z	Hi-Z	Deselected: Power Down
X	X	X	H	H	H	Hi-Z	Hi-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	Hi-Z	Write to Upper Byte Only
L	L	X	H	L	H	Hi-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	Hi-Z	Read Upper Byte Only
L	H	L	H	L	H	Hi-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	Hi-Z	Hi-Z	Outputs Disabled

NOTES:
1. $A_{0L} - A_{12} \neq A_{0R} - A_{12R}$

2803 tbl 13

TRUTH TABLE II: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CS}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8 - I/O15	I/O0 - I/O7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

NOTES:
1. $A_{0L} - A_{12} \neq A_{0R} - A_{12R}$

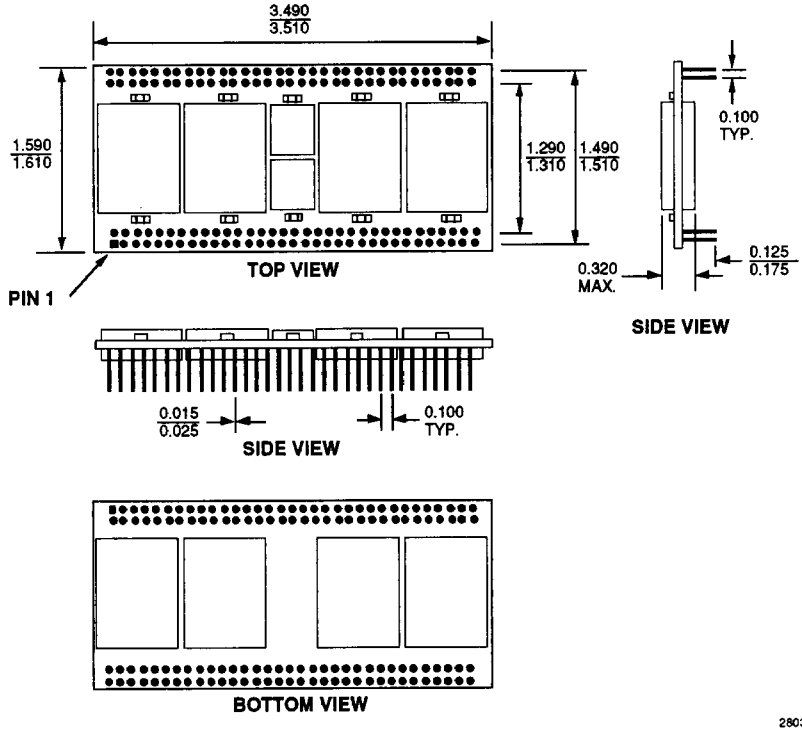
2803 tbl 14

INTERRUPT/BUSY FLAGS, DEPTH/WIDTH EXPANSION, MASTER/SLAVE CONTROL, SEMPAHORES

For more details regarding Interrupt/Busy flags, depth/width expansion, master/slave control, or semaphore operations, please consult the IDT7025 datasheet.

7-8-14

PACKAGE DIMENSIONS
7MB1006

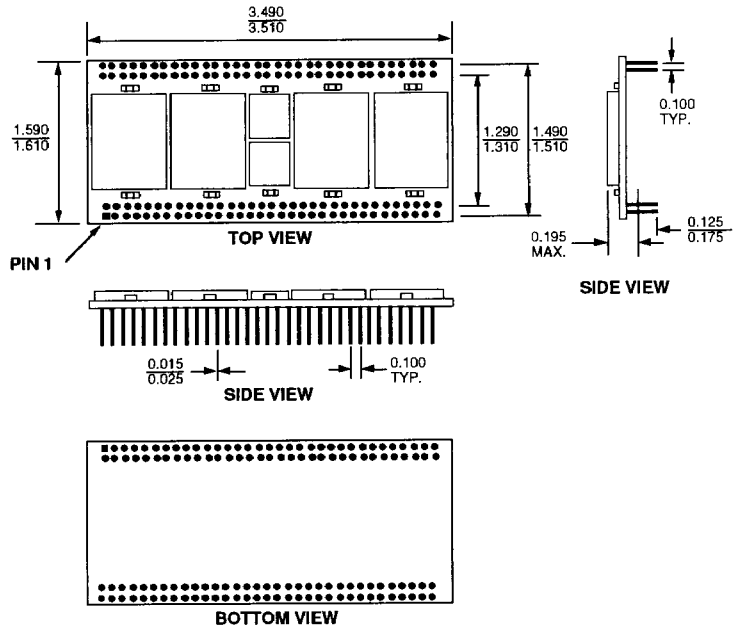


2803 drw 20

T-8-15

PACKAGE DIMENSIONS

7MB1008



2803 drw 21

7

7-8-16