F95029

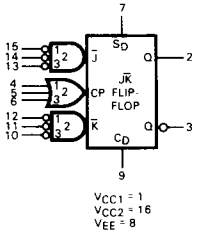
EDGE-TRIGGERED $\overline{J}$ $\overline{K}$ FLIP-FLOP

DESCRIPTION — The F95029 is a very high speed Edge-Triggered $\overline{J}$ $\overline{K}$ Flip-Flop designed for maximum speed. The multiple $\overline{J}$, $\overline{K}$, and clock inputs permit its use in most register and counter applications without extra gates. Careful control of clock pulse rise and fall times is not required, as the master/slave design has a dc threshold on the clock input which initiates the transition on the output.

Data is accepted by the master while the clock is LOW. Data present just prior to the rising edge of the clock (as specified by the set-up and hold times) is trapped in the master and transferred to the slave on the rising edge of the clock. Although this device uses a master/slave design, it is not "ones catching" (it responds only to the rising edge of the clock pulse).

The asynchronous inputs provide ability to control the state of the flip-flop independent of the conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided.

LOGIC SYMBOL



V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

PIN NAMES

$\overline{J}$	Synchronous Set Input (Active LOW)
$\overline{K}$	Synchronous Reset Input (Active LOW)
CP	Clock Input
S_D	Asynchronous Set Input
C_D	Asynchronous Clear Input
Q	True Output
$\overline{Q}$	Complement Output

TRUTH TABLES

SYNCHRONOUS

$\overline{J}_1$	$\overline{J}_2$	$\overline{J}_3$	$\overline{K}_1$	$\overline{K}_2$	$\overline{K}_3$	Q_{t+1}
L	L	L	L	L	L	$\overline{Q}_t$
L	L	L	One or More HIGH			H
One or More HIGH			L	L	L	L
One or More HIGH			One or More HIGH			Q_t

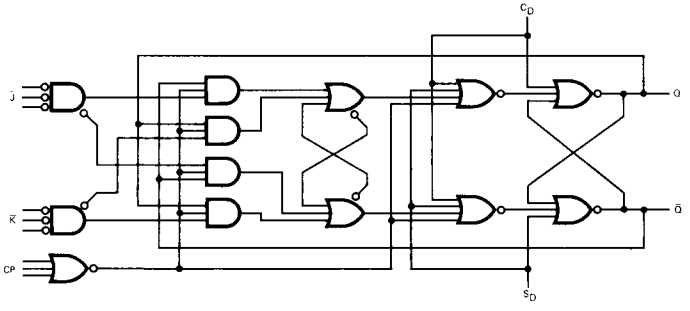
ASYNCHRONOUS

C_D	S_D	Q
L	L	Sync
L	H	H
H	L	L
H	H	Undetermined

L = LOW Voltage Level
H = HIGH Voltage Level

Q_t = Present Output State
Q_{t+1} = Output State after next Clock

LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays, as many gate functions are achieved internally without incurring a full gate delay.

DC CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output Voltage HIGH	-1025	-965	-880	mV	$V_{IN} = V_{IHA}$ or V_{ILB} per Truth Table	Loading is 50Ω to -2.0 V
V_{OL}	Output Voltage LOW	-1810	-1705	-1620	mV		
V_{OHC}	Output Voltage HIGH	-1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	
V_{OLC}	Output Voltage LOW			-1610	mV		
V_{IH}	Input Voltage HIGH	-1165		-880	mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1810		-1475	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			340	µA	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW	0.5			µA	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	-46	-36		mA	CP to V_{IL}, Other Inputs & Outputs Open	

DC CHARACTERISTICS: V_{EE} = -4.7 to -6.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OHC}	Output Voltage HIGH	-1050			mV	$V_{IN} = V_{IHB}$ or V_{ILA} per Truth Table	Loading is 50Ω to -2.0 V
V_{OLC}	Output Voltage LOW			-1595	mV		
V_{IH}	Input Voltage HIGH	-1155			mV	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW			-1500	mV	Guaranteed Input Voltage LOW for All Inputs	
I_{EE}	Power Supply Current	-52	-40		mA	CP to V_{IL}, Other Inputs & Outputs Open V_{EE} = -6.2 V	

SWITCHING CHARACTERISTICS: V_{EE} = -5.2 V, T_A = 75°C

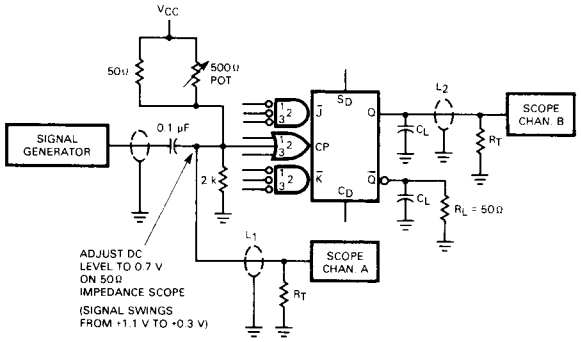
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{count}	Toggle Frequency	160	250		MHz	See Figure 1
t_{PHL}, t_{PHL}	Propagation Delay Clock to Output	1.6	2.8	4.4	ns	See Figure 2
t_{PLH}, t_{PHL}	Propagation Delay S_D, C_D to Output	1.1	3.6	6.3	ns	See Figure 3
t_{TLH} t_{THL}	Output Transition Time 20% to 80%, 80% to 20%	0.9	2.0	3.3	ns	See Figure 2

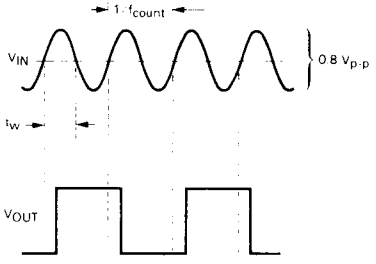
8

SWITCHING SET-UP REQUIREMENTS: V_{EE} = -5.2 V, T_A = 0°C to 75°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_s	Set-up Time, $\overline{J}$ or $\overline{K}$ to Clock	1.0	0		ns	See Figure 4
t_h	Hold Time, $\overline{J}$ or $\overline{K}$ to Clock	1.0	0		ns	
t_w	Clock Pulse Width		2.0		ns	See Figure 1

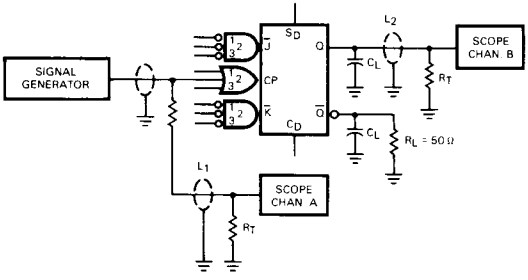
SWITCHING CIRCUITS AND WAVEFORMS

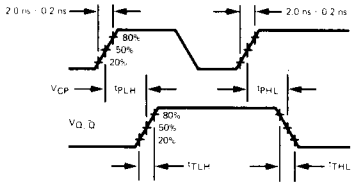




L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

Fig. 1. Minimum Clock Frequency

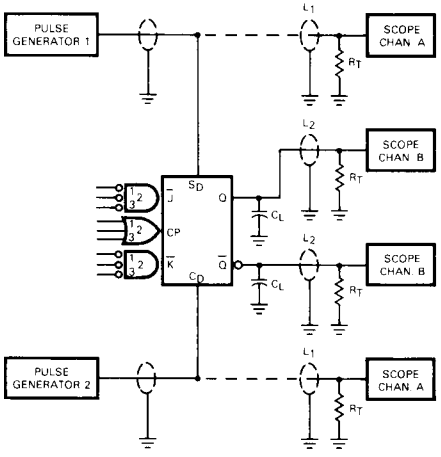


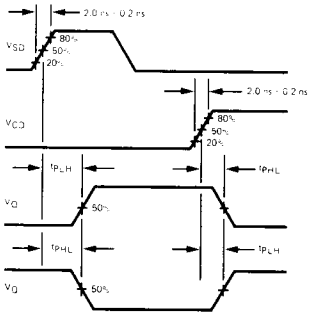


L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = -3.2 V

Fig. 2. Clock Input to Output

SWITCHING CIRCUITS AND WAVEFORMS (Cont'd.)





L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 3. Asynchronous Input to Output

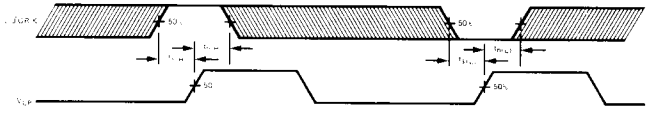
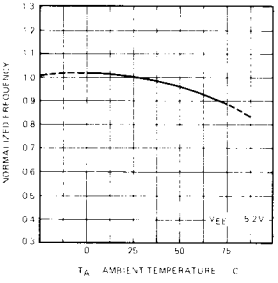


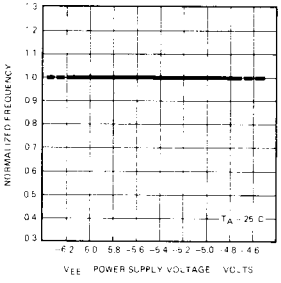
Fig. 4. Set-Up and Hold Time Waveforms

TYPICAL ELECTRICAL CHARACTERISTICS

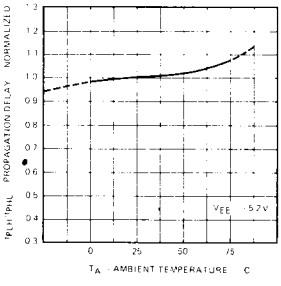
TOGGLE RATE VERSUS TEMPERATURE



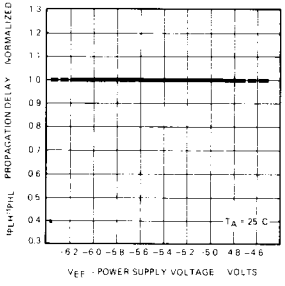
TOGGLE RATE VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



8