HB56A840BR Series

8,388,608-word × 40-bit High Density Dynamic RAM Module

HITACHI

ADE-203-
Rev. 0.0
Dec. 1, 1995

Description

The HB56A840BR is a 8 M × 40 dynamic RAM module, mounted 20 pieces of 16-Mbit DRAM (HM5116400BS) sealed in SOJ package. An outline of the HB56A840BR is 72-pin single in-line package. Therefore, the HB56A840BR makes high density mounting possible without surface mount technology. The HB56A840BR provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ only on the one side its module board.

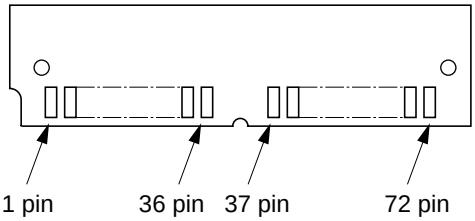
Features

- 72-pin single in-line package
  - Lead pitch : 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - Access time : 60 ns/70 ns/80 ns (max)
- Low power dissipation
  - Active mode: 4.47 W/3.94 W/3.68 W (max)
  - Standby mode: 210 mW (max)
- Fast page mode capability
- 4,096 refresh cycle: 64 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package	Contact pad
HB56A840BR-6B	60 ns	72-pin SIP socket type	gold
HB56A840BR-7B	70 ns		
HB56A840BR-8B	80 ns		

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	$\overline{OE}$	37	DQ19	55	DQ28
2	DQ0	20	DQ8	38	DQ20	56	DQ29
3	DQ1	21	DQ9	39	V_{SS}	57	DQ30
4	DQ2	22	DQ10	40	$\overline{CAS0}$	58	DQ31
5	DQ3	23	DQ11	41	A10	59	V_{CC}
6	DQ4	24	DQ12	42	A11	60	DQ32
7	DQ5	25	DQ13	43	$\overline{CAS1}$	61	DQ33
8	DQ6	26	DQ14	44	$\overline{RAS0}$	62	DQ34
9	DQ7	27	DQ15	45	$\overline{RAS1}$	63	DQ35
10	V_{CC}	28	A7	46	DQ21	64	DQ36
11	PD4	29	DQ16	47	$\overline{WE}$	65	DQ37
12	A0	30	V_{CC}	48	×40 (V_{SS})	66	DQ38
13	A1	31	A8	49	DQ22	67	PD0
14	A2	32	A9	50	DQ23	68	PD1
15	A3	33	NC	51	DQ24	69	PD2
16	A4	34	NC	52	DQ25	70	PD3
17	A5	35	DQ17	53	DQ26	71	DQ39
18	A6	36	DQ18	54	DQ27	72	V_{SS}

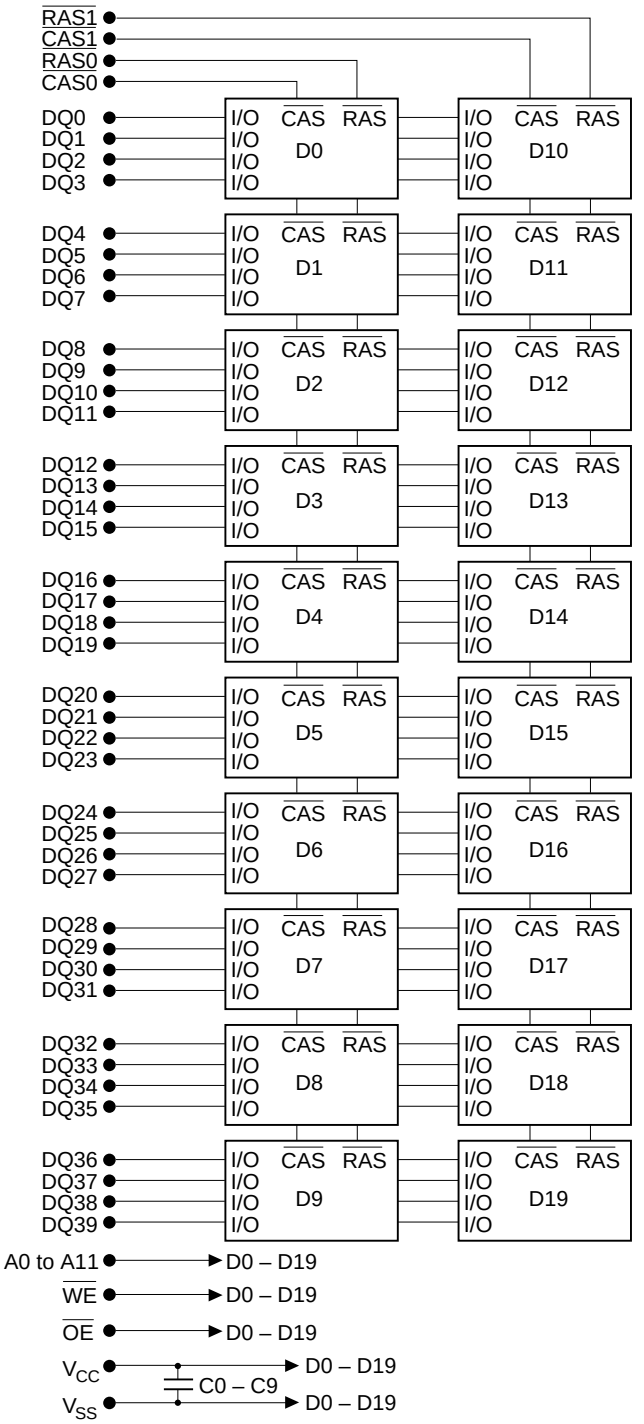
Pin Description

Pin Name	Function
A0–A11	Address input: A0–A11 Row address: A0–A11 Column address: A0–A9 Refresh address A0–A11
DQ0–DQ39	Data-in/data-out
$\overline{CAS0}$, $\overline{CAS1}$	Column address strobe
$\overline{RAS0}$, $\overline{RAS1}$	Row address strobe
$\overline{WE}$	Read/write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD0–PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56A840BR		
Pin No.	**Pin Name**	**60 ns**	**70 ns**	**80 ns**
67	PD0	NC	NC	NC
68	PD1	V_{SS}	V_{SS}	V_{SS}
69	PD2	NC	V_{SS}	NC
70	PD3	NC	NC	V_{SS}
11	PD4	V_{SS}	V_{SS}	V_{SS}

Block Diagram



Note: D0 – D19 : HM5116400

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	10	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to +70 °C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56A840BR								
		60 ns		70 ns		80 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	**Notes**
Operating current	I_{CC1}	—	850	—	750	—	700	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	40	—	40	—	40	mA	TTL interface, $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, Dout = High-Z	
		—	20	—	20	—	20	mA	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ ≥V_{CC} –0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	850	—	750	—	700	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	100	—	100	—	100	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	850	—	750	—	700	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	750	—	650	—	550	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	140	pF	1
Input capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I2}	—	160	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	90	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	25	pF	1, 2

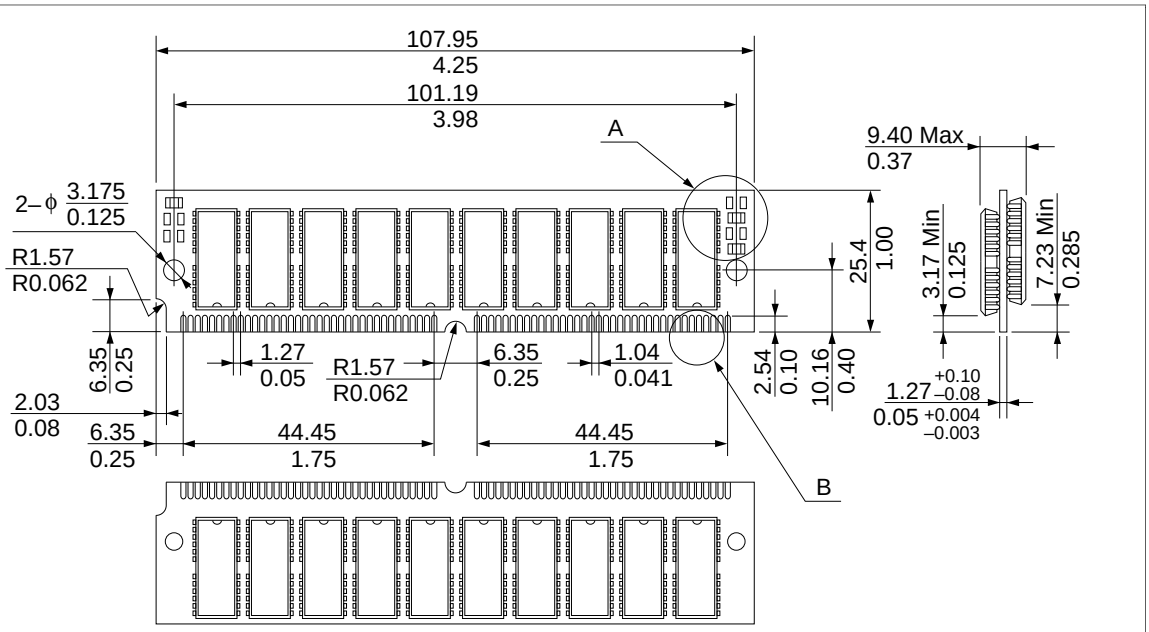
Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

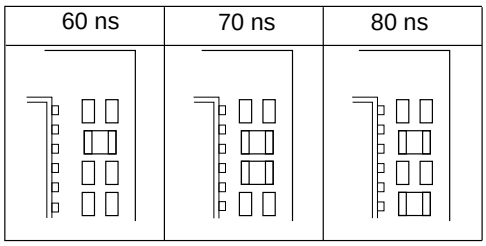
- Refer to the HM5116400B Series data sheet.

Physical Outline

Unit: mm/inch



Detail A



Detail B