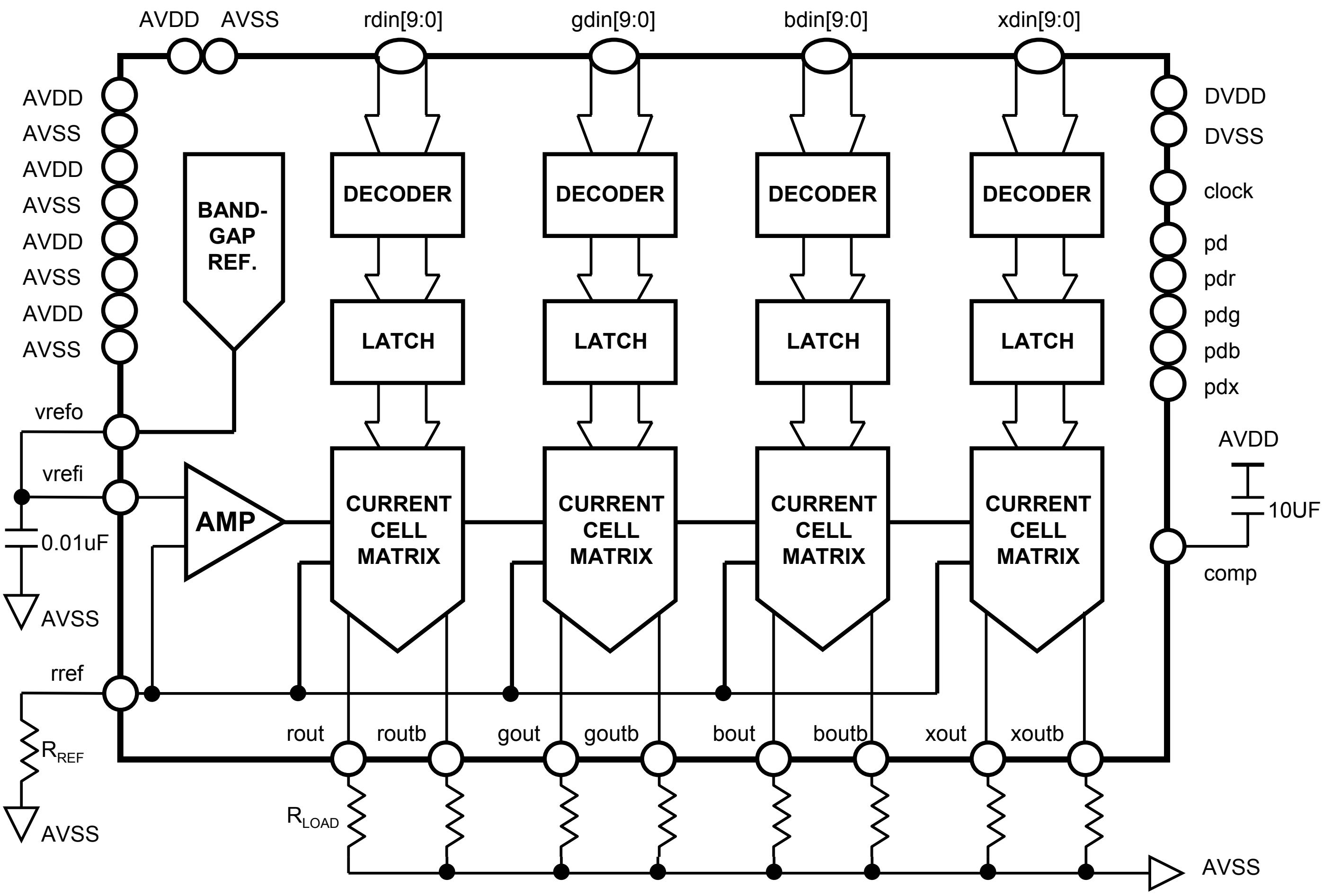
1. General Description

H18GDA13M is a CMOS(0.18㎛, 1-poly, 3-metal) high speed 10-bit, 4-channel DAC (Digital-to-Analog Converter) which has a high stable bandgap reference. Using highly accurate current cell and de-glitch circuit, the non-linearity error and glitch are decreased. This DAC is applied to video signal processing system such as HDTV, Digital TV, camcorder and other graphic display systems.

2. Features

- Analog output range : AVSS to AVSS + 1.28 (@ 37.5Ω load)
- Resolution : Max. 10 bits (≤ ±0.5 LSB DNL error)
- Maximum conversion rate : 108 Msps
- Power supply : 1.8V(digital block) / 3.3V(analog block)
- Power dissipation : 500mW (@108Msps with 37.5Ω load)
- Power-down mode : active high
- Process : 0.18㎛ CMOS generic Process (1-poly, 3-metal)
- Cell Size : 1526㎛ × 754㎛(with guard ring)

3. Block Diagram with Recommended Application Circuit



4. Pin Descriptions

Name	Type	Description
DVDD	Power	Digital power (= 1.8V)
DVSS	Ground	Digital ground
AVDD	Power	Analog power (= 3.3V)
AVSS	Ground	Analog ground
vrefo	Output	Voltage reference output
vrefi	Input	Voltage reference input
rref	Input	Resistor reference
comp	Input	Compensation
rout	Output	R-channel current output
routb	Output	R-channel current output inverted
gout	Output	G-channel current output
goutb	Output	G-channel current output inverted
bout	Output	B-channel current output
boutb	Output	B-channel current output inverted
xout	Output	X-channel current output
xoutb	Output	X-channel current output inverted
rdin[9:0]*	Input	R-channel data input
gdin[9:0]*	Input	G-channel data input
bdin[9:0]*	Input	B-channel data input
xdin[9:0]*	Input	X-channel data input
clock	Input	Clock input
pdr	Input	R-channel power-down
pdg	Input	G-channel power-down
pdb	Input	B-channel power-down
pdx	Input	X-channel power-down
pd	Input	All power-down

* The most significant bit is rdin[9], gdin[9], bdin[9] and xdin[9] in each digital input(bus) signal.

5. Function Description

Digital inputs are sampled at falling clock edge and converted to analog signal with one clock latency. The detailed description is as follows.

The decoder and latch blocks sample the digital inputs at falling clock edge. And the following current cell block controls the output current according to the inputs. The analog output voltage arithmetic expression is as follows.

$$V_{OUT} = AVSS + R_{LOAD} \times I_{OUT}$$

Where AVSS is ground and R_{LOAD} is output load resistance. I_{OUT} is determined by reference resistance and bias voltage as following expression.

$$I_{OUT} = I_{REF} / 265.76 \times (\text{ digital input values}), \quad \text{where } I_{REF} = vrefi / R_{REF}$$

R_{REF} is 140Ω with R_{LOAD} of 37.5Ω, and vrefi is connected to the vrefo which is output voltage of band-gap reference of 1.24V. The analog output swing range is AVSS to AVSS+1.28V typically.

<table>
<tr><th>Mode</th><th>pd</th><th>pdr</th><th>pdg</th><th>pdb</th><th>pdx</th></tr>
<tr><td>Normal Operation</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>All Power-down</td><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>R-ch Power-down</td><td rowspan="4" colspan="5">The channel power-down is not supported on the fixed R_{REF}. Just you can adopt channels along with adjustment of rref in your application. In this case, unused channels are power-downed.</td></tr>
<tr><td>G-ch Power-down</td></tr>
<tr><td>B-ch Power-down</td></tr>
<tr><td>X-ch Power-down</td></tr>
</table>

6. Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD	Operating Voltage	2.97	3.30	3.63	V
DVDD	Operating Voltage	1.62	1.80	1.98	V
VIL	Input Low Voltage	0	-	0.3DVDD	V
VIH	Input High Voltage	0.7DVDD	-	DVDD	V

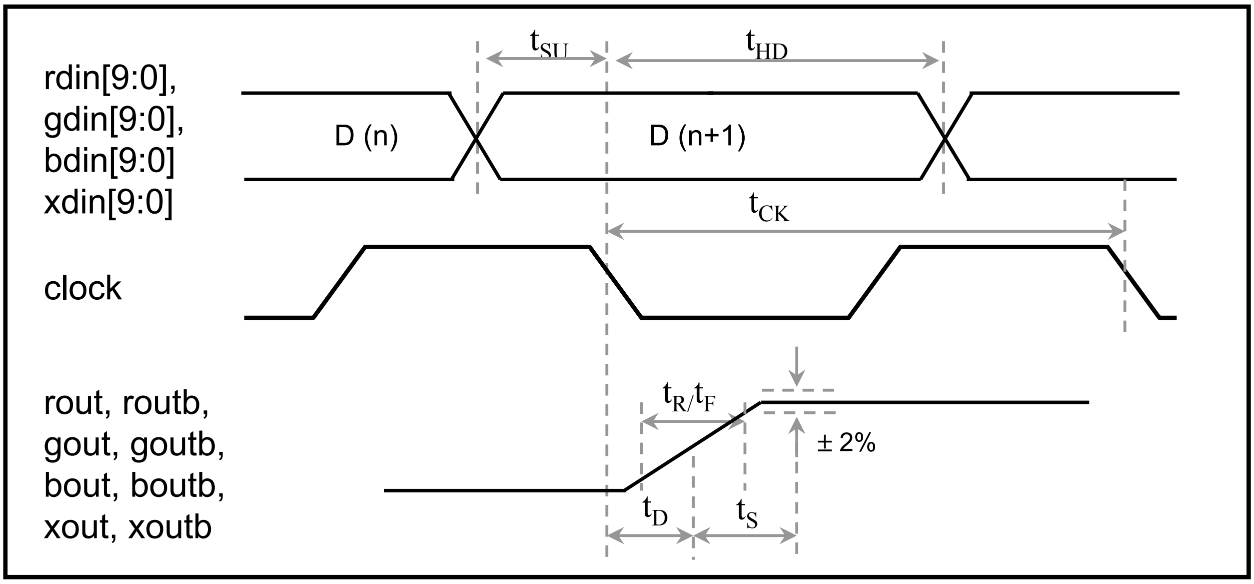
7. Electrical Characteristics

(Temp = 25 ℃, AVDD = 3.3V, R_{LOAD} = 37.5Ω, R_{REF} = 140Ω)

Symbol	Parameter	Min.	Typ.	Max.	Unit
IDD	Static Current Dynamic Current @108 MHz		164	 TBD	mA mA
	Resolution			10	bits
INL	Integral Non-linearity	-1.0	±0.5	+1.0	LSB
DNL	Differential Non-linearity	-1.0	±0.5	+1.0	LSB
	Ch. to Ch. Mismatch*		2		%
SFDR	Dynamic Range				dB
IFS	Full Scale Current		34.08		mA
t_{CK}	Clock Period	9.2			nS
	Clock Width High/Low	1.0/1.0			nS
t_{SU}	Setup Time	0.5			nS
t_{HD}	Hold Time	0.5			nS
t_D	Clock to Valid Output		2.5	4.5	nS
t_R	Rise Time		2.2	3.2	nS
t_F	Fall Time		2.2	3.2	nS
t_S	Settling Time		4.0	8.0	nS
vrefo	Voltage Drift (0 ~ 125 ℃)	1.22	1.24	1.26	V

* Channel to channel mismatch, which is measured on the full scale current I_{FS} output with R_{LOAD}
Definition : [{max ($V_{OUT,R}$, $V_{OUT,G}$, $V_{OUT,B}$, $V_{OUT,X}$) - min ($V_{OUT,R}$, $V_{OUT,G}$, $V_{OUT,B}$, $V_{OUT,X}$)} / avg ($V_{OUT,R}$, $V_{OUT,G}$, $V_{OUT,B}$, $V_{OUT,X}$)] x 100%

8. Timing Diagram

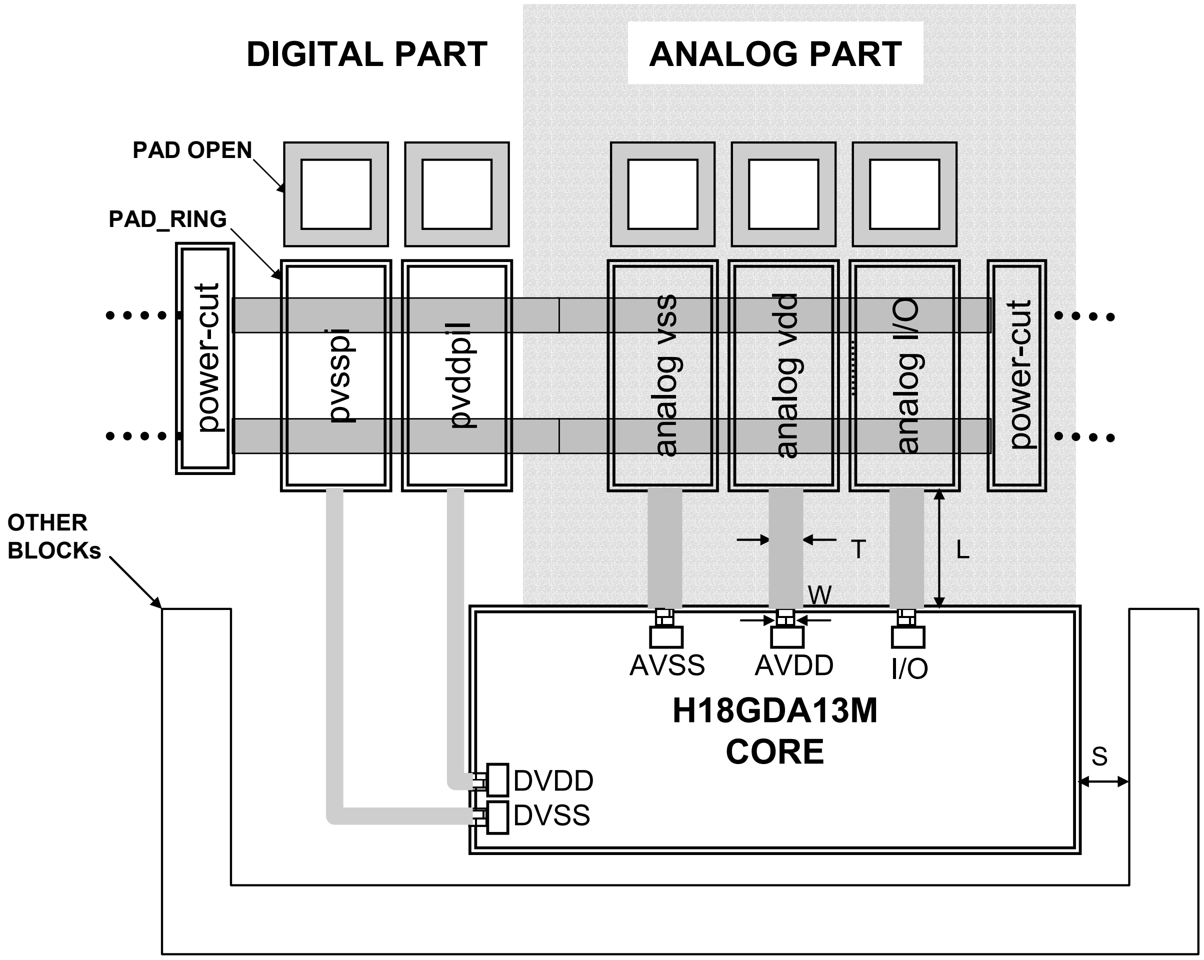


9. Layout Guide

Power supply de-coupling and analog signal routing

The analog and the digital powers of the DAC should be separated from each other to prevent the glitch which is coupled into the analog power from digital circuitry. The I/O powers are also separated as shown in Figure 1.

The analog signals such as analog output, rref and vrefi should be placed near their pads as possible. The recommended analog pads location is as follows.



* T≥ W (connector width in phantom)
* L : As short as possible from pad.
* S : the recommended space is more than 50um.
* Dual pvddas can be used as a AVDD.
* Dual pvssas can be used as a AVSS.
* Dual pa3 can be used as a analog I/O pad.
* The pdo can be used as a power-cutting cell