

SED1651

LOW-POWER 100-BIT LCD COMMON DRIVER

DESCRIPTION

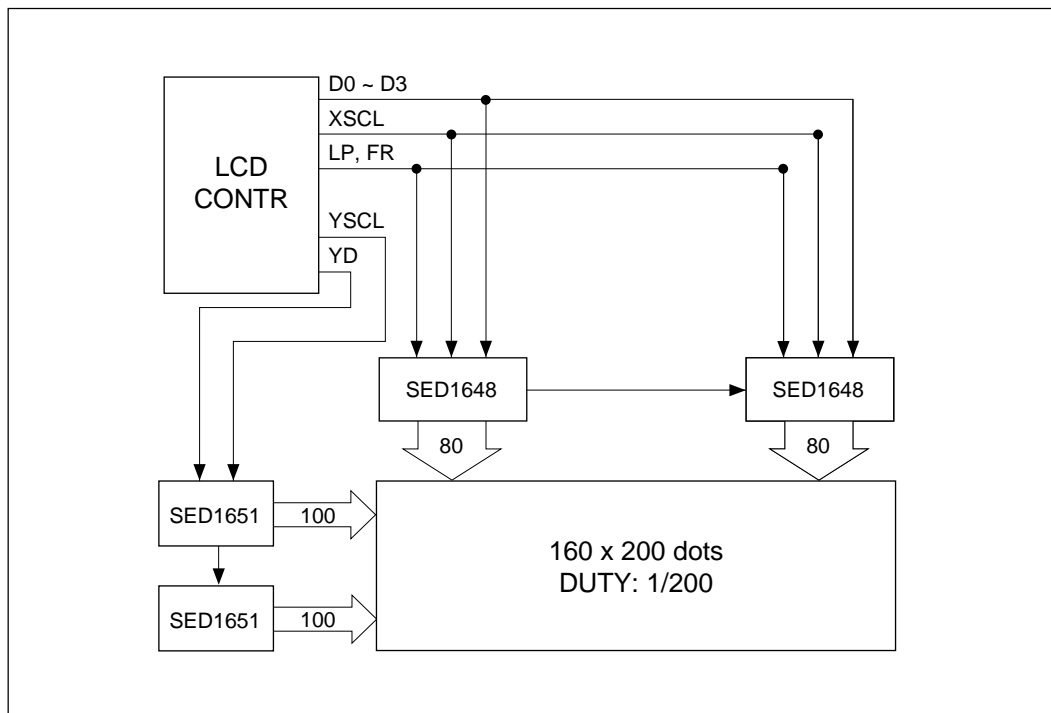
The SED1651 is a 100-output dot matrix LCD common (row) driver for driving high-capacity LCD panels at duty cycles higher than 1/64 (up to 1/300). The LSI has a wide range of the LCD driving voltages, and has its maximum drive voltage, V_O , isolated from V_{DD} for the flexibility of bias voltage generation.

The SED1651 is used in conjunction with the SED1648 (80-output segment driver) or the SED1640 (80-bit segment driver) to drive a large-capacity dot matrix LCD panel.

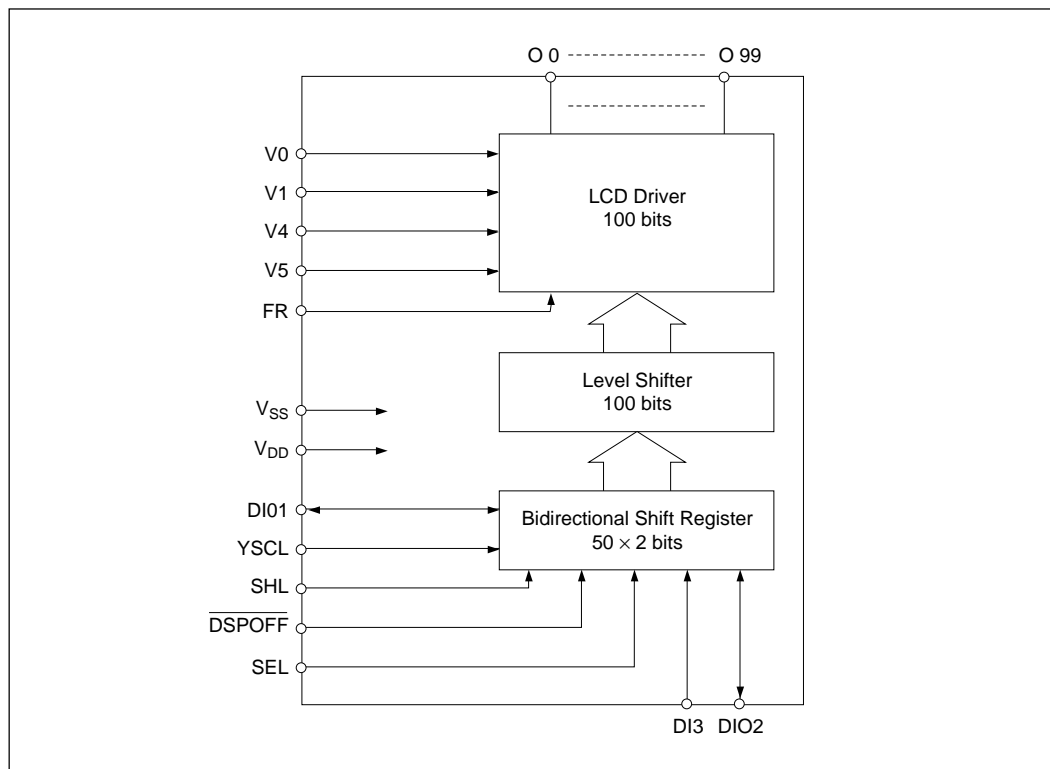
FEATURES

- Low-power CMOS technology
- 100-bit common (row) driver
- Low output impedance 750 Ω (typ)
- Duty cycle 1/64 to 1/300
- Ability to adjust offset bias of the LCD relative to V_{DD}
- Non-biased display off function
- Pin selection of the output shift direction
- LCD voltage -8 to -28V
- Supply voltage 2.7 to 5.5V
- Package Slim Al pad DIE (DoA)

SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

● Enable Shift Register

This is a bidirectional shift register used for transmitting common data. The shift register has a 50×2 bit structure, and is selectable to 50×2 bits or 100 bits depending on the setting of SEL.

When the 50×2 bit configuration is selected, the input for the second 50 bit shift register is DI3.

● Level Shifter

The level shifter is a level interface circuit which converts the signal voltage level from a logic circuit level to the LC driver voltage level.

● LCD Driver

The LCD driver outputs the LC drive voltage.

The relationship between the display blanking signal \overline{DSPOFF} , the contents of the shift register, the AC signal FR, and the On output voltage is as follows:

\overline{DSPOFF}	Contents of Shift Register	FR	O Output Voltage	
H	H	H	V5	(Select level)
		L	V0	
	L	H	V1	(Non-select level)
		L	V4	
L	—	—	V0	—

■ PIN DESCRIPTION

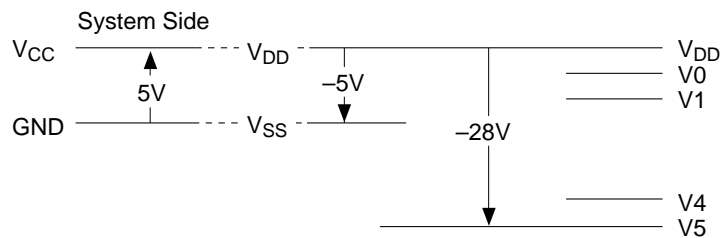
Pin Name	I/O	Function	No. of Pins																																			
O0 to O99	O	Common (row) output to drive LC. Output transition occurs on falling edge of YSCL.	100																																			
DIO1 DIO2	I/O	50 × 2 bit bi-directional shift register serial data I/O. This is set to input or output depending on the level of the SHL input. Output transition occurs on falling edge of YSCL.	2																																			
DI3	I	Scan pulse input terminal of the 50 × 2 structure. When SEL = L, DI3 = Vss or GND.	1																																			
SEL	I	Bi-directional shift register operating mode select input H: 50 × 2 (DI3 input) L: 100	1																																			
YSCL	I	Serial data shift clock input (shifts scan data on falling edge).	1																																			
SHL	I	Shift direction select and DIO terminal I/O control input. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th rowspan="2">SHL</th> <th colspan="6">O Output Shift Direction</th> <th colspan="2">DIO</th> </tr> <tr> <th>1</th> <th>2</th> <th>3</th> <th>4</th> <th>5</th> <th>6</th> <th>1</th> <th>2</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>0</td> <td>→</td> <td>49</td> <td>50</td> <td>→</td> <td>99</td> <td>I</td> <td>O</td> </tr> <tr> <td>H</td> <td>99</td> <td>→</td> <td>50</td> <td>49</td> <td>→</td> <td>0</td> <td>O</td> <td>I</td> </tr> </tbody> </table> <p>When SEL = "H", the DI3 input is input to O50 (SHL = "L") or O49 (SHL = "H"). When SEL = "L", the DI3 input is ignored and the DIO input is continuously shifted.</p>	SHL	O Output Shift Direction						DIO		1	2	3	4	5	6	1	2	L	0	→	49	50	→	99	I	O	H	99	→	50	49	→	0	O	I	1
SHL	O Output Shift Direction						DIO																															
	1	2	3	4	5	6	1	2																														
L	0	→	49	50	→	99	I	O																														
H	99	→	50	49	→	0	O	I																														
DSPOFF	I	LC display blanking control input. A low level clears the shift register, immediately causing all common outputs to go to V0.	1																																			
FR	I	LC drive output AC signal input.	1																																			
VDD, Vss	Power	Power source for logic: VDD: 0V (GND) Vss: -2.7 to -5.5V	3																																			
V0, V1, V4, V5	Power	LC Drive Circuit Power: V5: -8 to -28V VDD ≥ V0 ≥ V1 > V4 ≥ V5	8																																			

Total 119

■ ELECTRICAL CHARACTERISTICS
 ● Absolute Maximum Ratings

Parameter	Symbol	Condition	Unit
Power voltage (1)	V _{SS}	-7.0 to +0.3	V
Power voltage (2)	V ₅	-30.0 to +0.3	V
Power voltage (3)	V ₀ , V ₁ , V ₄	V ₅ - 0.3 to + 0.3	V
Input voltage	V _I	V _{SS} - 0.3 to + 0.3	V
Output voltage	V _O	V _{SS} - 0.3 to + 0.3	V
Output current (1)	I _O	20	mA
Output current (2)	I _{OCOM}	20	mA
Operating temperature	T _{opr}	-40 to +85	°C
Storage temperature (1)	T _{stg1}	-65 to +150	°C

Notes: *1. The voltages are all relative to V_{DD} = 0V.
 *2. Ensure that the relationship between V₀, V₁, V₄, and V₅ is always as follows: V_{DD} ≥ V₀ ≥ V₁ ≥ V₄ ≥ V₅.



*3. The LSI may be permanently damaged if the logic system power is floating or V_{SS} is less than or equal to -2.6V when power is applied to the LC drive circuit system. Special caution must be paid to the power sequences when turning the power on and off.

● DC Electrical Characteristics

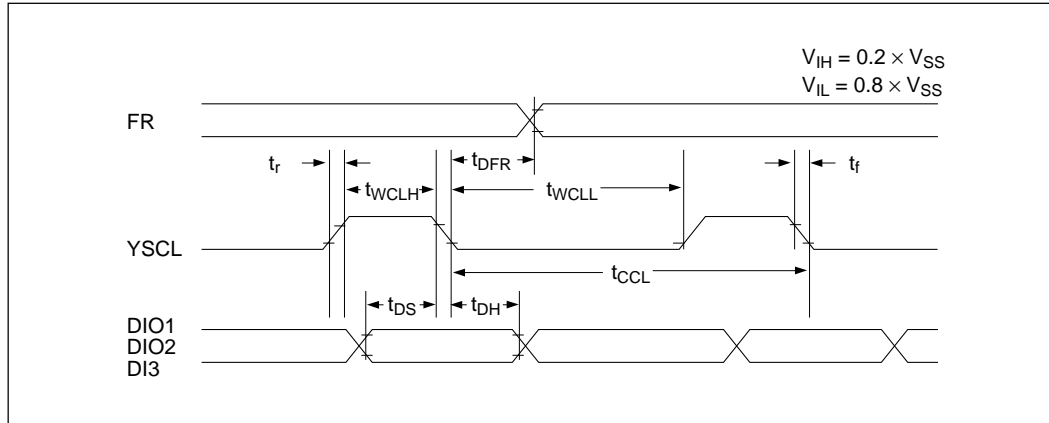
Unless otherwise specified, V_{DD} = V_O = 0V,
V_{SS} = -5.5 to -2.7V, T_a = -40 to 85°C

Parameter	Symbol	Conditions	Applicable Pins	Min	Typ	Max	Unit
Power voltage (1)	V _{SS}		V _{SS}	-5.5	-5.0	-2.7	V
Recommended operating voltage	V ₅		V ₅	-28.0	—	-12.0	V
Possible operating voltage	V ₅	Function operation	V ₅	—	—	-8.0	V
Power voltage (2)	V _O		V _O	-2.5	—	0	V
Power voltage (3)	V ₁		V ₁	2/9 × V ₅	—	V _{DD}	V
Power voltage (4)	V ₄		V ₄	V ₅	—	7/9 × V ₅	V
High-level input voltage	V _{IH}		DIO1, DIO2, FR, YSCL, SHL, DI3, DSPOFF, SEL	0.2 × V _{SS}	—	—	V
Low-level input voltage	V _{IL}			—	—	0.8 × V _{SS}	V
High-level output voltage	V _{OH}	I _{OH} = -0.3mA	DIO1, DIO2	V _{DD} - 0.4	—	—	V
Low-level output voltage	V _{OL}	I _{OL} = 0.3mA		—	—	V _{SS} + 0.4	V
Input leakage current	I _{LI}	V _{SS} ≤ V _{IN} ≤ 0V	YSCL, SHL, DI3, DSPOFF, FR, SEL	—	—	2.0	μA
I/O leakage current	I _{LI/O}	V _{SS} ≤ V _{IN} ≤ 0V	DIO1, DIO2	—	—	5.0	μA
Static current	I _{BDS}	V ₅ = -12.0 to -28.0V V _{IH} = V _{DD} , V _{IL} = V _{SS}	V _{DD}	—	—	25	μA
Output resistance	R _{COM}	Δ V _{ON} = 0.5V, V _O = V _{DD} , V ₁ = -1.5V, V ₄ = -18.5V, V ₅ = -20.0V	O0 to O99	—	0.75	1.0	KΩ
Average operating consumption current (1)	I _{SS1}	V _{SS} = -5.0V, V _{IH} = V _{DD} , V _{IL} = V _{SS} , f _{YSCL} = 12KHz, Frame frequency = 60 Hz, Input data: 1/200; T _a = 25°C, Each duty cycle is "H", no load	V _{SS}	—	7	15	μA
				—	5	10	μA
Average operating consumption current (2)	I _{SS2}	V _{SS} = -5.0V, V _O = 0V, V ₁ = -1.5V, V ₄ = -18.5V, V _{EE} = V ₅ = -20.0V; other parameters are the same as for I _{SS1}	V ₅	—	7	15	μA
Input terminal capacitance	C _I	T _a = 25°C	YSCL, SHL, SEL, DSPOFF, FR, DI3	—	—	8	pF
I/O terminal capacitance	C _{I/O}		DIO1, DIO2	—	—	15	pF



SED1651

- AC Characteristics
 - Input Timing Characteristics



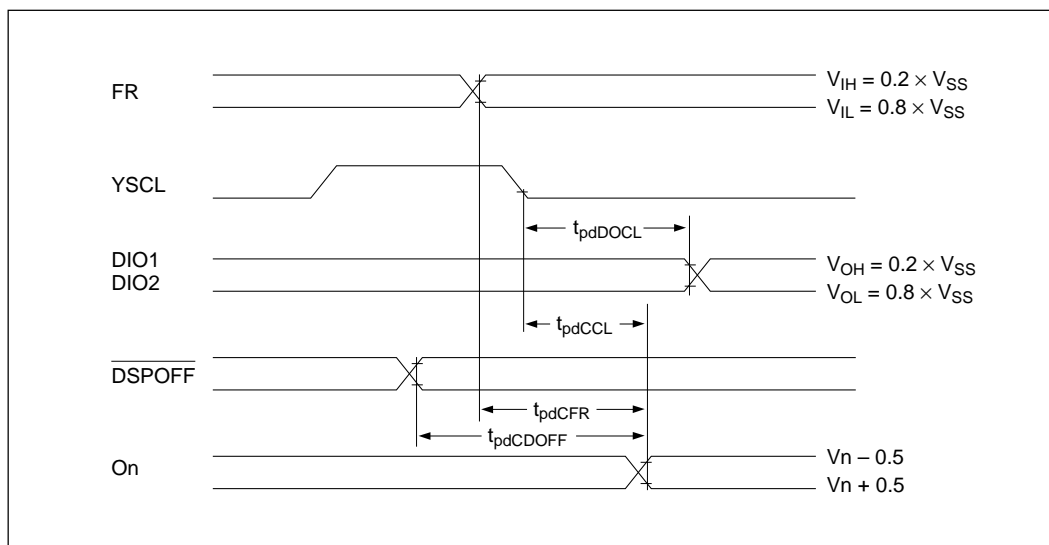
$V_{SS} = -5.0 \pm 10\%$, $T_a = -40$ to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	t_r		—	50	ns
Input signal fall time	t_f		—	50	ns
YSCL frequency	t_{CCL}		500	—	ns
YSCL high-level pulse width	t_{WCLH}		70	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		100	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		-300	300	ns

$V_{SS} = -4.5$ to -2.7V , $T_a = -40$ to 85°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input signal rise time	t_r		—	50	ns
Input signal fall time	t_f		—	50	ns
YSCL frequency	t_{CCL}		1000	—	ns
YSCL high-level pulse width	t_{WCLH}		160	—	ns
YSCL low-level pulse width	t_{WCLL}		330	—	ns
Data setup time	t_{DS}		200	—	ns
Data hold time	t_{DH}		10	—	ns
Allowable FR delay	t_{DFR}		-500	500	ns

o Output Timing Characteristics



$V_{SS} = -5.0V \pm 10\%$, $T_a = -40$ to $85^\circ C$

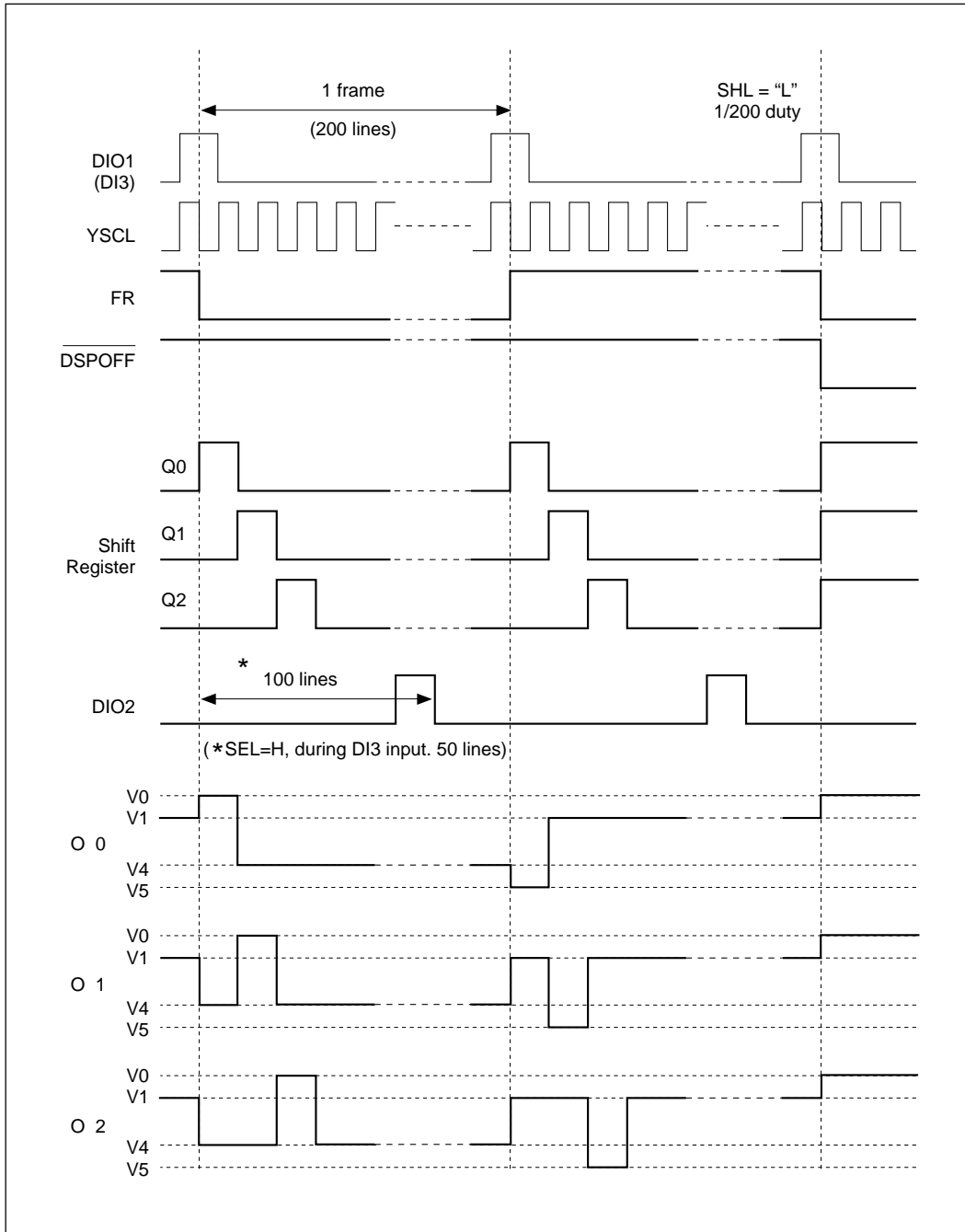
Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → DIO) delay time	t_{pdDOCL}	$CL = 15pF$	—	350	ns
(YSCL fall → On output) delay time	t_{pdCCL}	$V_5 = -12$ to $-28.0V$	—	1.0	μs
(DSPOFF → On output) delay time	$t_{pdCDOFF}$				
(FR → On output) delay time	t_{pdCFR}	$CL = 100pF$	—	1.0	μs

$V_{SS} = -4.5$ to $-2.7V$, $T_a = -40$ to $85^\circ C$

Parameter	Symbol	Conditions	Min	Max	Unit
(YSCL fall → DIO) delay time	t_{pdDOCL}	$CL = 15pF$	—	400	ns
(YSCL fall → On output) delay time	t_{pdCCL}	$V_5 = -12$ to $-28.0V$	—	2.0	μs
(DSPOFF → On output) delay time	$t_{pdCDOFF}$				
(FR → On output) delay time	t_{pdCFR}	$CL = 100pF$	—	2.0	μs

o **Timing Diagram**

Timing diagram (assuming 1/200 duty). (This diagram provided only as a reference)



■ LCD DRIVING POWER

● Method of Forming Each Voltage Level

The simplest way to obtain the voltage levels for driving the LCs is to use resistive voltage dividers between V5 and VDD, and to drive the LCs with op amp voltage followers.

In consideration of the use of op amps, V0 and VDD are separated and given separate terminals. When op amps are not going to be used, connect V0 to VDD.

When a resistive voltage divider is used, select the lowest resistances allowed by the system power supply tolerances.

Permanent damage may result to the LSI when there is serial resistance in the VDD power line. This is because the voltage drop that will occur at VDD will cause the power level relationships within the LCD (i.e., $V_{DD} \geq V0 \geq V1 > V4 \geq V5$) to fail.

When a guard resistance is inserted, voltage stabilization using a capacitance is necessary.

● Cautions During Power Up and Power Down

Because of the high voltage of the LC driving system of this LSI, if the power to the logic system is floating or if VSS is less than or equal to -2.5V when a high voltage is applied to the LC driving system, then too much current will flow, causing damage to the LSI.

It is recommended that the display off function (\overline{DSPOFF}) be used to keep the LCD driver output level at V0 until the LCD drive system voltage stabilizes.

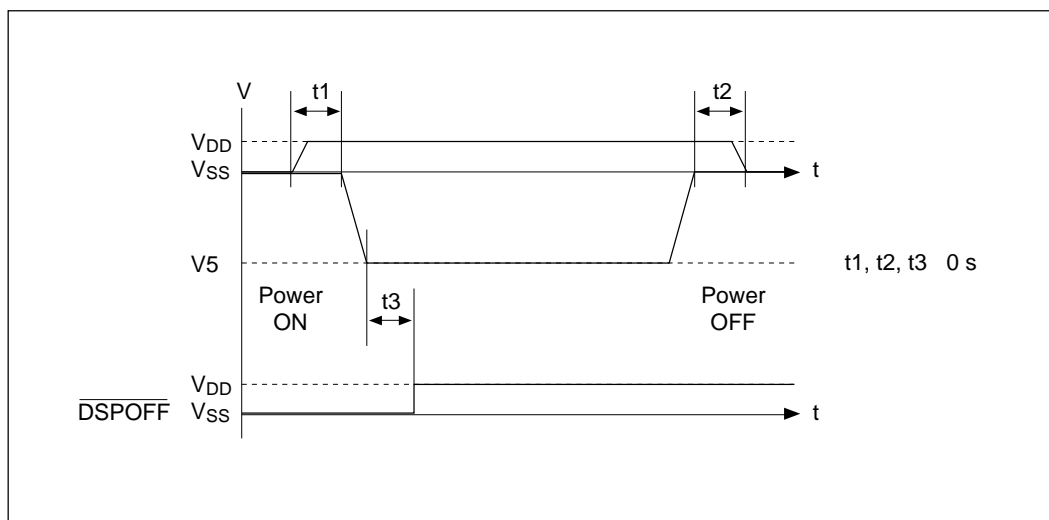
Follow the sequences below during power up and power down:

Power up: Logic system on → LC drive system on (or simultaneous)

Power down: LC drive system off → Logic system off (or simultaneous)

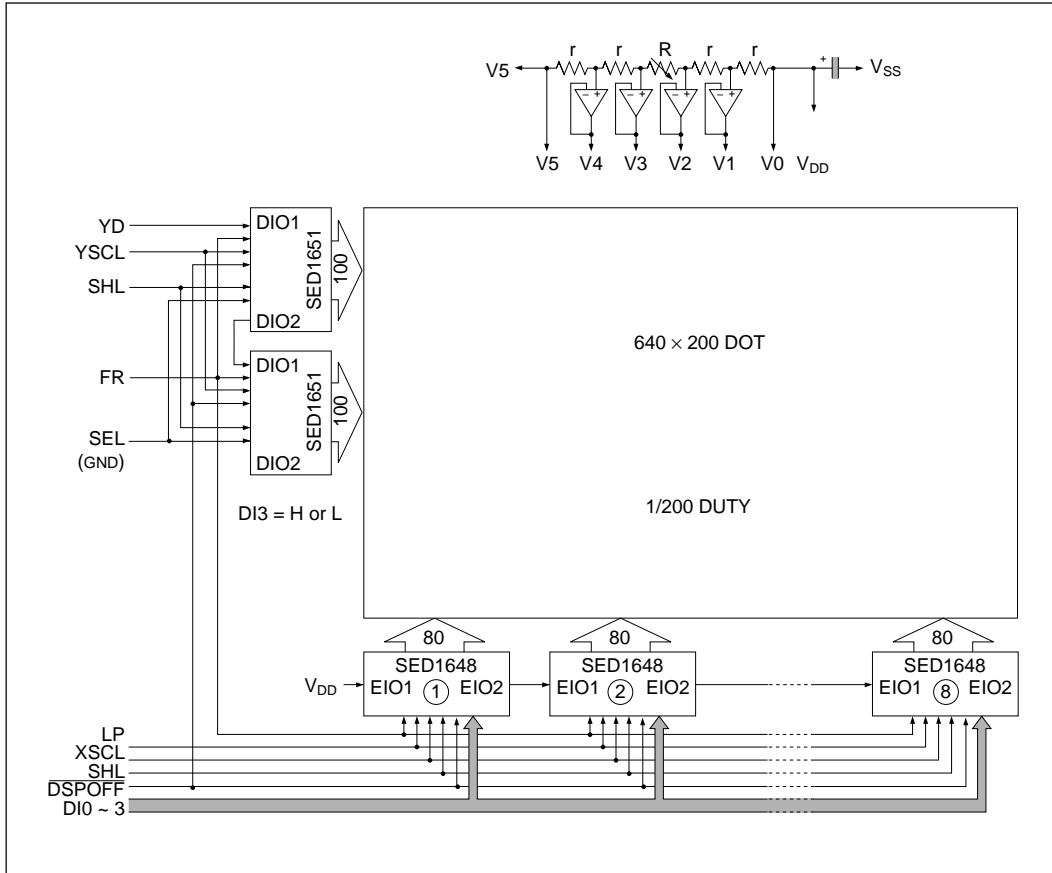
As a way to prevent excessive current, insert a high-speed fuse or guard resistance in series with the LC power source.

The optimal value of the guard resistance must be selected based on the capacitance of the LC cells.

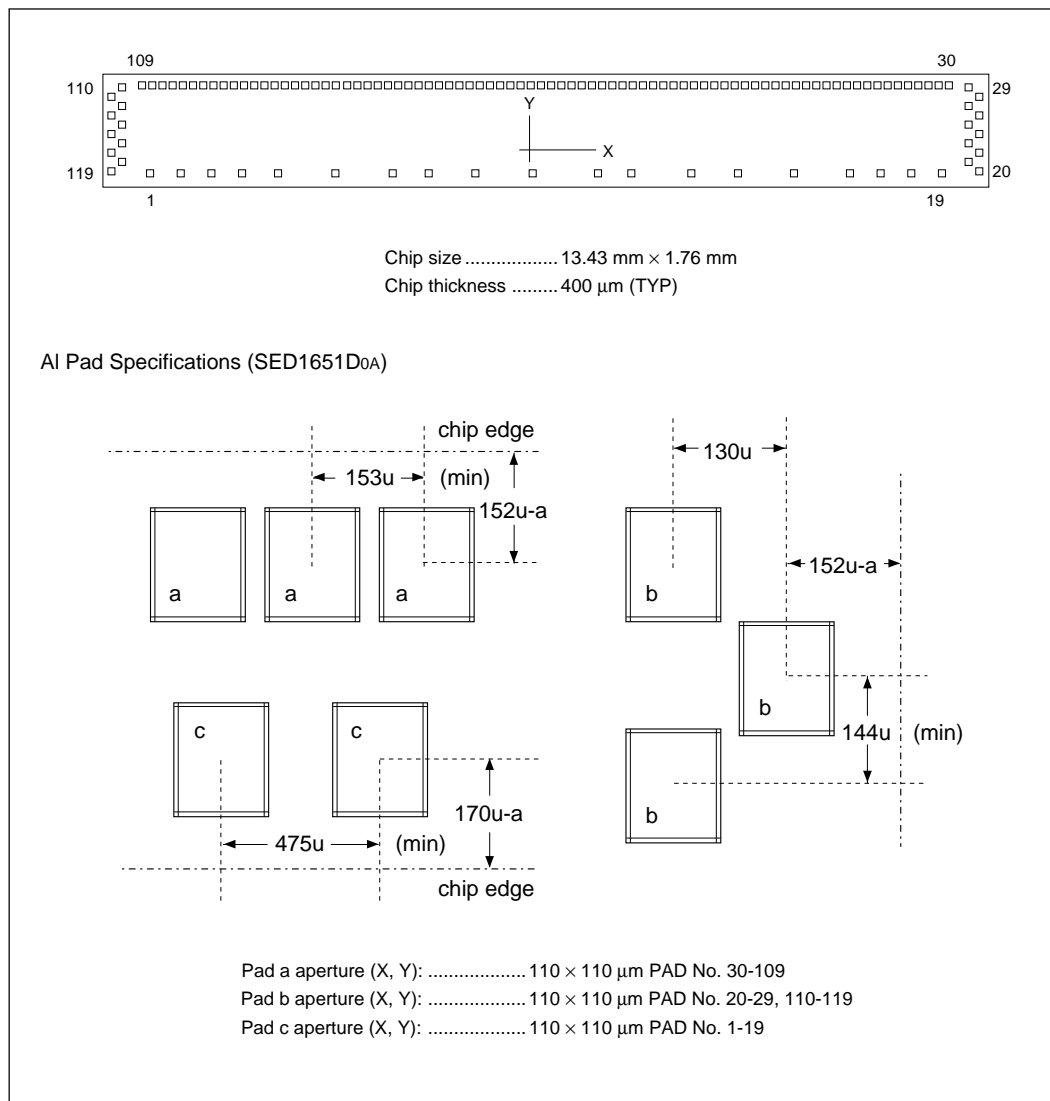


SED1651

- EXAMPLE OF CONNECTION
- Large Screen LCD Structure Diagram



■ PAD LAYOUT



■ PAD COORDINATES

Unit: μm

Pad No.	Pad Name	X Coord.	Y Coord.	Pad No.	Pad Name	X Coord.	Y Coord.	Pad No.	Pad Name	X Coord.	Y Coord.
1	DIO2	-5985	-709	41	O21	4386	727	81	O61	-1770	727
2	V0	-5510	-709	42	O22	4232	727	82	O62	-1924	727
3	V1	-5035	-709	43	O23	4078	727	83	O63	-2078	727
4	V4	-4560	-709	44	O24	3924	727	84	O64	-2232	727
5	V5	-4038	-709	45	O25	3771	727	85	O65	-2385	727
6	Vss	-3164	-709	46	O26	3617	727	86	O66	-2539	727
7	SEL	-2280	-709	47	O27	3463	727	87	O67	-2693	727
8	SHL	-1767	-709	48	O28	3309	727	88	O68	-2847	727
9	DI3	-1064	-709	49	O29	3155	727	89	O69	-3001	727
10	YSCL	-181	-709	50	O30	3001	727	90	O70	-3155	727
11	Vbd	770	-709	51	O31	2847	727	91	O71	-3309	727
12	DSPOFF	1283	-709	52	O32	2693	727	92	O72	-3463	727
13	FR	2176	-709	53	O33	2539	727	93	O73	-3617	727
14	Vss	2879	-709	54	O34	2385	727	94	O74	-3771	727
15	V5	3753	-709	55	O35	2232	727	95	O75	-3924	727
16	V4	4560	-709	56	O36	2078	727	96	O76	-4078	727
17	V1	5035	-709	57	O37	1924	727	97	O77	-4232	727
18	V0	5510	-709	58	O38	1770	727	98	O78	-4386	727
19	DIO1	5985	-709	59	O39	1616	727	99	O79	-4540	727
20	O0	6560	-610	60	O40	1462	727	100	O80	-4694	727
21	O1	6430	-466	61	O41	1308	727	101	O81	-4848	727
22	O2	6560	-321	62	O42	1154	727	102	O82	-5002	727
23	O3	6430	-177	63	O43	1000	727	103	O83	-5156	727
24	O4	6560	-32	64	O44	846	727	104	O84	-5310	727
25	O5	6430	112	65	O45	693	727	105	O85	-5463	727
26	O6	6560	257	66	O46	539	727	106	O86	-5617	727
27	O7	6430	401	67	O47	385	727	107	O87	-5771	727
28	O8	6560	545	68	O48	231	727	108	O88	-5925	727
29	O9	6430	690	69	O49	77	727	109	O89	-6079	727
30	O10	6079	727	70	O50	-77	727	110	O90	-6430	690
31	O11	5925	727	71	O51	-231	727	111	O91	-6560	545
32	O12	5771	727	72	O52	-385	727	112	O92	-6430	401
33	O13	5617	727	73	O53	-539	727	113	O93	-6560	257
34	O14	5463	727	74	O54	-693	727	114	O94	-6430	112
35	O15	5310	727	75	O55	-846	727	115	O95	-6560	-32
36	O16	5156	727	76	O56	-1000	727	116	O96	-6430	-177
37	O17	5002	727	77	O57	-1154	727	117	O97	-6560	-321
38	O18	4848	727	78	O58	-1308	727	118	O98	-6430	-466
39	O19	4694	727	79	O59	-1462	727	119	O99	-6560	-610
40	O20	4540	727	80	O60	-1616	727				