National Semiconductor

ADVANCE INFORMATION

SCAN182952A
Serially Controlled Access Network 18-Bit Registered Transceiver with 25Ω Series Resistor Outputs

General Description

The SCAN182952A is a high performance BiCMOS 18-bit registered transceiver featuring two 18-bit back to back registers that store data flowing in both directions between two bidirectional buses. Each register is organized into dual 9-bit bytes that can be cascaded together for full 18-bit operation. This device is compliant with IEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

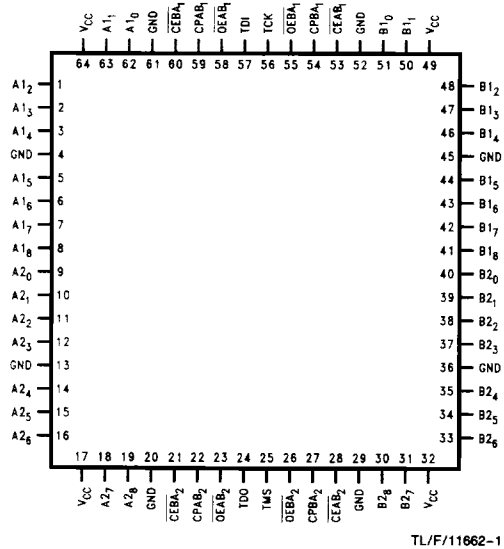
- High performance BiCMOS technology (T_{PD} < 4 ns, typical)
- 25Ω series resistor outputs eliminate the need for external terminating resistors
- Byte wide direction and enable control
- Low noise
- 64-pin PQPF package
- IEEE 1149.1 compliant
- Includes CLAMP, IDCODE and HIGHZ instructions
- Member of National's SCAN™ products

Pin Descriptions

Pin Names	Description
$A1_{(0-8)}$	A1-Register Inputs/B1-Register TRI-STATE Outputs
$B1_{(0-8)}$	B1-Register Inputs/A1-Register TRI-STATE Outputs
$A2_{(0-8)}$	A2-Register Inputs/B2-Register TRI-STATE Outputs
$B2_{(0-8)}$	B2-Register Inputs/A2-Register TRI-STATE Outputs
$\overline{OEAB}_n$	Output Enable AB_n
$CPAB_n$	AB_n-Register Clock
$\overline{CEAB}_n$	AB_n-Register Clock Enable
$\overline{OEBA}_n$	Output Enable BA_n
$CPBA_n$	BA_n-Register Clock
$\overline{CEBA}_n$	BA_n-Register Clock Enable

Connection Diagram

64-Pin PQFP



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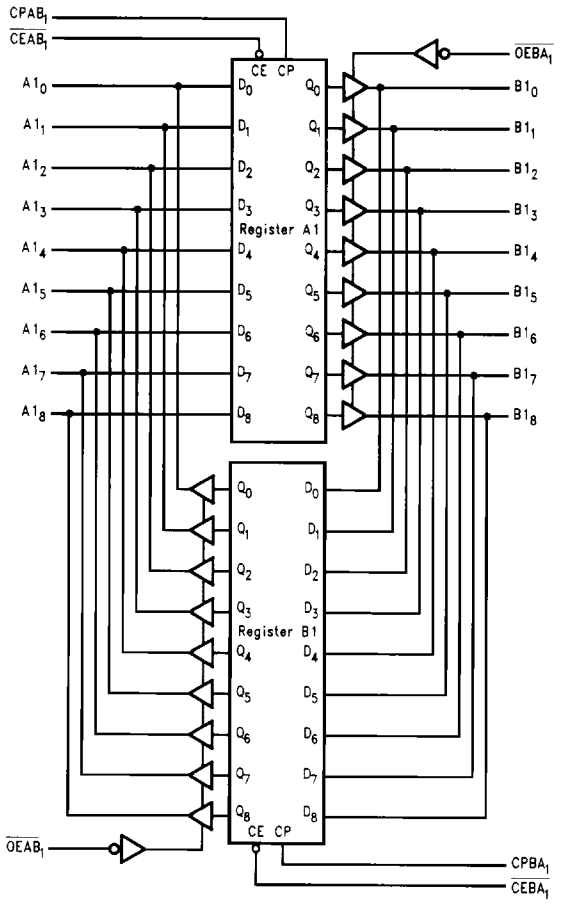
Function Table

Inputs						Data I/O		Operation Mode
$\overline{OEBA}_n$	$\overline{OEAB}_n$	$CPAB_n$	$CPBA_n$	$\overline{CEAB}_n$	$\overline{CEBA}_n$	A1 and A2	B1 and B2	
H	L	H or L	H or L	X	X	Unused	Unused	Isolation
H	L	X	X	H	H	Unused	Unused	Isolation
H	L	↗	H or L	L	X	Input	Unused	Store A_n Data
H	L	↗	X	L	H	Input	Unused	Store A_n Data
H	L	H or L	↗	X	L	Unused	Input	Store B_n Data
H	L	X	↗	H	L	Unused	Input	Store B_n Data
H	L	↗	↗	L	L	Output	Input	Store A_n and B_n Data
L	L	X	X	X	X	Output	Input	Stored B_n to A_n Bus
H	H	X	X	X	X	Input	Output	Stored A_n to B_n Bus

H = HIGH Voltage Level
L = LOW Voltage Level
H/L = High or Low voltage level excluding transitions
X = Don't care
↗ = low to high transition

Logic Diagrams



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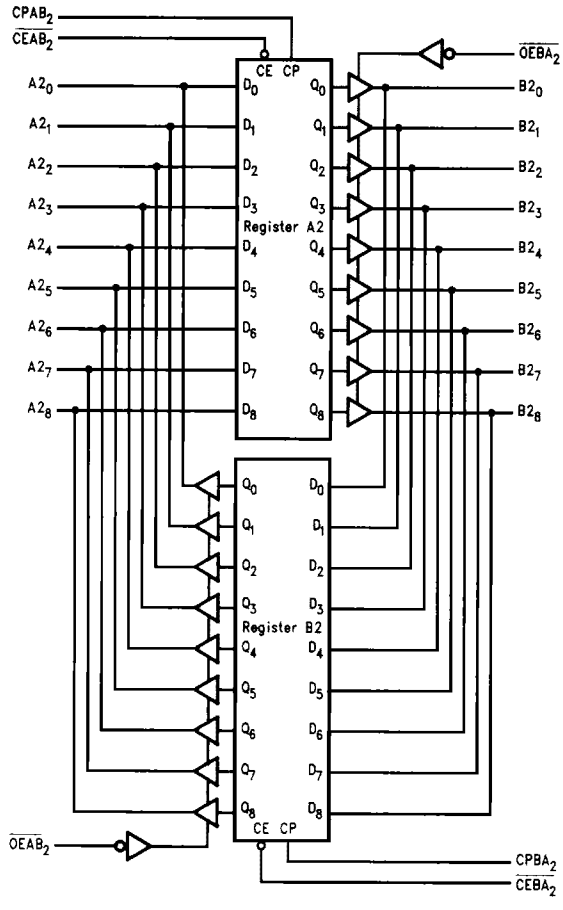
Logic Diagrams (Continued)



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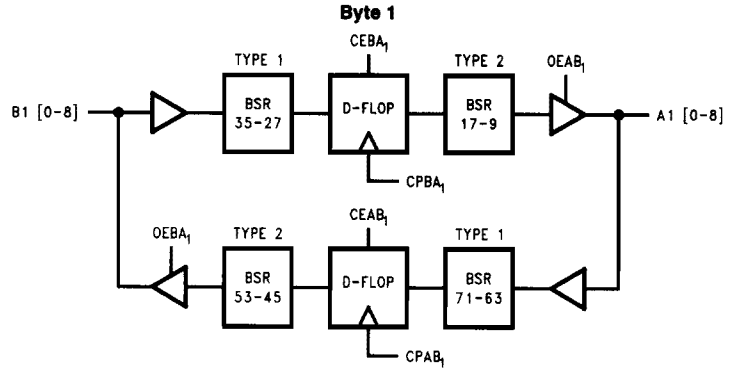
Block Diagrams



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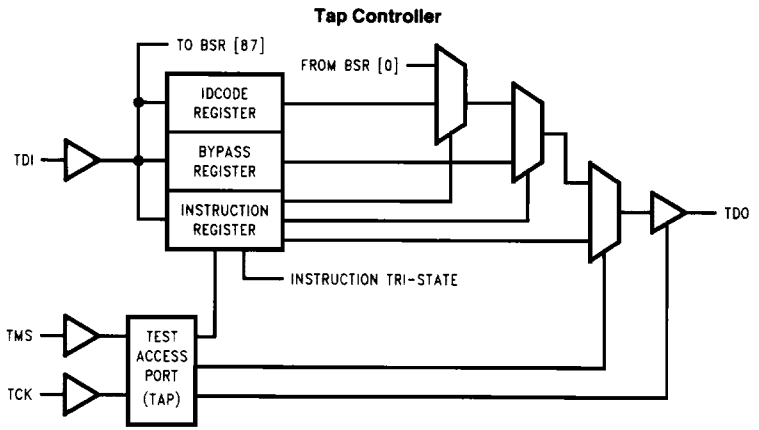

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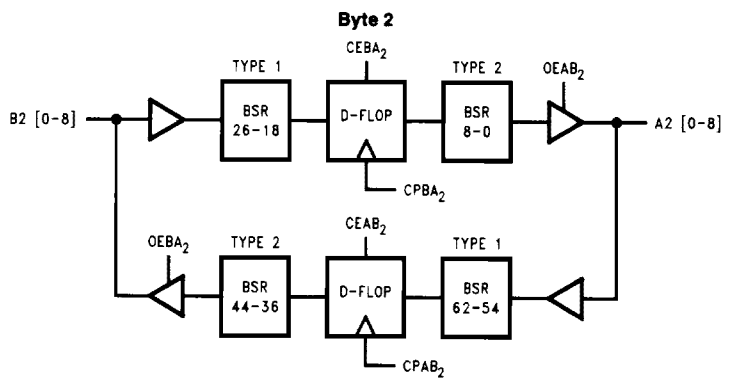

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Note: BSR stands for Boundary Scan Register