

FUJITSU

262144 BIT CMOS STATIC COLUMN DYNAMIC RAM

MB81C258-10
MB81C258-12
MB81C258-15

October 1988
Edition 3.0

262,144 x 1 BIT CMOS STATIC COLUMN DYNAMIC RAM

The Fujitsu MB 81C258 is CMOS static column dynamic random access memory, SC-DRAM, which is organized as 262144 word by 1 bit. This SC-DRAM is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required.

The advantage of SC-DRAM is achieving the static mode operation such as read, write and read-modify-write cycles in spite of dynamic RAM and the fast read and write operation can be performed by this mode.

The MB 81C258 is fabricated using silicon gate CMOS process. Since the CMOS circuit dissipates very small power, it can be easily used in battery backed-up application system such as hand held computer.

The MB 81C258 is pin compatible with HM 51258.

All inputs and outputs are TTL compatible.

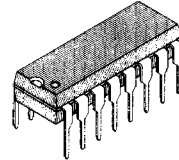
- 262144 x 1 SC-DRAM, 16-pin DIP/18-pin PLCC
- Silicon-gate, CMOS, single transistor cell
- Row Access Time (t_{RAC}),
 - 100 ns max. (MB 81C258-10)
 - 120 ns max. (MB 81C258-12)
 - 150 ns max. (MB 81C258-15)
- Random Cycle Time (t_{RC}),
 - 200 ns min. (MB 81C258-10)
 - 230 ns min. (MB 81C258-12)
 - 260 ns min. (MB 81C258-15)
- Address Access Time (t_{AA}),
 - 45 ns max. (MB 81C258-10)
 - 55 ns max. (MB 81C258-12)
 - 70 ns max. (MB 81C258-15)
- Static Mode Cycle Time (t_{SC}),
 - 50 ns min. (MB 81C258-10)
 - 60 ns min. (MB 81C258-12)
 - 75 ns min. (MB 81C258-15)
- Low Power Dissipation
 - 330 mW max. (MB 81C258-10)
 - 275 mW max. (MB 81C258-12)
 - 248 mW max. (MB 81C258-15)
 - 11 mW max. (TTL level input)
 - 1.65 mW max. (CMOS level input)
- Single 5V supply, $\pm 10\%$ tolerance
- 32 ms/256 refresh cycles
- \overline{RAS} -Only, \overline{CAS} -before- \overline{RAS} , and Hidden refresh capability
- Standard 16-pin Plastic DIP (Suffix: -P)
- Standard 18-pin Plastic LCC (Suffix: -PD)

ABSOLUTE MAXIMUM RATINGS

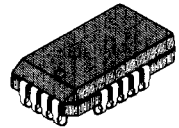
| Rating | Symbol | Value | Unit |
|--|-------------------|-------------|-------------|
| Voltage on any pin relative to V_{SS} | V_{IN}, V_{OUT} | -1 to +7 | V |
| Voltage on V_{CC} relative to V_{SS} | V_{CC} | -1 to +7 | V |
| Storage Temperature | T_{STG} | -55 to +125 | $^{\circ}C$ |
| Power Dissipation | P_D | 1.0 | W |
| Short Circuit output current | | 50 | mA |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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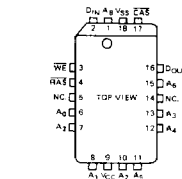
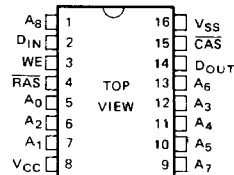


**PLASTIC PACKAGE
DIP-16P-M03**

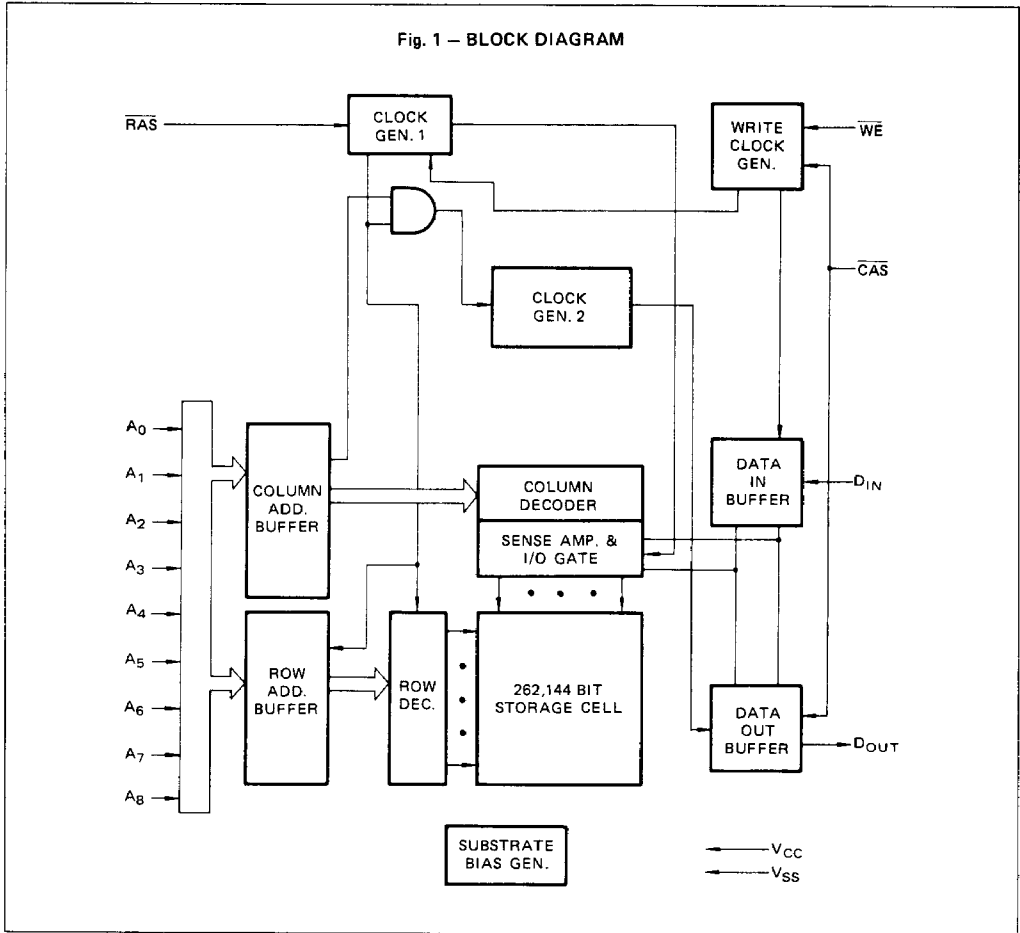


**PLASTIC PACKAGE
LCC-18P-M04**

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Parameter | Symbol | Typ | Max | Unit |
|---|------------------|-----|-----|------|
| Input Capacitance, A ₀ to A ₈ and D _{IN} | C _{IN1} | — | 7 | pF |
| Input Capacitance, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, WE | C _{IN2} | — | 10 | pF |
| Output Capacitance, D _{OUT} | C _{OUT} | — | 7 | pF |

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

| Parameter | Symbol | Min | Typ | Max | Unit | Operating Temperature |
|--------------------------------|----------------------|----------|----------|----------|------|-----------------------|
| Supply Voltage | V_{CC} V_{SS} | 4.5 0 | 5.0 0 | 5.5 0 | V | 0°C to +70°C |
| Input High Voltage, all inputs | V_{IH} | 2.4 | — | 6.5 | V | |
| Input Low Voltage, all inputs | V_{IL} | -1.0 | — | 0.8 | V | |

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DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

| Parameter | | Conditions | Symbol | Values | | Unit |
|---|-------------|--|------------|--------|-----|---------|
| | | | | Min | Max | |
| Operating Current* (Average power supply current) | MB81C258-10 | $\overline{CAS} = V_{IL}$ or V_{IH} , RAS cycling; $t_{RC} = \text{min}$ | I_{CC1} | — | 60 | mA |
| | MB81C258-12 | | | — | 50 | |
| | MB81C258-15 | | | — | 45 | |
| Standby Current (Power supply current) | TTL level | $\overline{RAS} = \overline{CAS} = V_{IH}$ | I_{CC2} | — | 2.0 | mA |
| | CMOS level | $\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2V$ | | — | 0.3 | |
| Static Mode Current* | MB81C258-10 | $\overline{RAS} = \overline{CAS} = V_{IL}$, RAS cycling; $t_{SC} = \text{min}$. | I_{CC3} | — | 40 | mA |
| | MB81C258-12 | | | — | 35 | |
| | MB81C258-15 | | | — | 30 | |
| \overline{CAS} -before- \overline{RAS} Refresh Current* (Average power current) | MB81C258-10 | \overline{RAS} cycling, \overline{CAS} -before- \overline{RAS} ; $t_{RC} = \text{min}$ | I_{CC4} | — | 55 | mA |
| | MB81C258-12 | | | — | 45 | |
| | MB81C258-15 | | | — | 40 | |
| Input Leakage Current | | $0V \leq V_{IN} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$; pins not under test = 0V | $I_{I(L)}$ | -10 | 10 | μA |
| Output Leakage Current | | $0V \leq V_{OUT} \leq 5.5V$; Data out disabled | $I_{O(L)}$ | -10 | 10 | |
| Output High Voltage | | $I_{OH} = -5mA$ | V_{OH} | 2.4 | — | V |
| Output Low Voltage | | $I_{OL} = 4.2mA$ | V_{OL} | — | 0.4 | |

NOTE: *: I_{CC} depends on the output load operating speed. The specified values are with the output pin open.

AC CHARACTERISTICS

(At Recommended operating conditions unless otherwise noted) **Notes 1, 2**

| Parameter | NOTES | Symbol | MB 81C258-10 | | MB 81C258-12 | | MB 81C258-15 | | Unit |
|---|------------|-----------|--------------|--------|--------------|--------|--------------|--------|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Time Between Refresh | | t_{REF} | — | 32 | — | 32 | — | 32 | ms |
| Random Read/Write Cycle Time | | t_{RC} | 200 | — | 230 | — | 260 | — | ns |
| Read-Modify-Write Cycle Time | | t_{RWC} | 245 | — | 285 | — | 325 | — | ns |
| Access Time from \overline{RAS} | 3 5 | t_{RAC} | — | 100 | — | 120 | — | 150 | ns |
| Access Time from \overline{CAS} | | t_{CAC} | — | 25 | — | 30 | — | 35 | ns |
| Output Buffer Turn off Delay Time | | t_{OFF} | 0 | 25 | 0 | 25 | 0 | 30 | ns |
| Transition Time | | t_T | 3 | 50 | 3 | 50 | 3 | 50 | ns |
| Column Address Access Time | 4 5 | t_{AA} | — | 45 | — | 55 | — | 70 | ns |
| Output Hold Time from Column Address Change | | t_{AOH} | 5 | — | 5 | — | 5 | — | ns |
| Access Time from \overline{WE} Precharge | | t_{WPA} | — | 25 | — | 30 | — | 35 | ns |
| Access Time Relative to last Write | 6 | t_{ALW} | — | 90 | — | 110 | — | 140 | ns |
| Write Latched Data Hold Time | | t_{WOH} | 0 | — | 0 | — | 0 | — | ns |
| \overline{RAS} Precharge Time | | t_{RP} | 90 | — | 100 | — | 100 | — | ns |
| \overline{RAS} Pulse Width | | t_{RAS} | 65 | 100000 | 75 | 100000 | 95 | 100000 | ns |
| \overline{RAS} Hold Time | | t_{RSH} | 25 | — | 30 | — | 35 | — | ns |
| \overline{CAS} Pulse Width (Read) | | t_{CAS} | 25 | 100000 | 30 | 100000 | 35 | 100000 | ns |
| \overline{CAS} Pulse Width (Write) | | t_{CAS} | 15 | 100000 | 20 | 100000 | 25 | 100000 | ns |
| \overline{CAS} Hold Time (Read) | | t_{CSH} | 100 | — | 120 | — | 150 | — | ns |
| \overline{CAS} Hold Time (Write) | | t_{CSH} | 80 | — | 95 | — | 115 | — | ns |
| \overline{RAS} to \overline{CAS} Delay Time | | t_{RCD} | 25 | 75 | 25 | 90 | 30 | 115 | ns |
| \overline{CAS} to \overline{RAS} Set Up Time | | t_{CRS} | 20 | — | 25 | — | 30 | — | ns |
| Row Address Set Up Time | | t_{ASR} | 0 | — | 0 | — | 0 | — | ns |
| Row Address Hold Time | | t_{RAH} | 15 | — | 15 | — | 20 | — | ns |
| Column Address Set Up Time | 7 | t_{ASC} | 0 | — | 0 | — | 0 | — | ns |
| Column Address Hold Time | 7 | t_{CAH} | 20 | — | 25 | — | 30 | — | ns |
| \overline{RAS} to Column Address Delay Time | 8 9 | t_{RAD} | 20 | 55 | 20 | 65 | 25 | 80 | ns |
| Column Address Hold Time Referenced to \overline{RAS} | | t_{AR} | 100 | — | 120 | — | 150 | — | ns |
| Write Address Hold Time Referenced to \overline{RAS} | | t_{AWR} | 80 | — | 90 | — | 110 | — | ns |
| Read Address to \overline{RAS} Lead Time | | t_{RAL} | 45 | — | 55 | — | 70 | — | ns |
| Column Address Hold Time Referenced to \overline{RAS} Rising Time | 10 | t_{AHR} | 15 | — | 15 | — | 20 | — | ns |



AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) **Notes 1, 2**

| Parameter | NOTES | Symbol | MB 81C258-10 | | MB 81C258-12 | | MB 81C258-15 | | Unit |
|---|-------|------------|--------------|-----|--------------|-----|--------------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Last Write to Column Address Delay Time | 11 12 | t_{LWAD} | 20 | 45 | 20 | 55 | 25 | 70 | ns |
| Column Address Hold Time Referenced to Last Write | | t_{AHLW} | 90 | — | 110 | — | 140 | — | ns |
| Read Command Set Up Time Referenced to \overline{CAS} | | t_{RCS} | 0 | — | 0 | — | 0 | — | ns |
| Read Command Hold Time Referenced to \overline{RAS} | 13 | t_{RRH} | 10 | — | 10 | — | 10 | — | ns |
| Read Command Hold Time Referenced to \overline{CAS} | 13 | t_{RCH} | 0 | — | 0 | — | 0 | — | ns |
| \overline{WE} Pulse Width | | t_{WP} | 15 | — | 20 | — | 25 | — | ns |
| \overline{WE} Inactive Time | | t_{WI} | 15 | — | 20 | — | 25 | — | ns |
| Write Command Hold Time | | t_{WCH} | 15 | — | 20 | — | 25 | — | ns |
| Write Command to \overline{RAS} Lead Time | | t_{RWL} | 25 | — | 30 | — | 35 | — | ns |
| Write Command to \overline{CAS} Lead Time | | t_{CWL} | 25 | — | 30 | — | 35 | — | ns |
| \overline{RAS} to \overline{WE} Delay Time | 14 | t_{RWD} | 100 | — | 120 | — | 150 | — | ns |
| \overline{CAS} to \overline{WE} Delay Time | | t_{CWD} | 25 | — | 30 | — | 35 | — | ns |
| Column Address to \overline{WE} Delay Time | | t_{AWD} | 45 | — | 55 | — | 70 | — | ns |
| \overline{RAS} to Second Write Delay Time | | t_{RSWD} | 105 | — | 125 | — | 155 | — | ns |
| Write Command Hold Time Referenced to \overline{RAS} | | t_{WCR} | 80 | — | 95 | — | 115 | — | ns |
| \overline{RAS} Precharge Time from Last Write | | t_{RPLW} | 135 | — | 155 | — | 165 | — | ns |
| Write Set Up Time for Output Disable | 14 | t_{WS} | 0 | — | 0 | — | 0 | — | ns |
| Write Hold Time for Output Disable | 14 | t_{WH} | 0 | — | 0 | — | 0 | — | ns |
| D_{IN} Set Up Time | | t_{DS} | 0 | — | 0 | — | 0 | — | ns |
| D_{IN} Hold Time | | t_{DH} | 20 | — | 25 | — | 30 | — | ns |
| D_{IN} Hold Time Reference to \overline{RAS} | | t_{DHR} | 80 | — | 90 | — | 110 | — | ns |
| Refresh Set Up Time for \overline{CAS} Referenced to \overline{RAS} (\overline{CAS} -before- \overline{RAS} cycle) | | t_{FCS} | 20 | — | 25 | — | 30 | — | ns |

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AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) **Notes 1, 2**

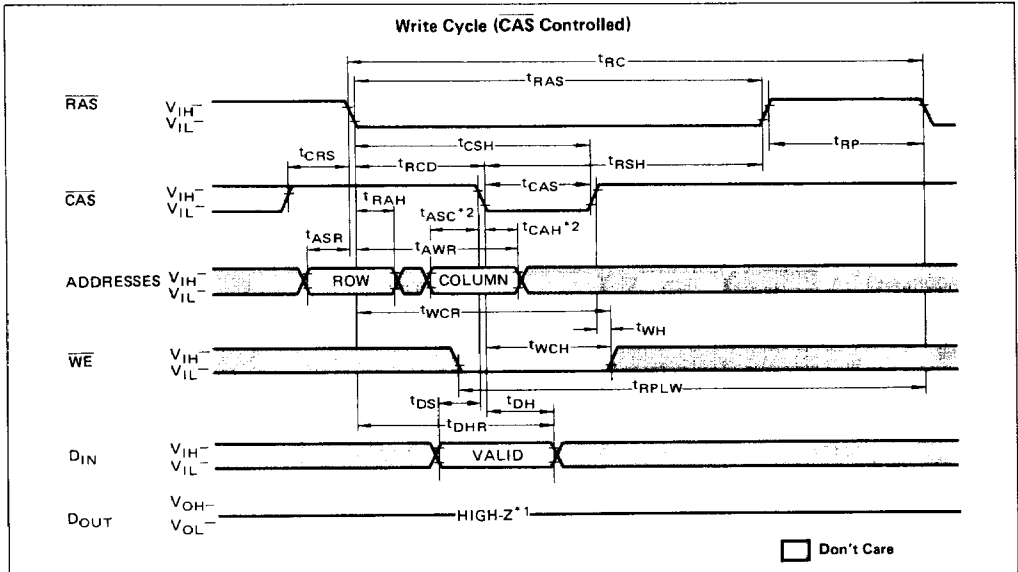
| Parameter | NOTES | Symbol | MB 81C258-10 | | MB 81C258-12 | | MB 81C258-15 | | Unit |
|--|-----------|-------------------|--------------|-------|--------------|-------|--------------|-------|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Refresh Hold Time for $\overline{\text{CAS}}$ Referenced to RAS (CAS-before-RAS cycle) | | t_{FCH} | 20 | — | 25 | — | 30 | — | ns |
| $\overline{\text{CAS}}$ Precharge Time (CAS-before-RAS cycle) | | t_{CPR} | 20 | — | 25 | — | 30 | — | ns |
| RAS Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh cycles) | | t_{RPC} | 20 | — | 20 | — | 20 | — | ns |
| Static Mode Read/Write Cycle Time | | t_{SC} | 50 | — | 60 | — | 75 | — | ns |
| Static Mode Read-Modify-Write Cycle Time | | t_{SRWC} | 95 | — | 115 | — | 145 | — | ns |
| Static Mode $\overline{\text{CAS}}$ Precharge Time | | t_{CP} | 15 | — | 20 | — | 25 | — | ns |
| Refresh Counter Test Cycle Time | 15 | t_{RTC} | 440 | — | 520 | — | 610 | — | ns |
| Refresh Counter Test RAS Pulse Width | 15 | t_{TRAS} | 340 | 10000 | 410 | 10000 | 500 | 10000 | ns |
| Refresh Counter Test $\overline{\text{CAS}}$ Precharge Time | 15 | t_{CPT} | 50 | — | 60 | — | 70 | — | ns |
| Refresh Counter Test $\overline{\text{CAS}}$ to Col. Address Delay Time | 15 | t_{CADT} | — | 100 | — | 120 | — | 150 | ns |
| Refresh Counter Test Access Time from $\overline{\text{CAS}}$ | 15 | t_{CACT} | — | 135 | — | 165 | — | 205 | ns |
| Refresh Counter Test $\overline{\text{CAS}}$ to WE Delay Time | 15 | t_{CWDT} | 135 | — | 165 | — | 205 | — | ns |

NOTES:

- An Initial pause ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{IH}}$) of 200 μs is required after power-up followed by any 8 RAS-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- AC characteristics assume $t_{\text{T}} = 5\text{ns}$, $V_{\text{IN}} = 0\text{V}$ to 3V, $V_{\text{IH}} = 2.4\text{V}$, $V_{\text{IL}} = 0.8\text{V}$, $V_{\text{OH}} = 2.4\text{V}$, and $V_{\text{OL}} = 0.4\text{V}$.
- Assumes that $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.
- Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Assumes that $t_{\text{LWAD}} \leq t_{\text{LWAD}}(\text{max})$. If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
- Write Cycle Only.
- Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only;

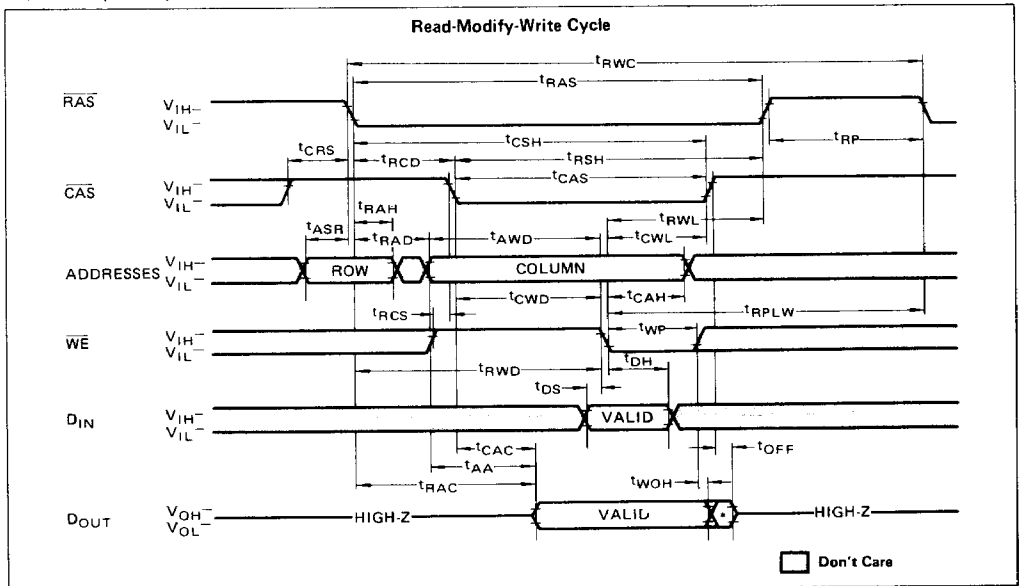
if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .

- $t_{\text{RAD}}(\text{min}) = t_{\text{RAH}}(\text{min}) + t_{\text{T}} (t_{\text{T}} = 5\text{ns})$
- t_{AHR} is specified to latch column address by the rising edge of RAS.
- Operation within the $t_{\text{LWAD}}(\text{max})$ limit insures that $t_{\text{ALW}}(\text{max})$ can be met. $t_{\text{LWAD}}(\text{max})$ is specified as a reference point only; if t_{LWAD} is greater than the specified $t_{\text{LWAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
- $t_{\text{LWAD}}(\text{min}) = t_{\text{CAH}}(\text{min}) + t_{\text{T}} (t_{\text{T}} = 5\text{ns})$.
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- t_{WS} , t_{WH} , and t_{WD} are specified as a reference point only. If $t_{\text{WS}} \geq t_{\text{WS}}(\text{min})$ and $t_{\text{WH}} \geq t_{\text{WH}}(\text{min})$, the data output pin will remain High-Z state throughout entire cycle. If $t_{\text{WD}} \geq t_{\text{RWD}}(\text{min})$, The data output will contain data read from the selected cell.
- CAS-before-RAS refresh counter test cycle only.

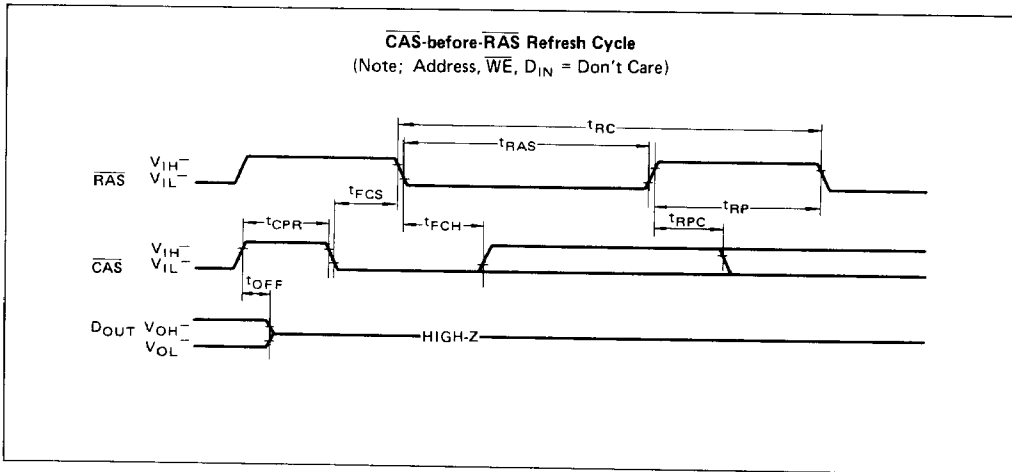
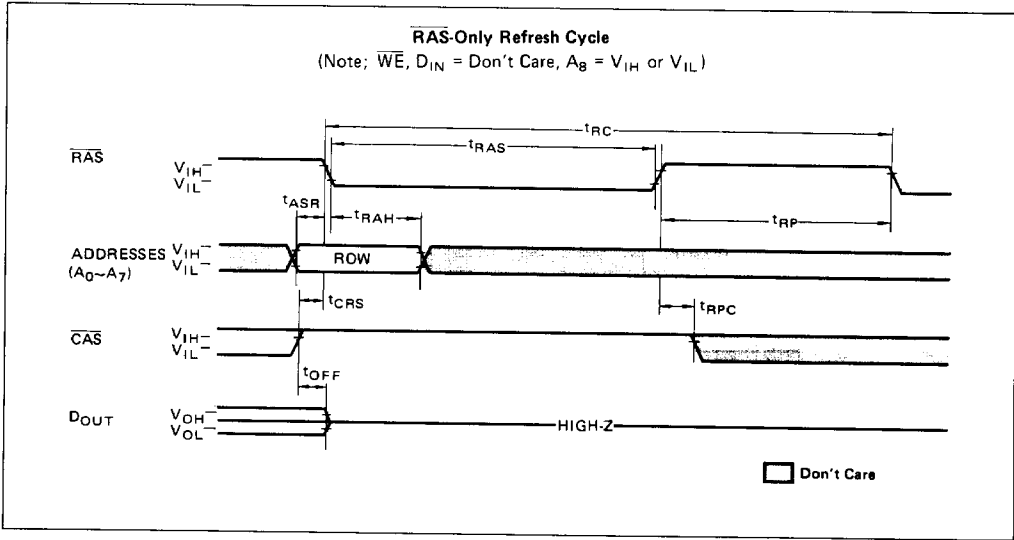


*1: If $t_{WS} \geq t_{WS}(\text{min})$ and $t_{WH} \geq t_{WH}(\text{min})$, D_{OUT} is high-Z.

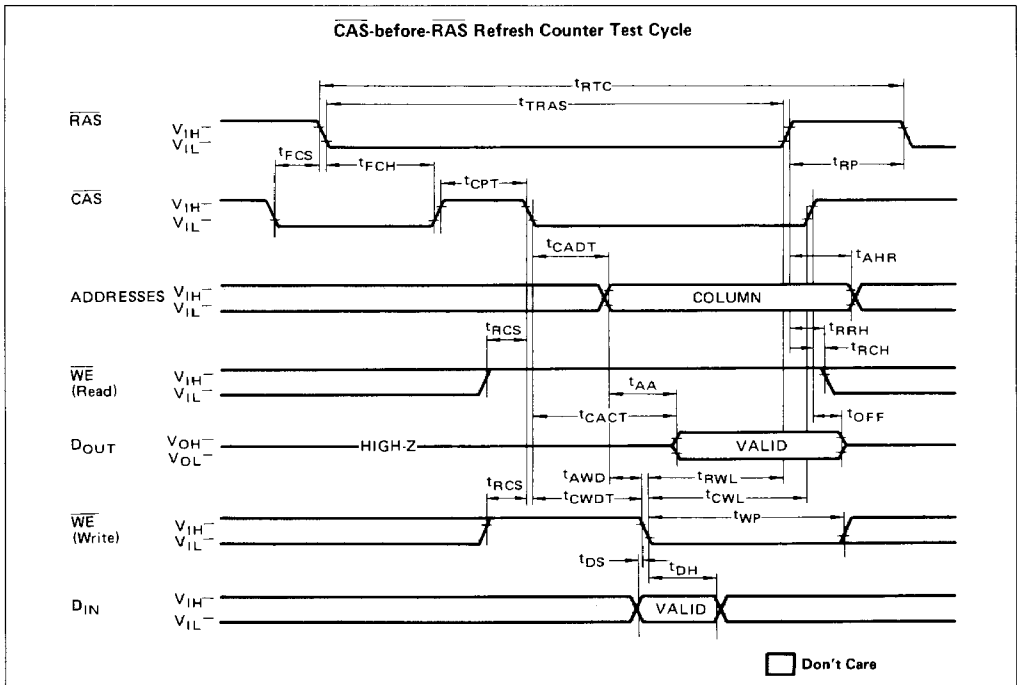
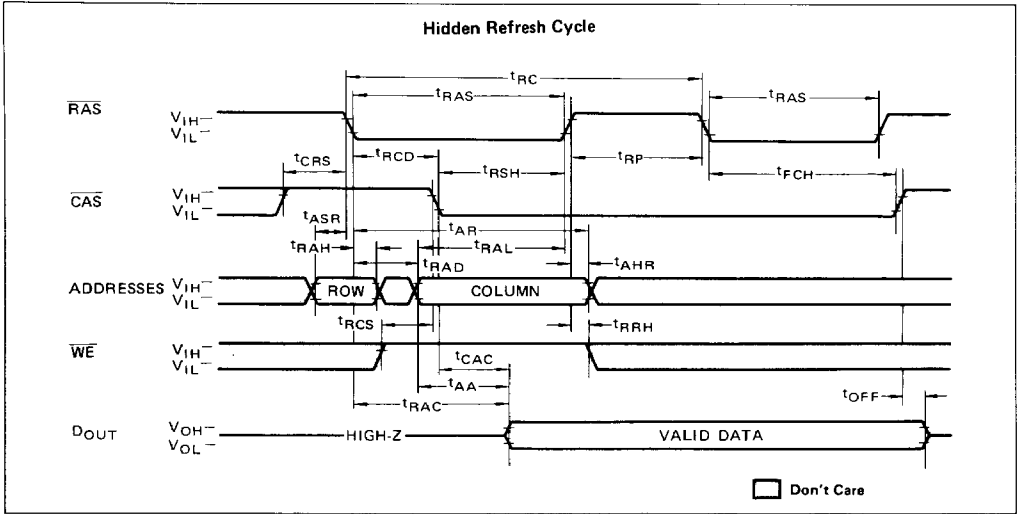
*2: Write Cycle only.



*: Invalid Data



2





DESCRIPTION

Address Inputs:

A total of eighteen binary input address bits are required to decode any one of the 262,144 storage cells within the MB 81C258. Nine row address bits are established on the address input pins (A_0 to A_8) and latched with the Row Address Strobe (\overline{RAS}). The nine column address bits are established on the address input pins (A_9 to A_{17}) after the Row Address Hold Time has been satisfied. In read cycle, the column address are not latched by the Column Address Strobe (\overline{CAS}), so the column address must be stable until the output becomes valid. In write cycle, the column addresses are latched by the later falling edge of \overline{CAS} or \overline{WE} .

Write Enable:

Read or Write cycle is selected with the \overline{WE} inputs. A high on \overline{WE} selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of \overline{CAS} or \overline{WE} (Both \overline{CAS} and \overline{WE} are low). The time period of the write operation is determined by internal circuit, thus next write operation will be inhibited during the write operation.

Data Input:

Data is written into the MB 81C258 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of \overline{CAS} or \overline{WE} .

Data Output:

The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same polarity as data in. The output is in high impedance state until \overline{CAS} is brought low. In a read cycle, the access time is determined by the following conditions:

1. t_{RAC} from the falling edge of \overline{RAS} .
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of \overline{CAS} .

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC} = t_{RCD} + t_{CAC}$ or $t_{RAC} = t_{RAD} + t_{AA}$.

Data output remains valid while the column address inputs are kept constant. However, when \overline{CAS} goes high, the output returns to high impedance state. In the static mode, the output

data is internally latched by the later falling edge of \overline{CAS} or \overline{WE} and remains valid internally until either returns to high.

Static Mode:

The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, \overline{CAS} can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.

1. Static mode read cycle;
 In a static mode read cycle, the access time is t_{RAC} from the falling edge of \overline{RAS} or t_{AA} from the column address input. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle,
 In a static mode write cycle, the data is written into the cell triggered by the later falling edge of \overline{CAS} or \overline{WE} . If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle.
3. Static mode read-modify-write cycle;
 In the static mode read-modify-write cycle, \overline{WE} goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of \overline{CAS} . The data and column address inputs are strobed and latched by the falling edge of \overline{WE} .
4. Static mode mixed cycle,
 In the static mode, read, write, and read-modify-write cycles can be mixed in any order.
 In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions:
 1. t_{ALW} from the falling edge of \overline{WE} at previous write cycle.
 2. t_{AA} from the column address inputs.
 3. t_{WPA} from the rising edge of \overline{WE} at the read cycle.
 4. t_{CAC} from the falling edge of \overline{CAS} .

Refresh:

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 4ms.

The MB 81C258 offers the following three types of refresh.

1. \overline{RAS} only refresh;
 The \overline{RAS} -only refresh avoids any output during refresh because the output buffer is high impedance state due to \overline{CAS} high. Strobing of each 256 row address (A_0 to A_7) with \overline{RAS} will cause all bits in each row to be refreshed. During \overline{RAS} -only refresh cycle, (either V_{IH} or V_{IL}) is permitted to A_8 .
2. \overline{CAS} -before- \overline{RAS} refresh;
 \overline{CAS} -before- \overline{RAS} refreshing available on the MB 81C258 offers an alternate refresh method. If \overline{CAS} is held low for the specified period (t_{FCS}) before \overline{RAS} goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next \overline{CAS} -before- \overline{RAS} refresh.
3. Hidden refresh;
 A hidden refresh cycle will be executed while maintaining latest valid data at the output pin by extending the \overline{CAS} low time. For the MB 81C258, a hidden refresh cycle is \overline{CAS} -before- \overline{RAS} refresh. The internal refresh address counter provides the refresh address, as in a normal \overline{CAS} -before- \overline{RAS} refresh cycle.

\overline{CAS} -before- \overline{RAS} refresh counter Test:

A special timing sequence using \overline{CAS} -before- \overline{RAS} refresh counter test cycle provides a convenient method of verifying the function of \overline{CAS} -before- \overline{RAS} refresh activated circuitry. After the \overline{CAS} -before- \overline{RAS} refresh cycle, if \overline{CAS} goes to high and goes to low again while \overline{RAS} is held low, the read and read-modify-write cycles are enabled according to the state of \overline{WE} . This is shown in the \overline{CAS} -before- \overline{RAS} counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed is shown below.

ROW ADDRESS — Bits A_0 to A_7 are provided by the refresh counter. The

bits A_8 is set high internally.
COLUMN ADDRESS – All the bits A_0 to A_8 are provided by externally after t_{CADT} .
 The recommended procedure of \overline{CAS} -before- \overline{RAS} refresh counter test cycle is shown below. The timing of \overline{CAS} -before- \overline{RAS} refresh counter test cycle should be used.

- 1) Initialize the internal refresh address

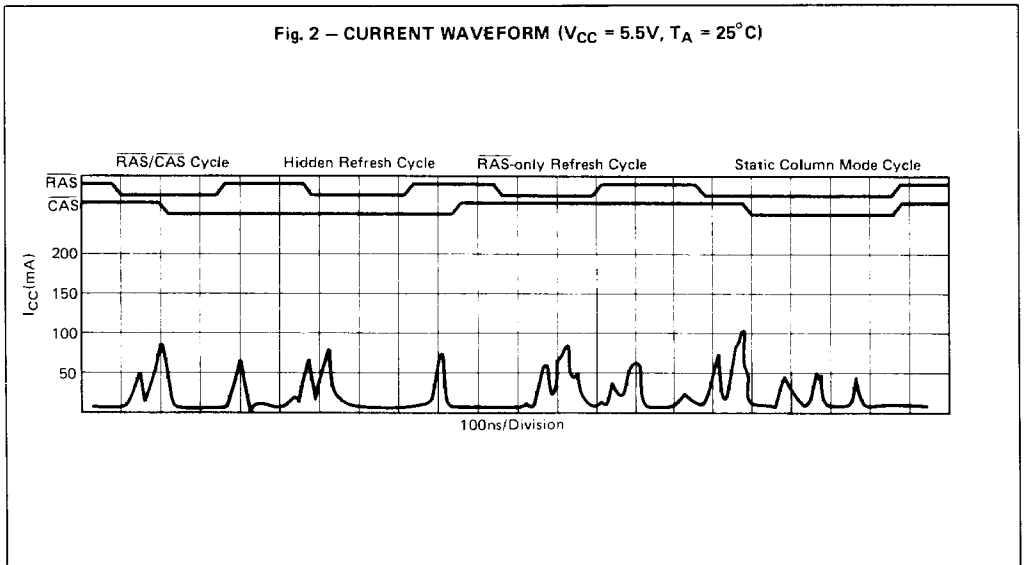
counter by using eight \overline{CAS} -before- \overline{RAS} refresh cycles.

- 2) Throughout the test, use the same column address.
- 3) Using a write cycle, write 0s to all 256 row addresses.
- 4) Using \overline{CAS} -before- \overline{RAS} refresh counter test cycle in read-modify-write mode, read the 0 written in step 3), and simultaneously write a 1

to the same cell. This step is repeated 256 row address generated by internal refresh address counter.

- 5) Using a normal read cycle, read back the 1s written in step 4), from all 256 locations.
- 6) Complement the test pattern and repeat step 3), 4), and 5).

Fig. 2 – CURRENT WAVEFORM ($V_{CC} = 5.5V, T_A = 25^\circ C$)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME (t_{RAC}) vs SUPPLY VOLTAGE

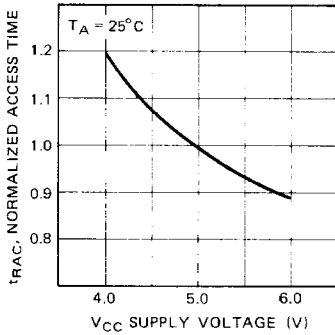


Fig. 4 – NORMALIZED ACCESS TIME (t_{RAC}) vs AMBIENT TEMPERATURE

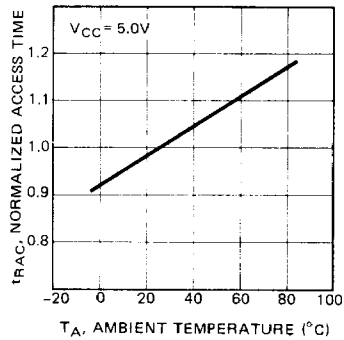


Fig. 5 – NORMALIZED ACCESS TIME (t_{AA}) vs SUPPLY VOLTAGE

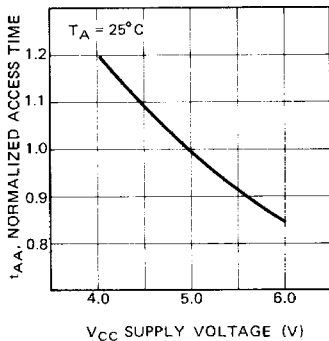


Fig. 6 – NORMALIZED ACCESS TIME (t_{AA}) vs AMBIENT TEMPERATURE

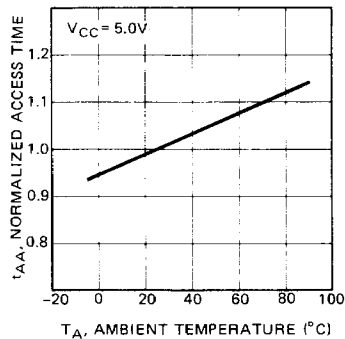


Fig. 7 – OPERATING CURRENT vs CYCLE RATE

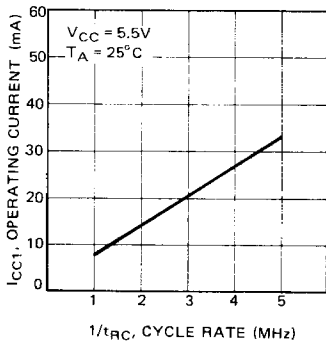
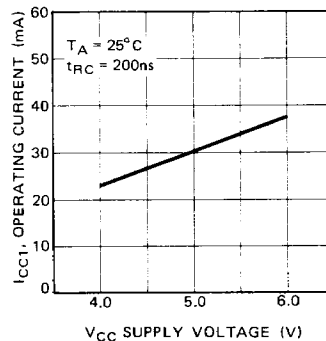


Fig. 8 – OPERATING CURRENT vs SUPPLY VOLTAGE





MB81C258-10
MB81C258-12
MB81C258-15

2

Fig. 9 – OPERATING CURRENT vs AMBIENT TEMPERATURE

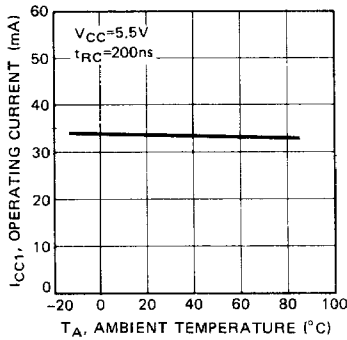


Fig. 10 – TTL STANDBY CURRENT vs SUPPLY VOLTAGE

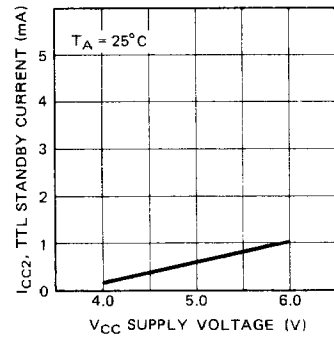


Fig. 11 – CMOS STANDBY CURRENT vs SUPPLY VOLTAGE

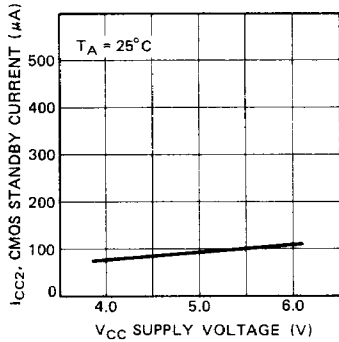


Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

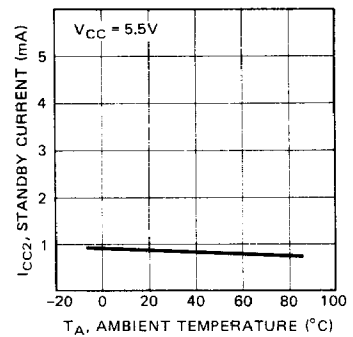


Fig. 13 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

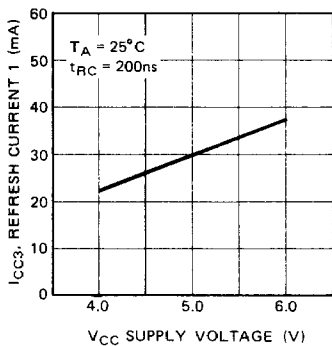


Fig. 14 – REFRESH CURRENT 1 vs CYCLE RATE

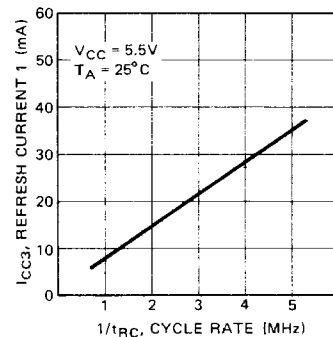


Fig. 15 – STATIC COLUMN MODE CURRENT vs CYCLE RATE

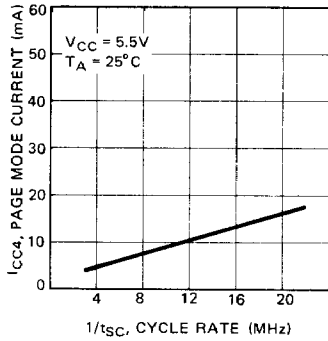


Fig. 16 – STATIC COLUMN MODE CURRENT vs SUPPLY VOLTAGE

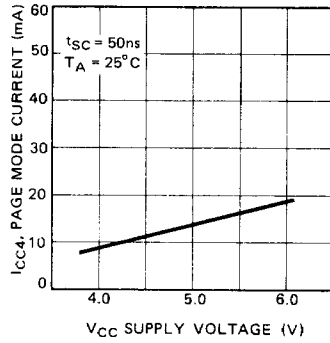


Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

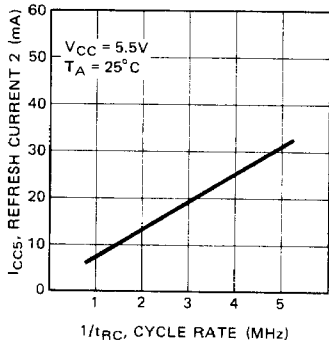


Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

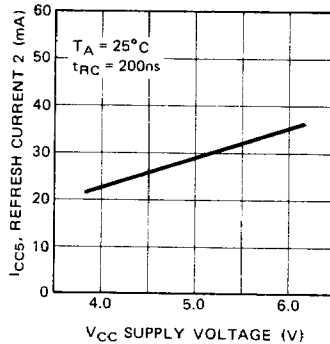


Fig. 19 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

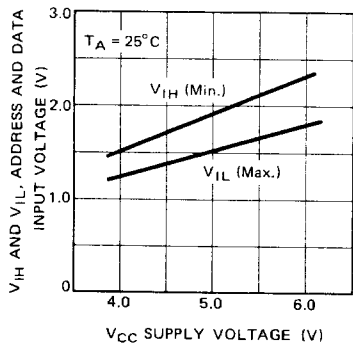


Fig. 20 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

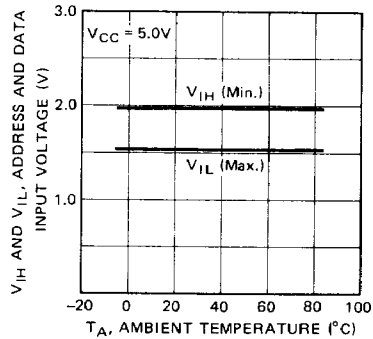




Fig. 21 – $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ AND $\overline{\text{WE}}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

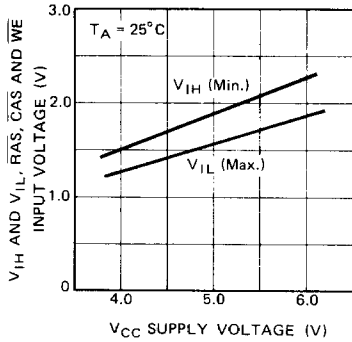


Fig. 22 – $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ AND $\overline{\text{WE}}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

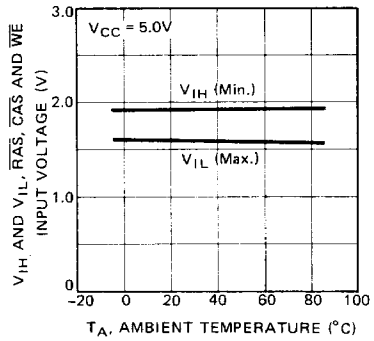


Fig. 23 – ACCESS TIME (t_{RAC}) vs LOAD CAPACITANCE

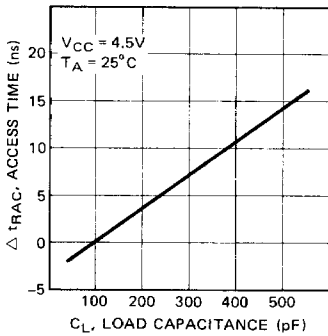


Fig. 24 – ACCESS TIME (t_{AA}) vs LOAD CAPACITANCE

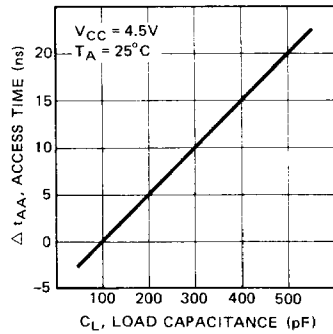


Fig. 25 – OUTPUT CURRENT vs OUTPUT VOLTAGE

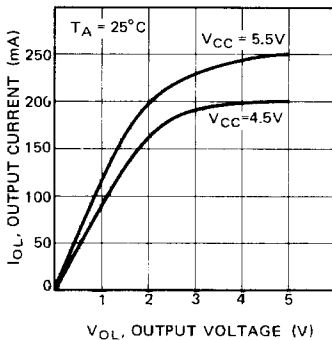


Fig. 26 – OUTPUT CURRENT vs OUTPUT VOLTAGE

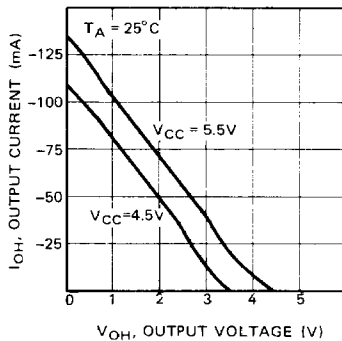


Fig. 27 – CURRENT WAVEFORM DURING POWER UP (1)

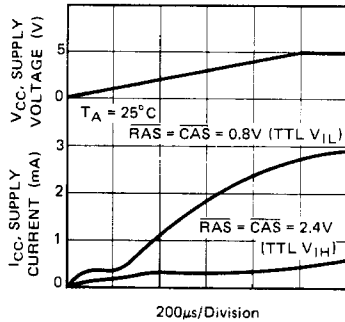
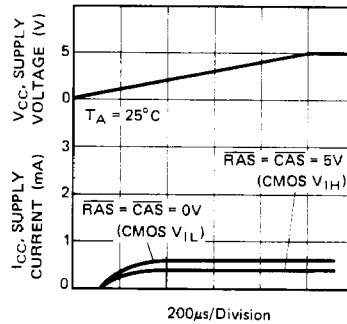


Fig. 28 – CURRENT WAVEFORM DURING POWER UP (2)



2

FUNCTIONAL TRUTH TABLE

| Operation Mode | Clock Input | | | Address Input | | Data | |
|---|-------------------------|-------------------------|------------------------|---------------------|--------|-------|----------------------|
| | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Row | Column | Input | Output |
| Standby | H | H | X | X | X | X | High-Z |
| Read Cycle | L | L | H | Valid | Valid | X | Valid |
| Write Cycle | L | L | L | Valid | Valid | Valid | High-Z* ¹ |
| Static Mode Read Cycle | L | L | H | Valid* ² | Valid | X | Valid |
| Static Mode Write Cycle | L | L | L | Valid* ² | Valid | Valid | High-Z* ¹ |
| Static Mode Mixed Cycle | L | L | L/H | Valid* ² | Valid | Valid | High-Z or Valid |
| $\overline{\text{RAS}}$ -only Refresh Cycle | L | H | X | Valid | X | X | High-Z |

X: Don't Care H: High level L: Low level

Note: *1: If $t_{\text{WS}} < t_{\text{WS}(\text{min})}$ and $t_{\text{WH}} < t_{\text{WH}(\text{min})}$, the data output become invalid.

*2: After first cycle, row address is not necessary.

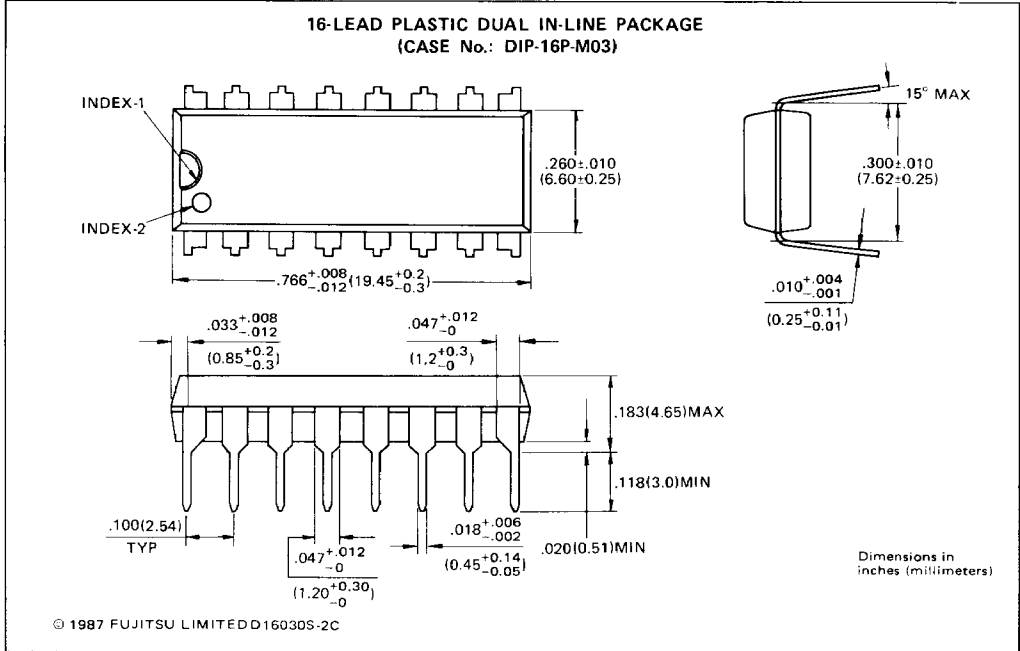


MB 81C258-10
FUJITSU MB 81C258-12
MB 81C258-15

PACKAGE DIMENSIONS

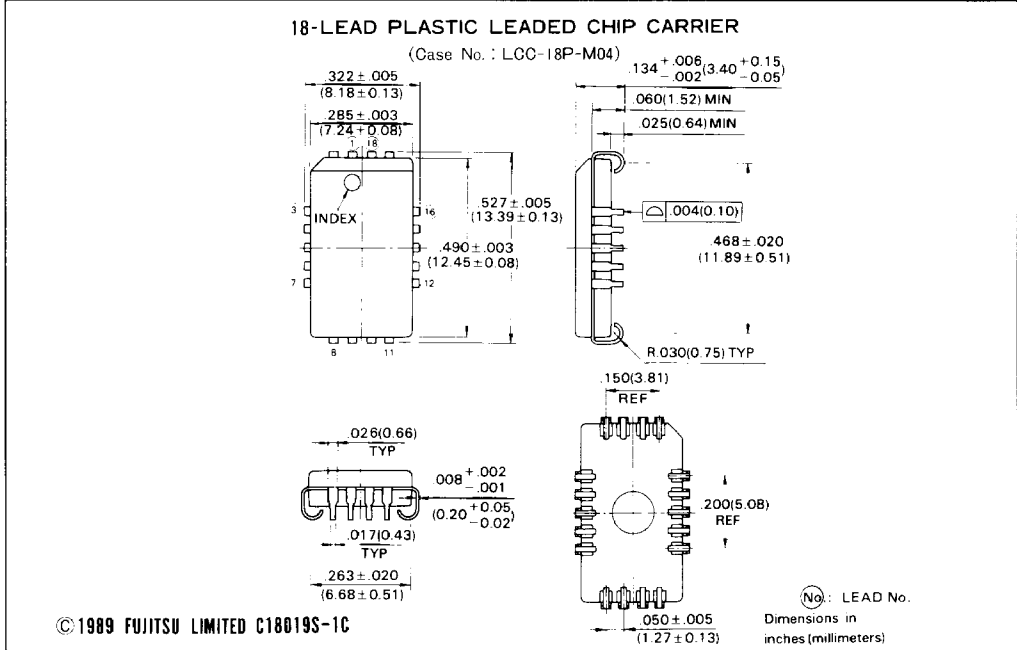
(Suffix: -P)

2



PACKAGE DIMENSIONS

(Suffix: -PD)



2