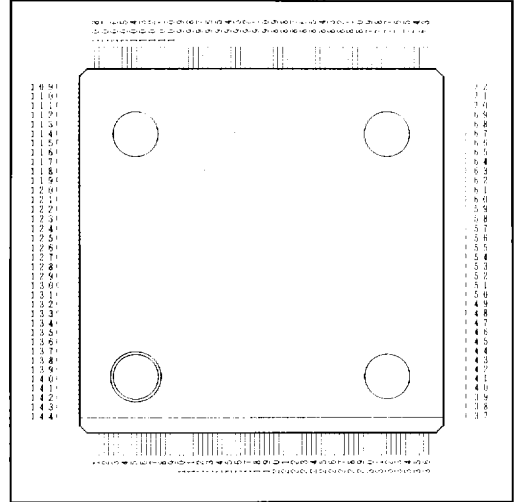


T7518

Hard Disk Controller

1. GENERAL DESCRIPTION

The Toshiba T7518 is a high-performance hard disk controller (HDC) which contains a disk controller, a system interface circuitry and a control CPU. The HDC, as combined with an external ROM, RAM and VFO circuit, offers a complete disk controlling function having SASI (Sugart Associates System Interface). In addition, the HDC is provided with extension pins for compatibility with SCSI (Small Computer System Interface). Its disk interface is based on data input/output by NRZ (Enhanced Small Device Interface). Use of a VFO circuit can provide an ST506 type disk interface.



2. FEATURES

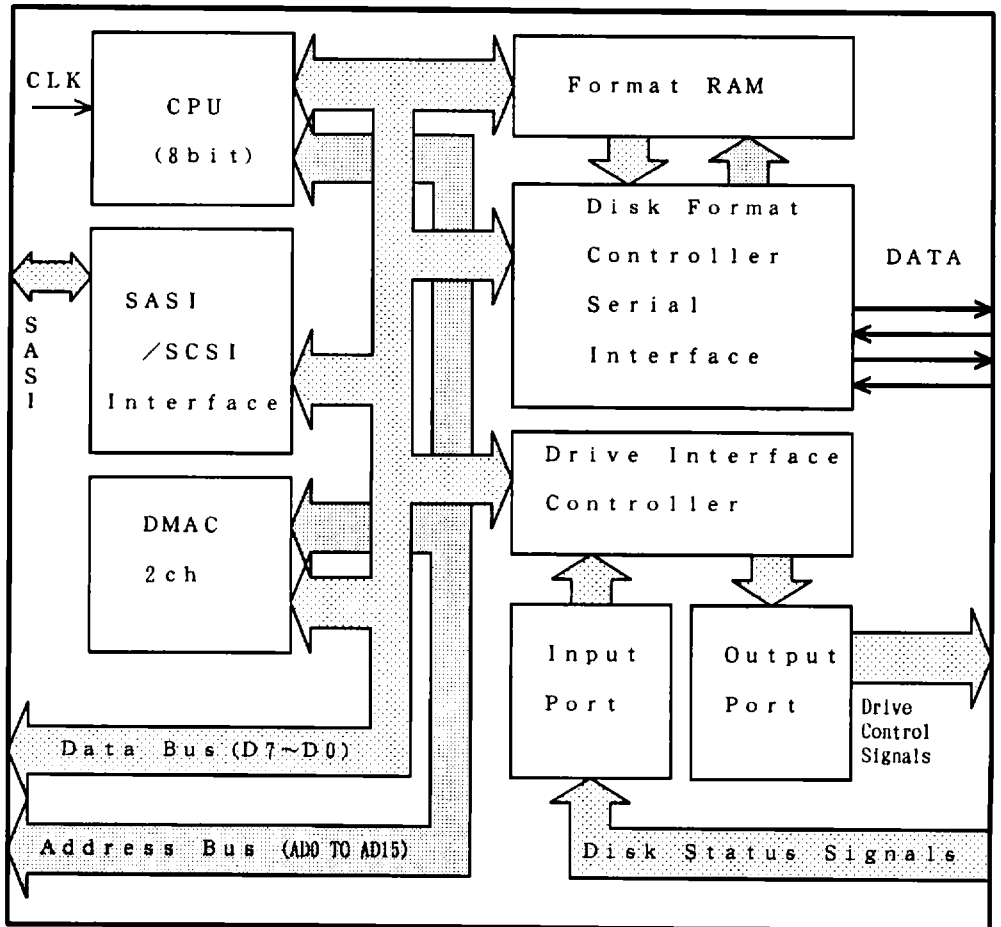
- o Si-gate high-speed CMOS technology
- o Low current dissipation ... Max. 30 mA
- o System interface
 - SASI
 - Compatible with SCSI
 - Intelligent disk controller
 - Data transfer rate ... 625 K bytes/s (type.), 1.2 M bytes/s (max.)
- o Disk control
 - Format programmable
 - Ability to control floppy disk
 - On-chip ECC/CRC
 - ID CRC ($X^{16} + X^{15} + X^2 + 1$) or ($X^{16} + X^{12} + X^5 + 1$)
 - DATA ECC ($X^{21} + 1$) ($X^{11} + X^2 + 1$)
- o Disk interface
 - ESDI/ST506
 - VFO control function
 - Up to 4 disks can be connected.
 - 8 heads (standard)
 - NRZ data transfer rate ... max. 5 (10) M bps
- o Single +5 V power
- o 144-pin flat package

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HARD DISK CONTROLLER

3. APPLIED SYSTEM

3.1 Block Diagram of HDC



HARD DISK CONTROLLER

4. PIN DESCRIPTION

4.1 Pin Configuration

PIN	I/O	SYMBOL	PIN	I/O	SYMBOL	PIN	I/O	SYMBOL	PIN	I/O	SYMBOL
1	O3	AD7	37	I	ACK0	73	IO	DB2	109	I	TRK000
2	O3	AD8	38	I	TC0	74	IO	DB3	110	I	SKCOMP0
3	O3	AD9	39	I	ID0	75	IO	DB4	111	I	DKSY0
4	O3	AD10	38	I	HRD0	76	IO	DB5	112	I	SLCT0
5	O3	AD11	41	I	HWR0	77	IO	DB6	113	I	STDY0
6	O3	AD12	42	I	RST0	78	IO	DB7	114	I	SKED0
7	O3	AD13	43	I	SCS10	79	G	GND	115	I	SCTP0
8	O3	AD14	44	I	T9	80	O	DIR	116	I	SELD10
9	O3	AD15	45	I	ATN0	81	O	STEP	117	I	SELDO0
10	G	GND	46	V	VDD	82	O	RWC	118	I	INDELO
11	IO	D7	47	O	CK4F	83	O	HRQ0	119	I	PWCLRO
12	IO	D6	48	O	CK2F	84	O	PERR	120	I	INT0
13	IO	D5	49	O	TS1	85	O	PT0	121	I	NM10
14	IO	D4	50	O	TS2	86	O	PT1	122	I	WAIT0
15	IO	D3	51	O	TS3	87	O	EX1	123	I	BUSREQ0
16	IO	D2	52	O	TS4	88	O	EX0	124	I	RESET0
17	IO	D1	53	O	TS5	89	O	HSEL2	125	G	GND
18	IO	D0	54	O	TS6	90	O	HSEL1	126	O	RAMEN0
19	V	VDD	55	O	TS7	91	O	HSEL0	127	O	ROMEN0
20	I	CLK	56	O	TS8	92	O	DSEL3	128	O	TRAP
21	I	MD0	57	O	TS9	93	O	DSEL2	129	O	HALT0
22	I	CLK1	58	O	TS10	94	O	DSEL1	130	O3	MREQ0
23	I	MD1	59	O	TS11	95	O	DSEL0	131	O3	IORQ0
24	I	MD2	60	O	TS12	96	O	AMEN	132	O3	RDO
25	I	PINH0	61	O	TS13	97	O	WCLK	133	O3	WRO
26	I	T5	62	O	I/O	98	O	WCP	134	O	BUSACK0
27	I	T6	63	O	C/D	99	O	WRDT	135	O	M10
28	I	T7	64	O	BSY	100	O	WRGT	136	O	RESH0
29	I	T8	65	O	HBEN	101	O	RDGT	137	V	VDD
30	I	TBRQ0	66	O	REQ	102	V	VDD	138	O3	AD0
31	I	T1	67	O	MSG	103	I	RDDT	139	O3	AD1
32	I	T2	68	O	FIFO	104	I	RCLK	140	O3	AD2
33	I	T3	69	G	GND	105	I	SCLK	141	O3	AD3
34	I	T4	70	IO	DBP	106	I	AMFUD	142	O3	AD4
35	I	NC	71	IO	DB0	107	I	READY0	143	O3	AD5
36	I	SEL0	72	IO	DB1	108	I	WFAULT0	144	O3	AD6

O:Output, I:Input, IO:Input/Output, O3:Output, three-state

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HARD DISK CONTROLLER

4.2 Pin Functions

NO.	SYMBOL	I/O	NAME AND FUNCTION
138	AD 0	0	<p>Address Bus (16 bits): Provides the address for access to the memory or I/O port and the buffer memory address for DMA data transfer.</p>
139	AD 1	0	
140	AD 2	0	
141	AD 3	0	
142	AD 4	0	
143	AD 5	0	
144	AD 6	0	
1	AD 7	0	
2	AD 8	0	
3	AD 9	0	
4	AD 10	0	
5	AD 11	0	
6	AD 12	0	
7	AD 13	0	
8	AD 14	0	
9	AD 15	0	
11	D 7	I O	<p>Data Bus (8 bits): Provides communication between the CPU, memory and I/O devices, and DMA data transfers.</p>
12	D 6	I O	
13	D 5	I O	
14	D 4	I O	
15	D 3	I O	
16	D 2	I O	
17	D 1	I O	
18	D 0	I O	
20	CLK	I	Internal CPU Clock: Divided by 2 on-chip and supplied to the CPU. Also used as the basic clock of the internal timer.
120	INTO	I	<p>nearly equivalent to the TLCS-Z80 signal lines.</p>
121	NMIO	I	
129	HALTO	0	
122	WAITO	I	
135	MIO	0	
136	RFSHO	0	
130	MREQO	0	
131	IORQO	0	
123	BUSREQO	0	
134	BUSACKO	I	
124	RESETO	0	System Reset: When this signal goes low, the CPU and registers are initialized.
127	ROMENO	0	Internally Decoded ROM Select: Normally, connected to the ROM-CS pin.
126	RAMENO	0	Internally Decoded RAM Select: Normally, connected to the RAM-CS pin.

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HARD DISK CONTROLLER

NO.	SYMBOL	I/O	NAME AND FUNCTION
132	RDO	0	Read control signal from Memory or I/O: Normally connected to the ROM or RAM-OE (Output Enable) pin.
133	WRO	0	Write control signal from Memory or I/O: Connected to the RAM-WE (Write Enable) pin.
30	TBRQ0	I	Hold Request: Provides the hold request signal (HRQ0) from an internal block to request the CPU to hold.
83	HRQ0	0	Hold Request: Produced by the DMA block in the T7518 to request the CPU to hold. Normally, connected to BUSREQ0 and TBRQ0.
39	ID0	I	Connects one bit of the data bus which indicates the ID as the target of SCSI on the board using this LSI.
64	BSY	0	SCSI Signal Line: Active high. Connected to the driver which drive the SCSI bus.
63	C/D	0	
62	I/O	0	
67	MSG	0	
66	REQ	0	
36	SEL0	I	
37	ACK0	I	SCSI Signal Line: Can be directly connected to the SCSI bus.
42	RST0	I	
45	ATN0	I	
70	DBP	I 0	
71	DB0	I 0	SCSI Data Bus.
72	DB1	I 0	
73	DB2	I 0	
74	DB3	I 0	
75	DB4	I 0	
76	DB5	I 0	
77	DB6	I 0	
78	DB7	I 0	
38	TC0	I	Reserved. (Used for applications other than SCSI. This pin must be connected to VDD when SCSI is used.)
40	HRD0	I	
41	HWR0	I	Reserved
65	HBEN	0	
68	FIFO	0	Reserved
43	SCSI0	I	SCSI Mode Select: (SCSI mode is selected with this signal low.)
25	PINH0	I	Signal which selects the mode disabling parity check of the SCSI data bus.
82	RWC	0	Write Current Control (general-purpose port).

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HARD DISK CONTROLLER

NO.	SYMBOL	I/O	NAME AND FUNCTION
89	HSEL2	0	Drive Head Select (general-purpose port).
90	HSEL1	0	
91	HSEL0	0	
100	WRGT	0	Write Gate.
110	SKCOMP0	I	Drive Seek Complete.
109	TRK000	I	Signal which indicates that the drive head is on track 0 position. (general-purpose port).
108	WFAURTO	I	Drive Fault Detect.
118	INDEX0	I	Drive Index.
107	READY0	I	Drive Ready.
81	STEP	0	Step: Moves the head for seeking (general-purpose port).
92	DSEL3	0	Drive Select (general-purpose port).
93	DSEL2	0	
94	DSEL1	0	
95	DSEL0	0	
80	DIR	0	Direction: Specifies the direction the head moves for seeking.
116	SELD00	I	Response to DSEL from the drive.
117	SELD10	I	
22	CLK1	I	Basic System Clock.
48	CK2F	0	Clock derived from dividing the clock by 4.
47	CK4F	0	Clock derived from dividing the clock supplied from CLK1 by 2.
105	SCLK	I	Basic Disk Clock: This clock is the same frequency as the disk data transfer rate.
104	RCLK	I	Read Clock: Synchronized to disk read data (RDDT).
103	RDDT	I	Disk Read Data (NRZ): Indicates "1" when it is high.
101	RDGT	0	Signal informing the VFO circuit that read operation has started.
106	AMFUD	I	Signal which is input to the HDC when the VFO detects an address mark (missing clock).
96	AMEN	0	Signal indicating that the write data is an address mark during write operation. The VFO circuit performs missing clock processing to the write data.
97	WCLK	0	Disk Data Write Clock.
98	WCP	0	Write Precompensation.
99	WRDT	0	Write Data to disk: synchronized to write clock.

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HARD DISK CONTROLLER

NO.	SYMBOL	I/O	NAME AND FUNCTION
119	PWCLR0	I	Reset to frequency divider.
128	TRAP	O	Output by the reset signal (RST0) from the host.
112	SLCT0	I	Connect this pin to VDD.
113	STDY0	I	Connect this pin to VDD.
114	SKED0	I	Connect this pin to VDD.
115	SCTP0	I	Connect this pin to VDD.
111	DKSY0	I	Connect this pin to VDD.
84	PERR	O	
85	PT0	O	
86	PT1	O	
87	EX1	O	
88	EX0	O	
21	MD0	I	Mode Select: Used by firmware.
23	MD1	I	
24	MD2	I	
31	T1	I	Connect this pin to GND.
32	T2	I	
33	T3	I	
34	T4	I	
26	T5	I	Connect this pin to VDD.
27	T6	I	Connect this pin to GND.
28	T7	I	
29	T8	I	
44	T9	I	
49	TS1	O	Test
50	TS2	O	
51	TS3	O	
52	TS4	O	
53	TS5	O	
54	TS6	O	
55	TS7	O	
56	TS8	O	
57	TS9	O	
58	TS10	O	
59	TS11	O	
60	TS12	O	
61	TS13	O	
35	NC		No Connection: Keep this pin open.
10	[GND]	G	Connect this pin to power GND.
69			
79			
125			
19	[VDD]	V	Connect this pin to power VDD (+5V).
46			
102			
137			

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5. FUNCTIONAL SPECIFICATIONS

5.1 Function Blocks

The T7518 HDC consists of four major blocks: CPU, HOST, DISK and DMA. HDC system operation is controlled by the CPU. All registers and control flags of each block can be accessed by I/O instructions invoked from the CPU, thereby providing complete control over the HDC. Fig. 5.1 shows a functional block diagram of the HDC, including the registers.

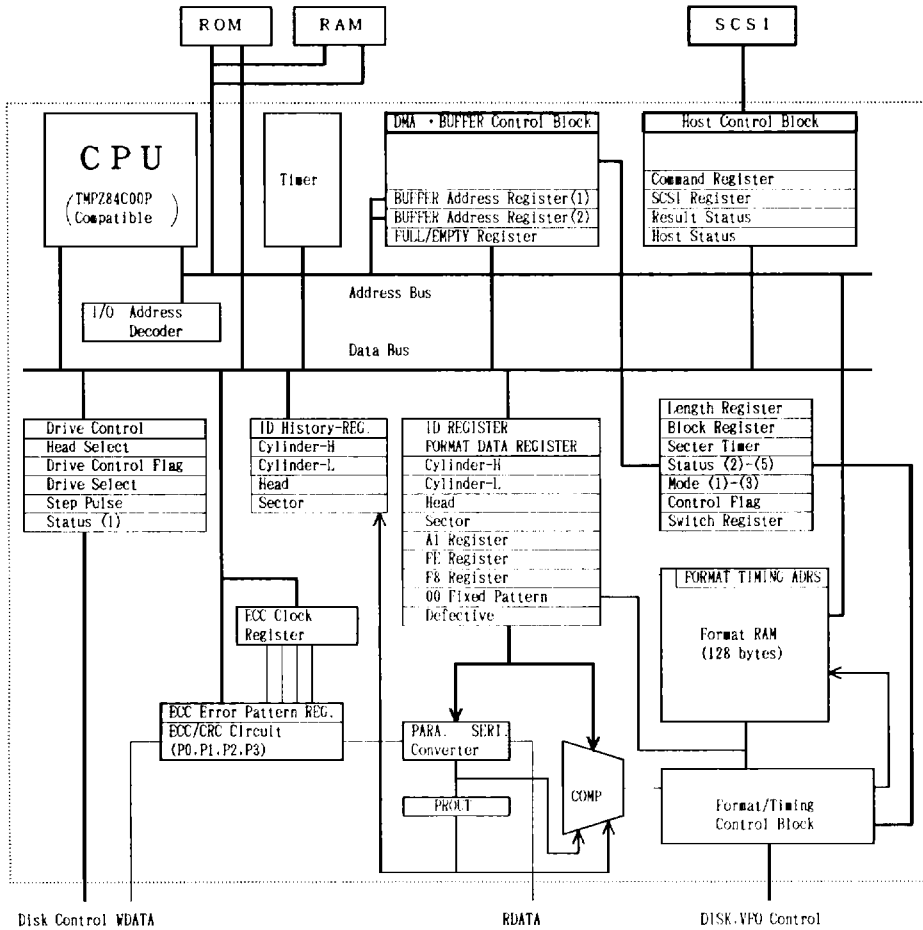


Fig. 5.1 HDC Functional Block Diagram

HARD DISK CONTROLLER

5.2 System Interface

5.2.1 Memory Interface

The HDC provides up to 64K bytes of memory, the complete space of which can be accessed by the internal CPU. The normally used memory map is shown in Fig. 5.2.1A. The memory map consists of three areas: ROM, RAM, and Format RAM. The ROM area can be up to 32K bytes and contains programs (firmware) which control the HDC, data patterns for formatting, etc... The RAM, also can be up to 32K bytes, of which 1K bytes from 8000H to 83FFH (or 8400H to 87FFH) is used as a buffer RAM area, with the rest being used as the CPU work area. The internal RAM (used for format control) is allocated to the 128-byte area from C000H to C080H, which can be accessed by the CPU through bank selection.

Access to memory is controlled by signals RDO, WRD, RAMEN0 and ROMEN0. ROMEN0 and RAMEN0 are directly used as Chip Select signals which select the ROM area and RAM area, respectively. CPU and DMA bus arbitration is performed by connecting HRQ0 to BUSREQ0. Data can be transferred in the route "disk --> RAM --> host" or the route "host --> RAM --> disk" via external buffer memory without intervention of the CPU. High-performance data transfer is assured because the RAM works as FIFO (first-in, first-out) memory. A typical inter-connection of the T7518 to the ROM/RAM is shown in Fig. 5.2.1B.

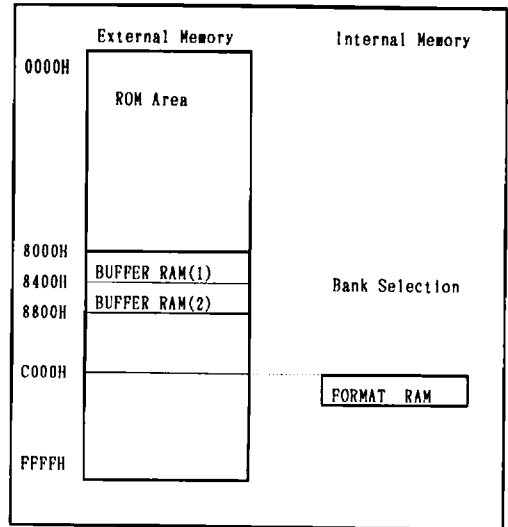


Fig. 5.2.1A Memory Map

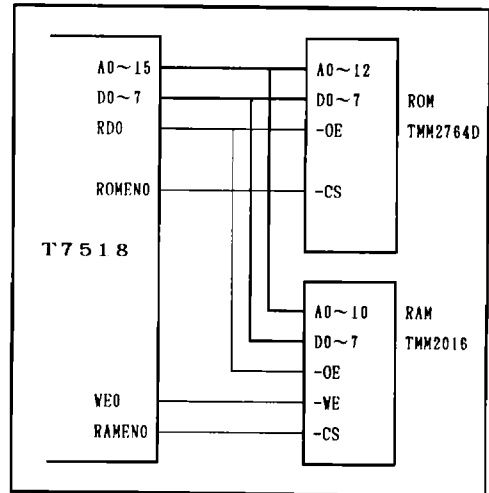


Fig. 5.2.1B Typical ROM/RAM Interconnection

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5.2.2 Disk Interface

The T7518 HDC supports the ST506 (floppy-like interface). Data is interfaced at NRZ level to enhance flexibility in hard disk control function. To achieve this, the HDC requires an external MFM encoder/decoder LSI. The TC8563F is an one-chip VFO LSI that contains this function, as well as a phase comparator and a VFO. The T7518 HDC, combined with the TC8563F, thus can support the ST506 completely. An example of this combined circuit is shown in Fig. 5.2.2.

By changing the external circuit through data interface at NRZ level, the T7518 HDC can handle RLL code and support ESDI (Enhanced Small Device Interface).

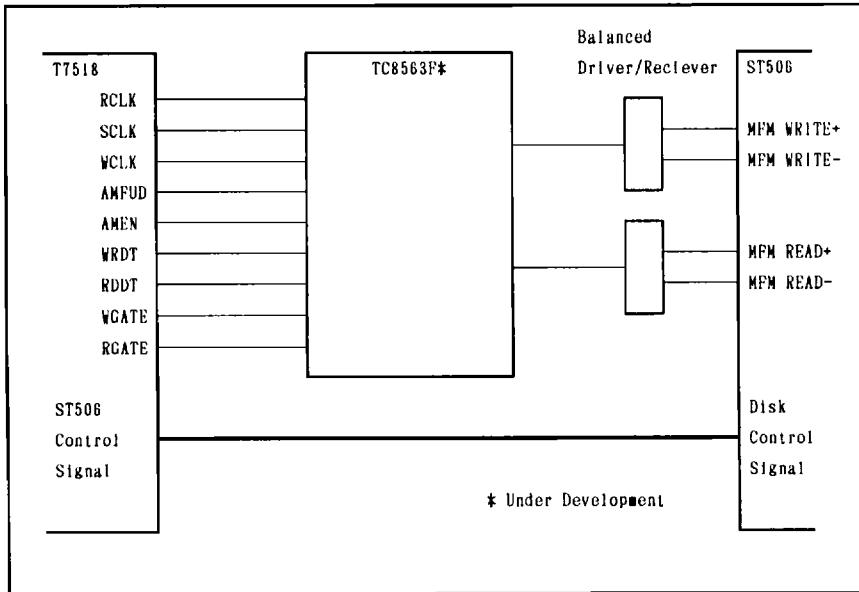


Fig. 5.2.2 Typical Circuit Using TC8563F

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HARD DISK CONTROLLER

5.2.3 Host Interface

The T7518 HDC is compatible with the subset of SCSI (Small Computer System Interface). The CPU uses firm-ware to analyze SCSI commands, so vendor and other commands can be easily changed. Data is transferred by DMA scheme at a rate of 625 KB/S (a maximum rate of 1.2 MB/S with an external circuit added).

SASI level interfacing as the subset of SCSI can be implemented by a bus driver connected externally. (See Fig. 5.2.3)

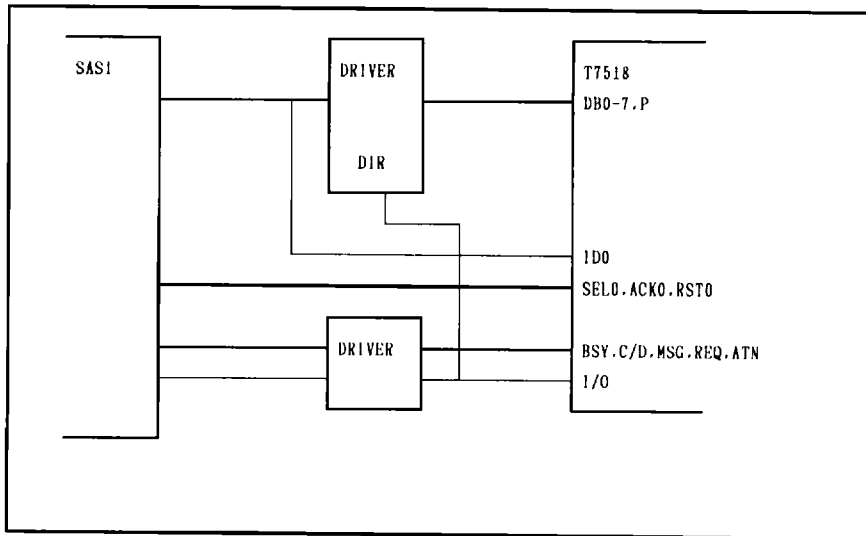


Fig. 5.2.3 Typical SASI Circuit

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5.3 CPU Block

The CPU contained in the HDC is a Z80* compatible CMOS version, equivalent to the Toshiba TMPZ84C00. All pins, except the Z80 CLK pin, that the original CPU has appear externally.

(* Z80 is trademark of Zilog.)

The internal CPU clock is a signal supplied at the HDC's CLK pin, which is divided by 2 in the circuit shown in Fig. 5.3A.

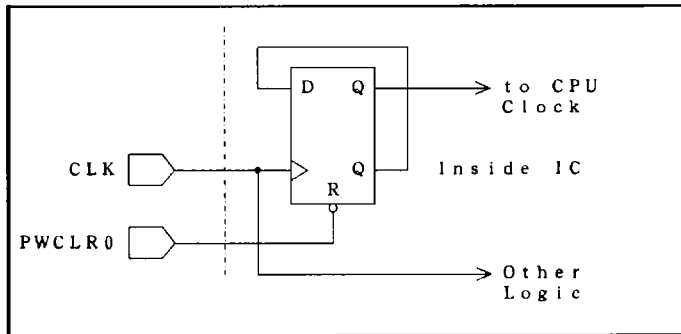


Fig. 5.3A CLK Input Circuit

PWCLR0 is the frequency divider reset signal, which is used where the internal clock must be synchronized to the external clock. Note that, as the TMPZ84C00 cannot be internally reset without clocks being input during resetting, PWCLR0 should be different from RESET. This means that at least 6 clocks (CLK's) must be input with RESET being on after PWCLR0 has been reset.

The internal CPU and DMA bus arbitration logic can be accomplished by connecting the bus request signal (HRQ0) from DMA circuit to CPU's BUSREQ0 and TBRQ0.

Fig. 5.3B shows the pin connection. Forcing the BUSREQ signal of the internal CPU to low level disables the internal CPU, thereby enabling the external CPU. Fig. 5.3C shows a typical circuit using the external CPU. This circuit allows an emulator to be set in the CPU for firmware development.

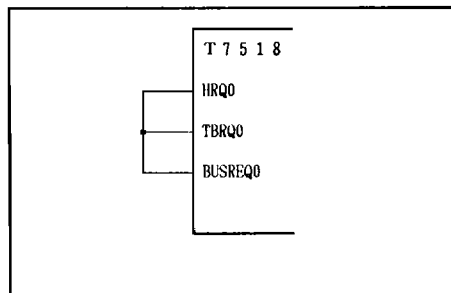


Fig. 5.3B Pin Connection for Normal Use

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HARD DISK CONTROLLER

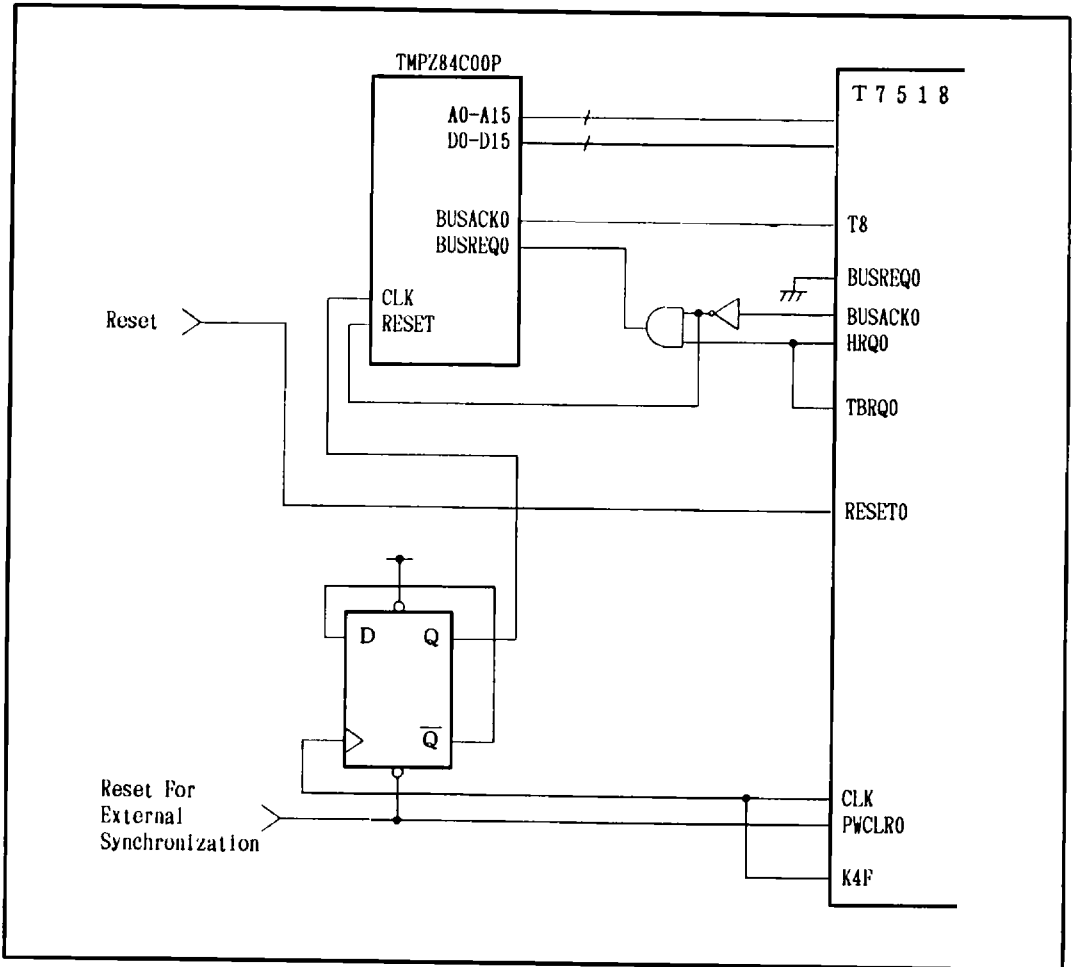


Fig. 5.3C Typical Circuit Using External CPU

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HARD DISK CONTROLLER

5.4 Registers

5.4.1 Internal Registers

ADD.	WRITE	SYMBOL	READ	SYMBOL
01	Block Register	BLKR	<---	
02	Sector Register	SECTR	<---	
03	Buffer Address 2(H)	BAR2H	<---	
04	Buffer Address 2(L)	BAR2L	<---	
05			Command Register	CMDR
06	FULL/EMPTY Register	FULR	-----	---
07	Length Register	LENGR	<---	
08	Mode Register (3)	MDR3	-----	---
09	Cylinder H	CYLRH	<---	
0A	Head Select	HSLR	Status Register (4)	STSR4
0B	Drive Control Flag	DRCR	Status Register (5)	STSR5
0C	Drive Select	DSLR	<---	
0D	Head Register	HEADR	<---	
0E	Host Status	HSTS	<---	
0F	Cylinder L	CYLRL	<---	
10	Sector Time H	STMHR	-----	---
11	FE Register	FER	Config. Register	CNFRG
12	F8 Register	F8R	Status Register (1)	STSR1
13	-----	-----	Status Register (2)	STSR2
14	Format Timing Address	FTADR	Status Register (3)	STSR3
15	A1 Register	A1R	ECC Error Pattern 1	ECCER1
16	Sector Time L	STMRL	ECC Error Pattern 2	ECCER2
17	Mode Register (1)	MDR1	-----	---
18	Reset Register	RSTR	ID History Register 1	HCYLRH
19	-----	-----	ID History Register 2	HCYLRL
1A	Step Pulse	STPR	ID History Register 3	HHEADR
1B	Mode Register (2)	MDR2	ID History Register 4	HSECTR
1C	ECC Pattern REG Clock	ECCLK	-----	---
1D	Defective Flag	DEFLG	-----	---
1E	Result Status	RSTS	-----	---
1F	Access Flag	ACSR	-----	---
20	-----	-----	-----	---
21	SCSI Register	SCSIR	-----	---
22	Transfer Word Counter	TBR	Error Register	ERG
23	-----	-----	-----	---
24	Switch Register	SWTR	SCSI Register	SCSIRR
25	-----	-----	-----	---

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HARD DISK CONTROLLER

5.4.2 Functions of Internal Registers

All internal registers are located in the I/O address space of the CPU. The internal CPU operates each of the registers to control the HDC. The function of each register is described below.
(Ex.)

[Register name] [Symbol] (R: Read, W: Write)

- o Command Register [CMDR] (R)
The command register temporarily holds the contents of the host data bus (DB0 to 7).
- o Host Status Register [HSTS] (R/W)
The host status register is used to transfer host status which can be read from the host bus (HRD0, SEL0=0, ID0=1). It cannot be used in the SCSI mode.
- o Result Status [RSTS] (W)
The result status register is used to transfer host status which can be read from the host bus (HRD0, SEL0=0, ID0=0). It cannot be used in the SCSI mode.
- o Length Register [LENGR] (R/W)
The length register is used to set the number of sectors to be transferred. The relation between the set value and the number of sectors to be set is as follows:
(FF) ---> 1 sector
(FE) ---> 2 sectors
:
:
(00) ---> 256 sectors
- o Buffer Address Register 1 [BAR1H, BAR1L]
The buffer address register 1 is an address pointer of the buffer memory used when DMA data is transferred from or to the host. No data can be set in this register. The OUT instruction with bit 2 of RSTR (reset register) set at "1" causes the BAR1H and BAR1L to be reset and initialized to 0.
- o Buffer Address Register 2 [BAR2H, BAR2L] (R/W)
The buffer address register 2 is an address pointer of the buffer memory used when data is transferred from or to the disk. The effective address consists of the low-order 2 bits of BAR2H and the 8 bits of BAR2L, making a total of 10 bits.

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HARD DISK CONTROLLER

o FULL/EMPTY Register [FULR] (W)

FULR is a flag register which manages data status in the buffer needed for its FIFO operation. The value to be set in this register depends on the data transfer mode.

- (1) DMA data transfer between the host and buffer memory.
- (2) Data transfer between the disk and buffer memory.
The data transfer defined in (1) and (2) above uses the SINGLE mode (which is selected by the mode register 2) and therefore does not require the FULL/EMPTY register to be set.
- (3) Writing host data to the disk.

This corresponds to normal disk write. Set the FULR as follows, according to the sector length of the disk:

128 bytes/sector	00H
256 bytes/sector	F0H
512 bytes/sector	FCH
1024 bytes/sector	FEH

In the burst DMA transfer mode (selected by the mode register 1), FFH must be set in the FULR regardless of the sector length.

- (4) Transfer of disk data to the host.

FFH must be set in the FULR regardless of the sector length.

o Block Register [BLKR] (R/W)

THE HDC performs multi-track processing with control returned to the CPU. This requires the remaining access sectors on each track to be set in the disk block before execution of multi-track processing. The relation between the set value and the number of sectors is as follows:

(FF)	----->	1 sector/track
(FE)	----->	2 sectors/track
.		.
(00)	----->	256 sectors/track

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HARD DISK CONTROLLER

o Format Timing Address Register [FTADR] (W)

The format timing address register specifies the starting address of format RAM. (For the format RAM, see 5.4.3 Format RAM.)

The timing pattern for a normal read/write cycle begins at the address specified by this register.

In a format write cycle, the first pattern begins at address 0 of the format RAM and the second and subsequent patterns begin at the address specified by the FTADR each time new sector formatting. This is because the track format on the disk is composed of the leading index field and succeeding sectors.

o Disk Address Registers [SECTR, CYLRH, CYLRL, HEADR] (R/W)

These are four registers (cylinder H, cylinder L, head and sector) which indicate the ID address of the disk. The sector register has an incrementing function for multi-sector processing. The length of a disk ID can be 2, 3 or 4 bytes, which is selected by the mode register 1 and the switch register.

These disk address registers are normally used to indicate the starting ID for a read/write operation but, in a format write cycle, are used to store parameter data.

o Data Pattern Registers [FER, F8R, A1R] (W)

These are data registers that are needed to format a disk. In actual disk formatting, the disk address registers are additionally used. Address mark data are contained in the A1R, ID area sync patterns in the FER, and data area sync patterns in the F8R.

The disk address registers are used to contain gap patterns for formatting and data patterns in the data field. (What register to use can be specified as format RAM data.)

GAP	SYNC	A M	F E	I D	CRC	GAP	SYNC	A M	F 8	DATA	E C C	GAP
-----	------	--------	--------	-----	-----	-----	------	--------	--------	------	-------------	-----

Example of format.

HARD DISK CONTROLLER

o Sector Timer Register [STMRH, STMRL] (W)

The sector timer register uses 2 bytes to contain values of sector processing time. It is used for a read/write cycle in the data field. The data setting is given as follows:

$$8 \times (\text{number of bytes in data field} + 2) \times (1 + \text{rotation change rate} + \underbrace{0.01}_{\substack{\uparrow \\ \text{margin}}}) \times \text{bit clock cycle time (ns)}$$

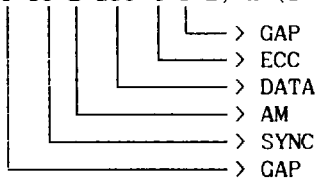
Before being actually set in the register, the value derived from the above calculation must be divided by 200 with the resulting fractions truncated. (This is because entry of 10 MHz in CLK causes the timer count clock to be 5 MHz = 200 ns).

The sector processing time is defined as the time from timer ID detection to the completion of data processing.

Ex. 256 bytes/sector

(2355) 10 932 H -- complimentary F6CEH (value to be set)

$$8 \times (3+13+2+256+4+3+2) \times (1+0.03+0.01) \times 200 / 200 = 2354.56$$



HARD DISK CONTROLLER

o Defective Flag Register [DEFLG] (W)

The defective flag register is used to indicate the position of a defective flag defined at disk formatting. The flag is assigned to one bit of the ID field. When defective flag bit = 1 is encountered during an ID search cycle in the data read/write mode, system will terminate the read/write operation and sets an error in the status register 5.

The relation between the set value and the flag position in the ID field is as follows:

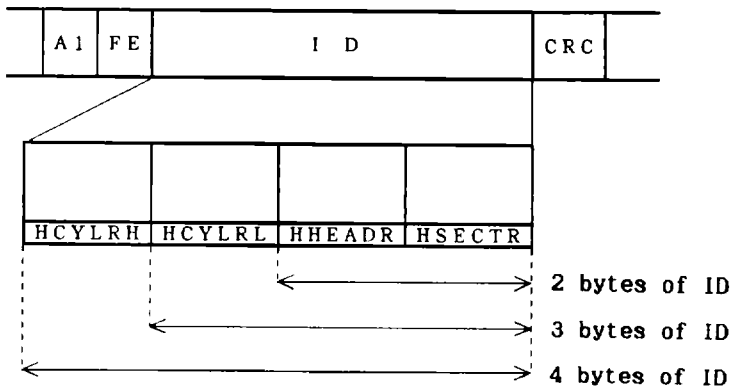
```

MSB in the ID address field ..... FFH
MSB-1 in the ID address field ..... FEH
MSB-2 in the ID address field ..... FDH
      .
      .
      .
  
```

This function performs defective track processing.

o ID History registers [HCYLRH, HCYLRL, HHEADER, HSECTR] (R)

These registers temporarily store the address data in the ID field located on the disk. The data becomes valid only when the defective flag is detected or address mismatch is encountered. The assignment of the register to ID addresses is as follows:



HARD DISK CONTROLLER

o ECC Error Pattern Register [ECCER1, ECCER2], (R)

The ECC error pattern register stores the error syndrome that occurs when an ECC error is encountered.

	D7							D0	
ECCER1	P1	P2	P3	P0	UCE	E11	E12	E13	

	D7							D0			
ECCER2	E14	E15	E16	E17	E18	E19	E20	E21			

The ECC circuit consists of four partial polynomials.

	7 Byte	4 Byte
P0 Register	$x^{22}+1$	$x^{21}+1$
P1 Register	$x^{11}+x^7+x^6+x$	----
P2 Register	$x^{12}+x^{11}+\dots+x^2+x+1$	----
P3 Register	$x^{11}+x^9+x^7+x^6+x^5+x+1$	$x^{11}+x^2+1$

The contents of the ECCER1 correspond to the result of these polynomials, as listed below:

- P0 : "1" if the contents of register P0 are all 0's
- P1 : "1" if the contents of register P1 are all 0's
- P2 : "1" if the contents of register P2 are all 0's
- P3 : "1" if the contents of register P3 are all 0's
- UCE : "1" if ECC is not correctable. Since this data is valid with the disk status ECCER bit set, do not reset this bit before the error is corrected.
- E11 to 21: Equal to the contents of bits 11 to 21 of register P0.

An ECC error can be corrected by the instruction (ECC Pattern REG Clock) which shifts registers P0 to P3.

o ECC Pattern REG Clock [ECCLK] (W)

The ECC pattern REG clock register generates clock pulses that shift registers P0, P1, P2 and P3 required to locate where an ECC error has occurred. One write cycle causes one shift. A clock pulse is generated to the register which corresponds to the bit having set "1" in the data.

	D7				D0			
	---	---	---	---	P1	P2	P3	P0

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HARD DISK CONTROLLER

o Head Select Register [HSLR] (W)

D0 to D2 are general-purpose output ports from which data is directly output to external pins HSEL0 to 2.

D7								D0	
---	---	---	FM	FD	HSEL2	HSEL1	HSEL0		

FD: floppy disk mode flag

FM: Selects FM or MFM when FD=1. To select FM, set this bit to "1".

o Drive Control Flag Register [DRCR] (W)

The drive control flag register provides general-purpose ports from which drive control signals are output.

D7								D0	
---	---	---	PT1	PT0	WCP	DIR	RWC		

o Drive Select Register [DSLRL] (W)

D7								D0	
HS	HW	0	CRFF	DSEL3	DSEL2	DSEL1	DSEL0		

DSEL0 to 3: General-purpose output ports

CRFF : Set this bit to "1" when starting the CRC initial value with "FFFF".

HW : When this bit is "1", RESULT STATUS register can be read.

HS : When this bit is "1", data is output to the host one clock earlier.

o Step Pulse Register [STPR] (W)

D7								D0	
---	---	---	PERR	STEP	TMSTR	MSG	TMRST		

TMRST : Signal to reset the 1.5 sec timer

MSG : General-purpose output port

TMSTR : Signal to start the 1.5 sec timer

STEP : General-purpose output port

PERR : Writing "1" in this bit causes the PERR pin to be set to "1". It can be cleared by RST or HCLR.

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HARD DISK CONTROLLER

o Status Register 1 [STSR1] (R)

D7						D0	
FLT	DKSY	READY	TRK000	SKOMP	SELDO	SELD1	SELDO

FLT : Input port for inverted WFAULT0 signal
 DKSY : Input port for inverted DKSY0 signal
 READY : Input port for inverted READY0 signal
 TRK000 : Input port for inverted TRK000 signal
 SKOMP : Input port for inverted SKCOMP0 signal
 SELDO : Input port for inverted SELD00 signal
 SELD1 : Input port for inverted SELD10 signal
 SELDO : Input port for inverted SELD0 signal

o Status Register 2 [STSR2] (R)

D7						D0	
INDEX	ECCER	HRCRDER	HDER	DCRCER	SYNER	HDCMPER	SCTP

INDEX : Signal which is toggled by the trailing edge of an index pulse.
 ECCER : Flag which indicates an ECC error (in the ECC mode)
 HRCRDER : Indicates a CRC error encountered when the ID field is read. Since this bit is reset when the next sector is accessed, it is valid only with the CRC error not masked by the mode register 2.
 HDER : Holds CRC errors occurring when the ID field is read.
 DCRCER : Flags that a CRC error has occurred in the data field.
 SYNER : Indicates that no sync code can be detected in the data field when the disk is read. Also indicates that data field processing has not ended within the time specified by the sector timer.
 HDCMPER : Indicates that an expected address was not found in the ID field written on the disk on the 256th trial.
 SCTP : Signal which is toggled once in response to two consecutive AMFUD signals. If AMRD = 1 is selected by the mode register 3 with INDEX detected after the firmware has issued a reset signal, the SCTP signal will be toggled at an address mark in the data field so that physical sectors can be counted by the firmware.

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HARD DISK CONTROLLER

o Status Register 3 [STSR3] (R)

D7						D0	
MSG	BLKEND	TC	TOUT	XFRERR	PRTYERR	RBFINH	AMNTFND

- MSG : MSG signal read port
- BLKEND : Indicates that all sectors set in the block register have been processed. This bit is set only when the processing has been normally terminated.
- TC : Flag which is set when the host has terminated DMA transfer in response to TCO. (Terminal count signal)
- TOUT : Time-over signal for the 1.5 sec timer
- XFRERR : Indicates that the host interface R/W control failed during DMA transfer.
- PRTYER : Indicates that a parity error occurred during data transfer on the host interface.
- RBFINH : Flag to be referenced at error retry on the disk. When set, this bit means that access of one sector to the buffer memory has been completed. At that time, the buffer address register 2 marks the beginning of the next sector area, while indicating that an error has occurred. When reset, this bit flags that the current sector has been normally terminated as long as the buffer address register 2 indicated the beginning of the next sector area. And it flags an error if the register indicates the current sector area. For the setup of retry, retry starts with one less than the current sector with the flag set and with the beginning of the current sector with the flag reset.
- AMNTFND : Address Mark Not Found. Indicates that, during three index pulses counted, neither address mark nor sync code has been found.

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HARD DISK CONTROLLER

o Status Register 4 [STSR4] (R) 0AH

D7						D0	
EMPTY	DELETED	SKENDL	SCTRDY	SLCTD	HSEL2	HSEL1	HSEL0

- EMPTY : Indicates the buffer status with the buffer memory being used in the FIFO mode. When this bit is "1" in a disk read cycle, the EMPTY bit indicates that the buffer memory is full and has no area for storage of the data to be read. In a disk write cycle, the bit indicates that the buffer memory is empty and the next data to be written on the disk has not yet been supplied from the host.
- DELETED : Deleted mark flag for "8 inch" FDD.
- SKENDL : General-purpose input port at which the reverse phase of SKED0 is input.
- SCTRDY : General-purpose input port at which the reverse phase of STDY0 is input
- SLCTD : General-purpose input port at which the reverse phase of SLCT0 is input.
- HSEL2-0 : Port at which the contents of HSEL2-0 are read from the head select register.

o Status Register 5 [STSR5] (R)

D7					D0		
CLRSTS	DKXFRER	FULL	DEF	SLCTD1	WPC	DIR	RWC

- CLRSTS : Set to "1" when (-ID0=0) and (-HRD0=0) or (-HWR0=0) (SCSI0=1)
- DKXFRER : Indicates that a transfer error was detected during transfer between the disk and buffer memory.
- FULL : Always set at "1".
- DEF : Indicates that the defective flag specified by the defective flag register was detected.
- SLCTD1 : General-purpose input port at which the inverted SLCT0 is input.
- WPC : Indicates the contents of the drive control flag register.
- DIR : Indicates the contents of the drive control flag register.
- RWC : Indicates the contents of the drive control flag register.

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HARD DISK CONTROLLER

o Mode Register 1 [MDR1] (W)

D7	D0						
DT1	DT0	ECC	ECC7	FIFO	SKIP	DELETED	ID4

DT1, DT0 : Specifies the number of bytes/sector.

DT1	DT0	
0	0	256
0	1	128
1	0	512
1	1	1024

- ECC : Provides the alternative of using ECC or CRC to check the data in the data field. ECC is selected when this bit is "1".
- ECC7 : Valid only when ECC=1. Selects the number of bytes of ECC. 7 bytes is selected when the bit is "1", and 4 bytes when the bit is "0".
- FIFO : Signal which provides the alternative of using the burst host transfer mode or not. When the bit is "0", the burst transfer mode is selected and the buffer RAM does not work in the FIFO mode, i.e., simultaneous transfer of data by the disk and host is impossible. When the bit is "1", the buffer RAM works in the FIFO mode.
- SKIP : Valid only when the switch register holds DSW1=1. With the bit at "1", data is skipped if the sync code in the data field has a specific pattern. The specific pattern indicates F8H when the DELETED bit is reset and the contents of F8R register when the DELETED bit is set.
- DELETED : Set with the FDD DELETED instruction. The sync code in the data field is normal when the bit is "1", and (F8)H when the bit is "0".
- ID4 : Specified the ID length with DSW3 in CNFGR register

REGISTER						
DSW3	ID4	Length	HCYLRH	HCYLR L	HHEADR	HSECTR
H	L	1Byte	---	---	---	0
H	H	2Bytes	---	---	0	0
L	L	3Bytes	---	0	0	0
L	H	4Bytes	0	0	0	0

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HARD DISK CONTROLLER

o Mode Register 2 [MDR2] (W)

D7						D0	
2KBF	DSKWR	HSTWR	SINGL	IDERMSK	IDRW	TCEN	DATACS

- 2KBF** : Specifies an area to contain buffer addresses for data transfer between the buffer memory and host. Addresses 8000H-83FFH are selected when the bit is "0", and 8400H-87FFH when the bit is "1". If the specified area exceeds 1K bytes, selection restarts with the starting address because the maximum buffer memory size is 1K bytes.
- DSKWR** : This flag provides the alternative of using the write command or read command for disk access. The write command is selected when the bit is "1".
- HSTWR** : This flag specifies the direction of transfer with respect to the host. When the bit is "1", the data is transferred from the host.
- SINGL** : Specifies a transfer mode in which the buffer is used. When the bit is "0", the data is transferred from the disk to the host via the buffer memory, or vice versa. When the bit is "1", data is transferred only between the disk and buffer or the host and buffer.
- IDERMSK** : This flag selects whether or not a CRC error on the ID is ignored. When the bit is "0", the CRC error is ignored.
- IDRW** : Specifies whether the disk is accessed in the ID field or in the data field. The command is decided depending on a combination of DSKWR and DATACS.

DATACS	IDRW	DSKWR	
0	1	0	ID read
1	1	1	ID write
1	0	0	Data read
1	0	1	Data write

- DATACS** : Specifies whether or not the data field on the disk format is accessed. When the bit is "1", the data field is accessed.

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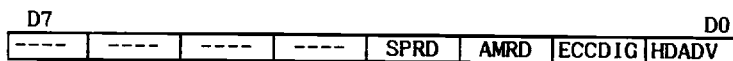
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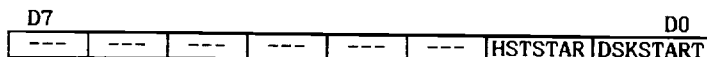
HARD DISK CONTROLLER

o Mode Register 3 [MDR3] (W)



- SPRD : Data can be read with this flag at "1" even if a CRC error occurs in the ID field.
- AMRD : Used to control the timing when SPRD is to be set. Setting this bit to "1" after an index pulse has been detected produces a signal which will be toggled at an address mark to SCTP of the status register 2 (STSR2). The signal is counted; when a required sector is reached, the data is read.
- ECCDIG : This flag is used to test the ECC circuit, and is equivalent to read long or write long of SCSI. It enables ECC data to be loaded to or from the buffer memory, thereby allowing an ECC circuit online test. For example, data which should cause an ECC error is written onto the disk and it is checked whether or not the error can be detected and corrected when the data is read.
- HDADV : This flag is used to efficiently perform multi-track processing. When the bit is "1" in the disk access mode, HRQ [CPU HOLD REQUEST] falls upon completion of transfer of the last sector on the current track. This then causes the CPU to resume. When the firmware makes head switching within a specified time, multi-track transfer can be implemented without rotational delay. Note: The last data that has been accessed will end without being transferred to the host. Therefore, the flag must be reset at the last access.

o Access Flag [ACSR] (W)



- HSTSTAR : This flag directs the start of DMA host data transfer. When "1" is written in this bit after necessary initialization, host data transfer will start.
- DSKSTART : This flag directs the start of reading from or writing to the disk. When "1" is written in this bit after necessary initialization, disk access will start.

When the access flag is set to start the appropriate operation, HRQ is output. Then the CPU will enter the hold mode with the HRQ connected externally to BUSREQ of the CPU.

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HARD DISK CONTROLLER

o Reset Register [RSTR] (W)

D7				D0			
---	---	---	---	MATRESET	RL CLR	ER CLR	ALL CLR

- MATRESET : Writing "1" in this bit forces DMA to terminate. This causes the HSTSTART and TC flags to be reset.
- RLCLR : Initializes the buffer address register.
- ERCLR : Resets all internal error flag registers. As the causes of error are not reset, they must be cleared in the specified procedure.
- ALLCLR : Resets all internal control flags and error flags.

o Config. Register [CNFGR] (R)

D7				D0			
MD2	MD1	MD0	DSW4	DSW3	DSW2	DSW1	DSW0

- MD2-0 : General-purpose input port
- DSW4-0 : The data set by the switch register [SWTR] can be read.

o Switch Register [SWTR] (W)

D7				D0			
BANK	----	INH	DSW4	DSW3	DSW2	DSW1	DSW0

- BANK : RAM bank selection signal. With this bit at "1", the internal format RAM is assigned to the CPU memory space, enabling the CPU to read or write data. The bit must be set at "0" for disk I/O.
- INT : Specifies whether or not the MSG bit is reset by a write command from the host bus.
- DSW4 : Selects a polynomial of CRC.
 "0" -- $X^{16} + X^{15} + X^2 + 1$
 "1" -- $X^{16} + X^{12} + X^5 + 1$
- DSW3 : Specifies the number of bytes in the ID field of the disk. (See Mode Register 1.)
- DSW2 : Set to "1" when the cycle of RCLK/SCLK from the drive is 100-150 ns, and to "0" when it is more than 150 ns. This flag is used to select the timing at which a DMA request is made from the disk to the buffer memory.
- DSW1 : Specifies whether or not the 'deleted' function (FDD specification) is validated. With the bit at "0", the function is invalidated.
- DSW0 : Signal which selects soft sector or hard sector scheme. With the bit at "0", soft sector scheme is valid.

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HARD DISK CONTROLLER

o Error Register [ERG] (R)

D7				D0			
WFLT	DR75	DR65	DR55	ATN	BANK	SCSI	BSY

WFLT : Indicates the contents of the flip-flop which is set by the falling edge of WFAULT0.
DR75 : Timer-over output of the internal 1.5 sec timer. This bit is reset simultaneously with the timer being reset.
DR65 : If this bit is "1", it indicates that either of the following errors has occurred:

o A parity error during host transfer.
o Host interface read/write signal out of specifications.

Identify either error by checking bits 3 and 4 of the status register 3.

DR55 : If this bit is "1", it means that an error relating mainly to the disk has occurred.

- (a) Address mark not found (Status register 3)
- (b) Sync error (Status register 2)
- (c) CRC error in the ID field (Status register 2)
- (d) Address mismatch (Status register 2)
- (e) Defective flag detected (Status register 5)
- (f) CRC error in the data field (Status register 2)
- (g) ECC error in the data field (Status register 2)
- (h) Disk data transfer error (Status register 5)
- (i) Deleted mark detected (Status register 4)
- (j) Disk drive error (if one of the following conditions is true)

WFAULT = 1
READY = 0
SKOMP = 0
SLTDO = 0

ATN : General-purpose input port at which the inverted input of ATN is read.
BANK : Port at which the BANK bit of the switch register is read.
SCSI : Inverted input of the SCSI0 signal.
BSY : Port at which the BSY bit of the SCSI register is read.

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HARD DISK CONTROLLER

o SCSI register [SCSIR] (W), [SCSIRR] (R)

D7					D0		
CLR	CLWFLT	EHWR	EHCL	ETC	CD	I/O	BSY

CLR : HCLR
CLWF : Clears the internally held WFAULT signal.
EHWR : Enables the HWR signal.
EHCL : Enables the HCLR signal in the SCSI mode.
ETC : Enables internal TC (Terminal count) from TBR register in the SCSI mode
CD : General-purpose output port. Output to the CD pin.
I/O : The value written in this register is directly output to the I/O pin. It is used as an I/O switching signal in the SCSI mode.
BSY : Forces the BSY pin to 1/0. Used to clear BSY as it is normally set when (-SELO=0) and (-ID0=0) are true.

o Transfer Byte Counter [TBR] (W)

D7				D0			
----	----	----	----	C3	C2	C1	C0

C0-3 : There may be the case where data whose length is smaller than the sector length must be transferred using this counter. To do this, set in this register the number of bytes to be transferred and start a HOST transfer cycle with the ETC bit of the SCSI register set at "1". Then the bytes will be transferred and the internal TC (terminal count) to complete the cycle. Assignment of settings to byte counts is as follows:

XF	1 byte
XE	2 bytes
XD	3 bytes
.	.
.	.

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HARD DISK CONTROLLER

5.4.3 Format RAM

The HDC contains 128 bytes of format RAM used to control the disk format. Its CPU addresses are from C000H to C080H. With "1" set in bit 7 of the switch register (SWTR), data can be read or written at these addresses by bank selection. The format RAM can be accessed from the disk on a 16-bit basis. The format timing addresses (FTADR) and contents of the corresponding CPU addresses are as shown in Fig. 5.4.3A.

FTADR	CPU Address shown in parentheses	
	MSB	LSB
0 0	(0 1)	(0 0)
0 1	(0 3)	(0 2)
0 2	(0 5)	(0 4)
0 3	.	.
	.	.

Fig. 5.4.3A Typical FORMAT RAM Configuration.

Each bit of the format RAM is defined as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EX1	EX0	CN5	CN4	CN3	CN2	CN1	CN0	RS2	RS1	RS0	AMEN	DREQ	RWGT	CRCON	AEND
(CPU SIDE ODD ADDRESS)								(CPU SIDE EVEN ADDRESS)							

- EX1, EX0 : Reserved for future expansion. These signals will be output to external pins EX1 and EX0.
- CN5-0 : Pattern counter. If the same pattern appears repeatedly, the count data is set in CN5-0 to provide a compressed pattern which allows efficient use of the format RAM area. Assignment of settings to counts is as follows:
- | | |
|----|---|
| 00 | 1 |
| FF | 2 |
| FE | 3 |
| . | . |
| . | . |
- AEND : Indicates the end point of the ID field and the data field. Normally, this bit is set to "1" by the next byte of than the CRC or ECC.
- CRCON : With this signal set at "1", CRC or ECC is generated or checked. CRCON is set to "1" in the area of the data field when CRC or ECC is generated, and until the CRC/ECC byte is reached when CRC or ECC is checked.
- RWGT : Produces RDGT/WGATE of the format. The mode register is used to select which should be output, RDGT or WGATE. (For the ST506 type, this signal must be temporarily cleared after ID search to prevent write splicing of the gap portion during a read cycle.)

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HARD DISK CONTROLLER

- DREQ** : Determines the timing at which the buffer memory is requested to send data, and the timing at which the ID is compared and verified in read/write instruction execution.
- (1) For address compare timing, the number of address bytes are output starting at one more than the ID address display format location.
 - (2) In the disk read mode, buffer request timing is output simultaneously with the data area.
 - (3) In the disk write mode, buffer request timing is output 2 bytes earlier than the data area. For the data field, as many bytes of format RAM as the data bytes are not needed. Output of only one bytes is necessary because the value of the internal length register (LENGR) is automatically counted under the condition that CRCON and DREQ are output simultaneously. This byte is output with AEND to inform the buffer that access to the data field has been terminated.
- AMEN** : Requests the external VFO to detect an address missing code in the disk read mode. This signal holds the format RAM address until the missing code is detected (i.e., until the AMFUND signal is input). For the ST506, the signal is output at the timing 2 bytes after the read gate has been opened, while at the same time the sync code register is selected by RS2-0. In the disk write mode, AMEN indicates that the write data is an address mark.
- RS2-0** : Sets parameters for disk format. This signal is also used to select registers and determines the CRC/ECC check timing.

RS2	RS1	RS0	WRITE MODE	READ MODE	ID SEARCH MODE
L	L	L	CYLRH	DISABLE	CYLRH
H	L	L	CYLRH	DATA READ	CYLRH
L	H	L	HEADR	DISABLE	HEADR
H	H	L	ECC/CRC	ECC/CRC CHECK	SECTOR
L	L	H	DATA REG (*)	DISABLE	---
H	L	H	RA1	RA1	RA1
L	H	H	'00'	DISABLE	---
H	H	H	RFE/RF8	RFE/RF8	RFE/RF8

* DATA Register are used to temporarily store the external buffer memory data.

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HARD DISK CONTROLLER

Examples of Format RAM Data

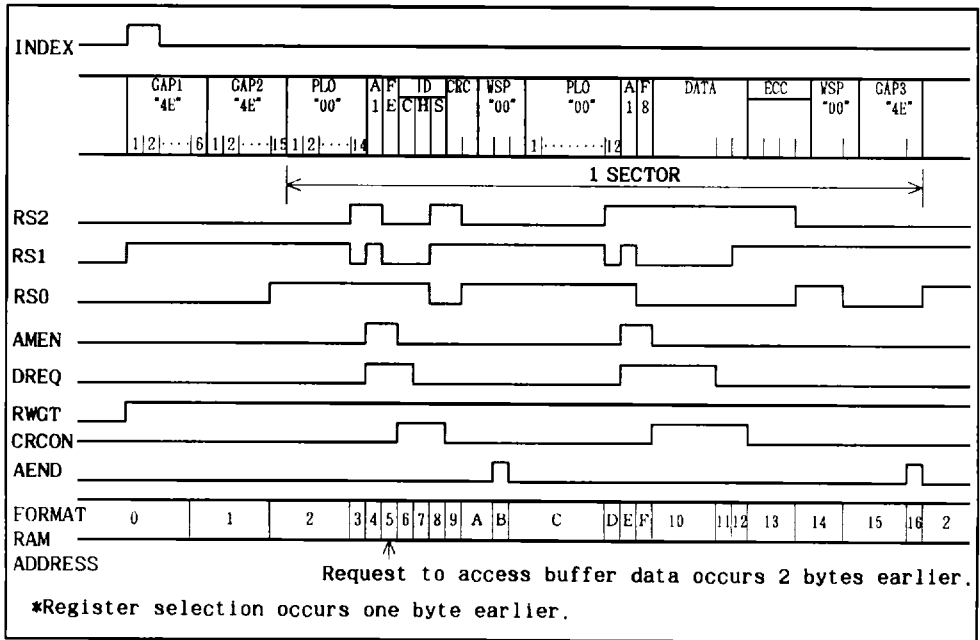


Fig. 5.4.3B Format 1

The contents of FORMAT RAM for FORMAT WRITE (ECC mode).

ADR	DB	0 4 4 H,	0 3 B H
0 0 0	DB	0 4 4 H,	0 3 B H
0 0 1	DB	0 4 4 H,	0 3 2 H
0 0 2	DB	0 6 4 H,	0 3 3 H
0 0 3	DB	0 A 4 H,	0 0 0 H
0 0 4	DB	0 F C H,	0 0 0 H
0 0 5	DB	0 3 C H,	0 0 0 H
0 0 6	DB	0 2 E H,	0 0 0 H
0 0 7	DB	0 2 6 H,	0 0 0 H
0 0 8	DB	0 C 6 H,	0 0 0 H
0 0 9	DB	0 C 4 H,	0 0 0 H
0 0 A	DB	0 6 4 H,	0 3 F H
0 0 B	DB	0 6 5 H,	0 0 0 H
0 0 C	DB	0 6 4 H,	0 3 5 H
0 0 D	DB	0 A 4 H,	0 0 0 H
0 0 E	DB	0 F C H,	0 0 0 H
0 0 F	DB	0 9 C H,	0 0 0 H
0 1 0	DB	0 8 E H,	0 0 0 H
0 1 1	DB	0 8 6 H,	0 0 0 H
0 1 2	DB	0 C 6 H,	0 0 0 H
0 1 3	DB	0 C 4 H,	0 3 E H
0 1 4	DB	0 6 4 H,	0 3 E H
0 1 5	DB	0 4 4 H,	0 3 4 H
0 1 6	DB	0 4 5 H,	0 0 0 H
0 1 7	DB	0 4 4 H,	0 3 F H
0 1 8	DB	0 4 E H,	0 0 0 H
0 1 9	DB	0 4 4 H,	0 3 F H
0 1 A	DB	0 4 5 H,	0 0 0 H
0 1 B	DB	0 0 0 H,	0 0 0 H

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HARD DISK CONTROLLER

In this example, the registers should be set following initial value.

FTADR = 02H
HEADR = 4EH
A1R = A1H
FER = FEH
F8R = F8H

Beside with this, the Buffer RAM holds ID Address data for sector-interleave.

- ADR00 : The format operation start on INDEX pulse receiving as is shown Fig.5.4.3B. The initiating entree of Format RAM is forced to "0" independently with the value set in FTADR.
- ADR00 to 01 : At first, according to the value RS2-0, HEADR register is selected and "4E" pattern is outputted as GAP data.
- ADR03 to 04 : AMEN signal is hold high level as 2 byte time so as to cover enough "A1" address mark byte.
- ADR05 : In ID section, the contents will be sent from Buffer RAM so that the DREQ signal generate to request for Data RAM. This data request will done 2 byte preceding.
- ADR0C to 0F : End of ID section will be execute by activating AEND signal. Just after ID section, Data section will start and operate as like as ID section sequence.
- ADR10 : In Data field, in the condition that both DREQ and CRCON are High level, the Data byte counting is done by means of internal length counter.
- ADR16 : AEND activation, which shows the end of Data section, results also that the address of Format RAM is set as FTADR so as to fill residue field with each sector embodies. The entree from 2 to 16 of Format RAM is used for this operation.

The number of sectors to format is defined by the block register [BLKR] value.

- ADR17 : At the final sector defined by [BLKR], the AEND activation is ignored and the pointer to Format RAM is progress to next step 17. (in return for setting the value [FTADR]) see Fig.5.4.3C.
- ADR18 : In this state, with the condition of both DREQ and CRCON being "High level ", writing operation of GAP with data "4E" will be done as well as data field. The length of this case is 4096 byte maximum however the coming of INDEX pulse also stops this operation.
- ADR19 to 1A : The INDEX pulse will interrupt this GAP writing and AEND is activated and reach to the end of FORMAT operation.

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HARD DISK CONTROLLER

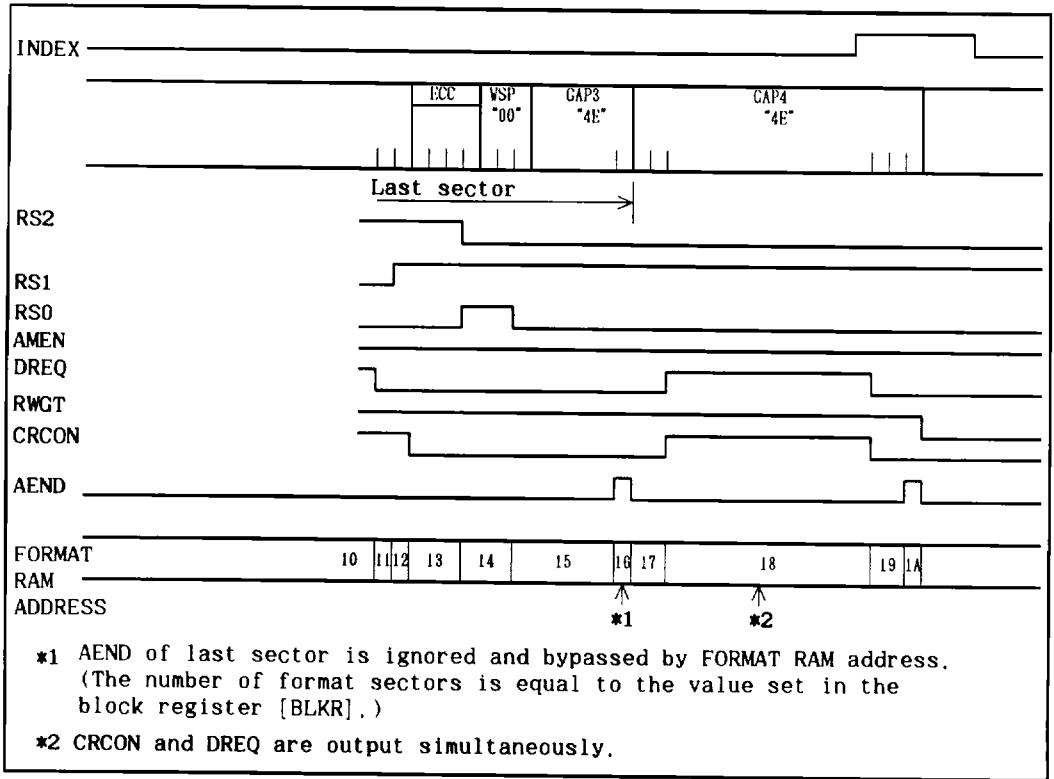


Fig. 5.4.3C Format 2

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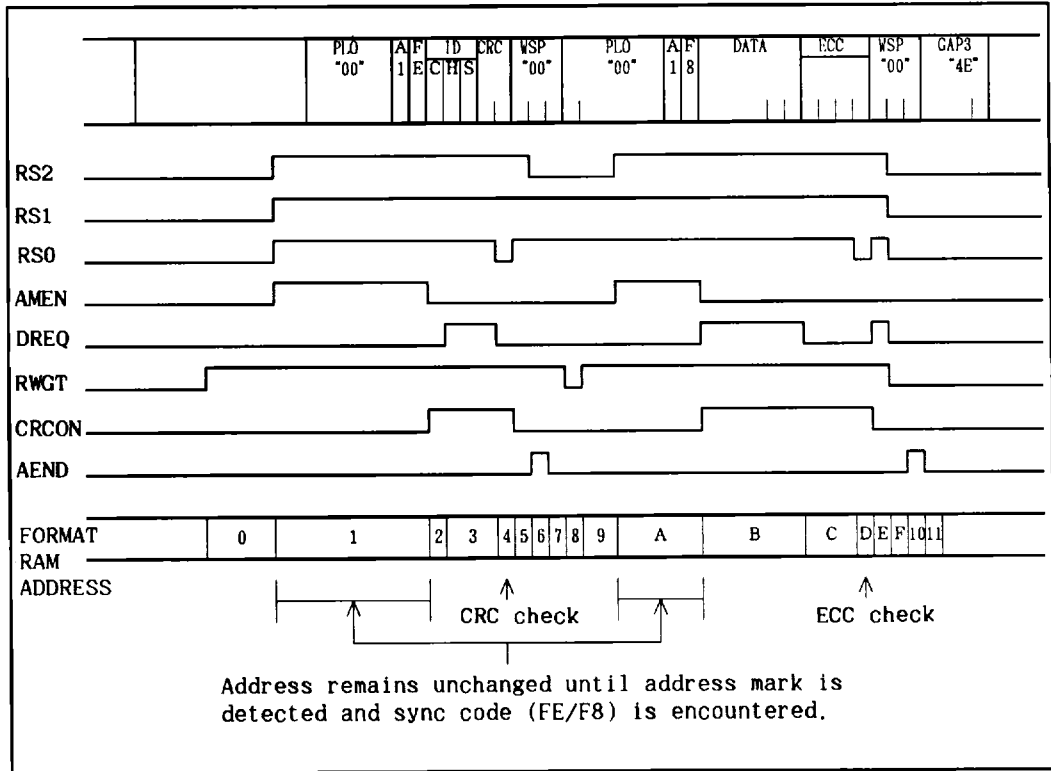


Fig. 5.4.3D READ

The contents of FORMAT RAM for DATA READ (ECC mode).

ADR	DB	004H, 03DH
000	DB	004H, 03DH
001	DB	0F4H, 000H
002	DB	0E6H, 000H
003	DB	0EEH, 03EH
004	DB	0C6H, 000H
005	DB	0E4H, 000H
006	DB	065H, 000H
007	DB	064H, 000H
008	DB	060H, 000H
009	DB	064H, 03DH
00A	DB	0F4H, 000H
00B	DB	0EEH, 000H
00C	DB	0E6H, 03EH
00D	DB	0C6H, 000H
00E	DB	0ECH, 000H
00F	DB	000H, 000H
010	DB	001H, 000H
011	DB	000H, 000H



HARD DISK CONTROLLER

In this example, the registers should be set following initial value.

FTADR = 0H
CYLRL = Cylinder Number
HEADR = Head Number
SECTR = Sector Number
A1R = A1H
FER = FEH
F8R = F8H

Beside with this, the Buffer RAM holds ID Address data for sector-interleave.

- ADR 00 : Several bytes of RWGT activation will initialize the internal data register.
- ADR 01 : The selection of RFE/RF8 register will lock the address progression of FORMAT RAM so as to waiting the AMFUDO activation from external VFO circuit. After AMFUDO is detected, sync-code (i.e.FE hex) is used to synchronize to the byte boundary of the bit oriented serial read data from disk drive. The synchronization of the byte will release the address lock and go next address.
- ADR 02 to 05 : This portion is for ID address field. The CRCON bit is stick to high level for CRC generation and detection as well as the DREQ bit is high level at a byte delayed so as to compare the ID address bytes. The high level of the CRCON bit will sustain whole CRC byte and at the second byte of the CRC byte the register for CRC checking is to be selected.
- ADR 06 : The end of ID section assigned by AEND signal and RWGT signal is temporarily Low level so as to inform external VFO of the end of the section.
- ADR 07 to 08 : Making of some idling time for skipping Write Splice (between WSP and PLO).
- ADR 09 to 0A : Address mark searching for Data section.
- ADR 0B : In the Data read process the only 1 byte of DREQ activation is needed.
- ADR 10 : The end of Data section is assigned by AEND.

In multi sector read operation, the sector register [SECTR] is automatically increased and if the block register doesn't point the final sector, the next sector read is continued.

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HARD DISK CONTROLLER

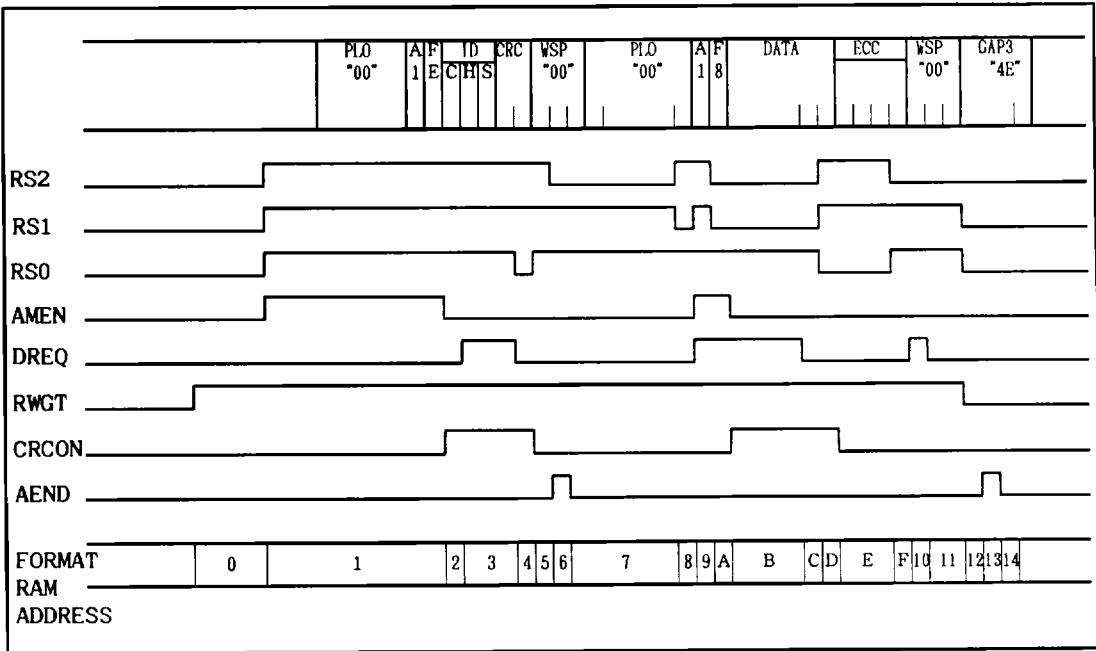


Fig. 5.4.3E WRITE

The contents of FORMAT RAM for DATA WRITE (ECC mode).

ADR	DB	004H, 03DH
000	DB	004H, 03DH
001	DB	0F4H, 000H
002	DB	0E6H, 000H
003	DB	0EEH, 03EH
004	DB	0C6H, 000H
005	DB	0E4H, 000H
006	DB	065H, 000H
007	DB	064H, 035H
008	DB	0A4H, 000H
009	DB	0FCH, 000H
00A	DB	03CH, 000H
00B	DB	02EH, 000H
00C	DB	026H, 000H
00D	DB	0C6H, 000H
00E	DB	0C4H, 03EH
00F	DB	064H, 000H
010	DB	06CH, 000H
011	DB	064H, 03FH
012	DB	000H, 03CH
013	DB	001H, 000H
014	DB	000H, 03FH

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HARD DISK CONTROLLER

The registers should be set as those of the READ operation. And operation is done same way as far as ID section in the READ operation. The WRGT output will be activated at a byte time after the AEND activation of ID section. In Data section, basically same as FORMAT but the Data field is filled with the contents of Buffer RAM.

After the activation of AEND in the Data section, next sector will be processed continuously under the condition the final sector not finished.

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6. ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

PARAMETER	SYMBOL	SPECIFICATIONS	UNIT
Supply voltage	VDD	-0.5 to +7.0	V
Input voltage	VIN	-0.5 to VDD +0.5	V
Operating temperature	Topr	-40 to 85	°C
Storage temperature	Tstg	-65 to +125	°C

6.2 DC Characteristics

(Ta=-40 to +85 °C, VDD=5V±10%)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Low level input voltage	VIL	VDD=5V	-0.5	0.8	V
High level input voltage	VIH	VDD=5V	2.2	VCC	V
Low level output voltage	VOL	IOL=2mA	--	0.4	V
High level output voltage	VOH	IOH=-1mA	4.0	--	V
Input leakage current	IIL		-10	+10	uA
Output floating leakage current	IDL		-10	+10	uA
Supply current	IDD		--	30	mA

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HARD DISK CONTROLLER

6.3 AC Characteristics

NO.	PARAMETER	MIN.	TYP.	MAX.	UNIT
1	CLK1 rise time			10	ns
2	CLK1 fall time			10	ns
3	CLK1 pulse width (high)	15			ns
4	CLK1 pulse width (low)	15			ns
5	CLK1 cycle time	50			ns
6	CLK rise time			15	ns
7	CLK fall time			15	ns
8	CLK pulse width (high)	40			ns
9	CLK pulse width (low)	40			ns
10	CLK cycle time	100			ns
11	SCLK rise time			15	ns
12	SCLK fall time			15	ns
13	SCLK pulse width (high)	75			ns
14	SCLK pulse width (low)	75			ns
15	SCLK cycle time	190			ns
16	RCLK rise time			15	ns
17	RCLK fall time			15	ns
18	RCLK pulse width (high)	75			ns
19	RCLK pulse width (low)	75			ns
20	RCLK cycle time	190			ns
21	CLK1 fall --> RAMEN0 fall			120	ns
22	CLK1 fall --> RAMEN0 rise			120	ns
23	RAMEN0 pulse width (low)	280			ns
24	CLK1 fall --> RDO fall			100	ns
25	CLK1 fall --> RDO rise			100	ns
26	RDD pulse width (low)	175			ns
27	AD15-0 valid RDO fall	90			ns
28	RD rise --> AD15-0 invalid	-20			ns
29	CLK1 data setup	30			ns
30	CLK1 data hold	20			ns
31	Memory read cycle time	380			ns
32	CLK1 fall --> WRO fall			100	ns
33	CLK1 fall --> WRO rise			100	ns
34	WRO pulse width (low)	125			ns
35	AD15-0 valid WRO fall	90			ns
36	WRO rise --> AD15-0 invalid	30			ns
37	Data valid --> WRO rise	190			ns
38	WRO rise --> Data invalid	20			ns
39	Memory write cycle time	380			ns

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HARD DISK CONTROLLER

NO.	PARAMETER	MIN.	TYP.	MAX.	UNIT
40	REQ rise --> ACKO fall (BURST MODE)	100			ns
41	ACKO fall --> HWRO fall	10			ns
42	HWRO pulse width (low)	50			ns
43	HWRO cycle time	700			ns
44	HWRO rise data setup time	20			ns
45	HWRO rise data hold time	25			ns
46	HWRO rise --> REQ fall			90	ns
47	TCO fall --> HWRO fall	30			ns
48	HWR rise --> TCO rise	30			ns
49	HRDO pulse width (low)	50			ns
50	HRDO cycle time	700			ns
51	HRDO fall data valid			70	ns
52	HRDO rise data invalid	20			ns
53	HRDO fall --> HBEN fall			90	ns
54	HRDO rise --> HBEN rise			90	ns
55	HRDO rise -->REQ fall			90	ns
56	TCO fall --> HRDO rise	30			ns
57	HRD rise --> TCO rise	30			ns
58	HBEN cycle time (FIFO MODE)	800			ns
59	REQ rise --> ACKO fall	100			ns
60	ACKO fall --> HWRO fall	10			ns
61	ACKO fall --> REQ fall	30			ns
62	HWRO pulse width (low)	45			ns
63	HWRO rise data setup time	20			ns
64	HWRO rise data hold time	25			ns
65	TC fall --> HWRO rise	30			ns
66	HWRO rise --> TCO rise	30			ns
67	HWRO rise --> REQ rise			130	ns
68	ACKO fall --> HRDO fall	10			ns
69	HRDO pulse width (low)	50			ns
70	HRDO fall data valid			70	ns
71	HRDO rise data invalid	20			ns
72	HRDO fall --> HBEN fall			90	ns
73	HRDO rise --> HBEN rise			90	ns
74	TCO fall --> HRDO rise	30			ns
75	HRD rise --> TCO rise	30			ns
76	IDO fall --> SEL0 fall (SASI MODE)	50			ns
77	BSYO fall --> SEL0 rise	50			ns
78	ACKO fall --> data valid			100	ns
79	K8RDO rise data hold	0			ns

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HARD DISK CONTROLLER

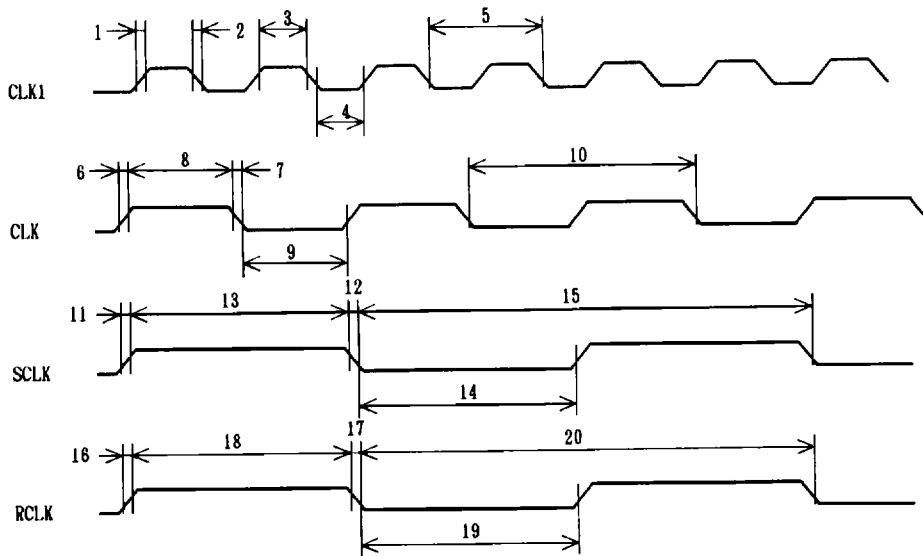
NO.	PARAMETER	MIN.	TYP.	MAX.	UNIT
80	REQ rise data setup	125		250	ns
81	ACKO fall --> REQ fall	5			ns
82	REQ fall data hold	100			ns
83	RCLK rise RDDT setup	0			ns
84	RCLK rise RDDT hold	50			ns
85	SCLK rise --> WCLK rise			40	ns
86	SCLK fall --> WCLK fall			40	ns
87	WCLK fall --> WRDT			55	ns
88	SCLK fall --> WRDT	40		85	ns

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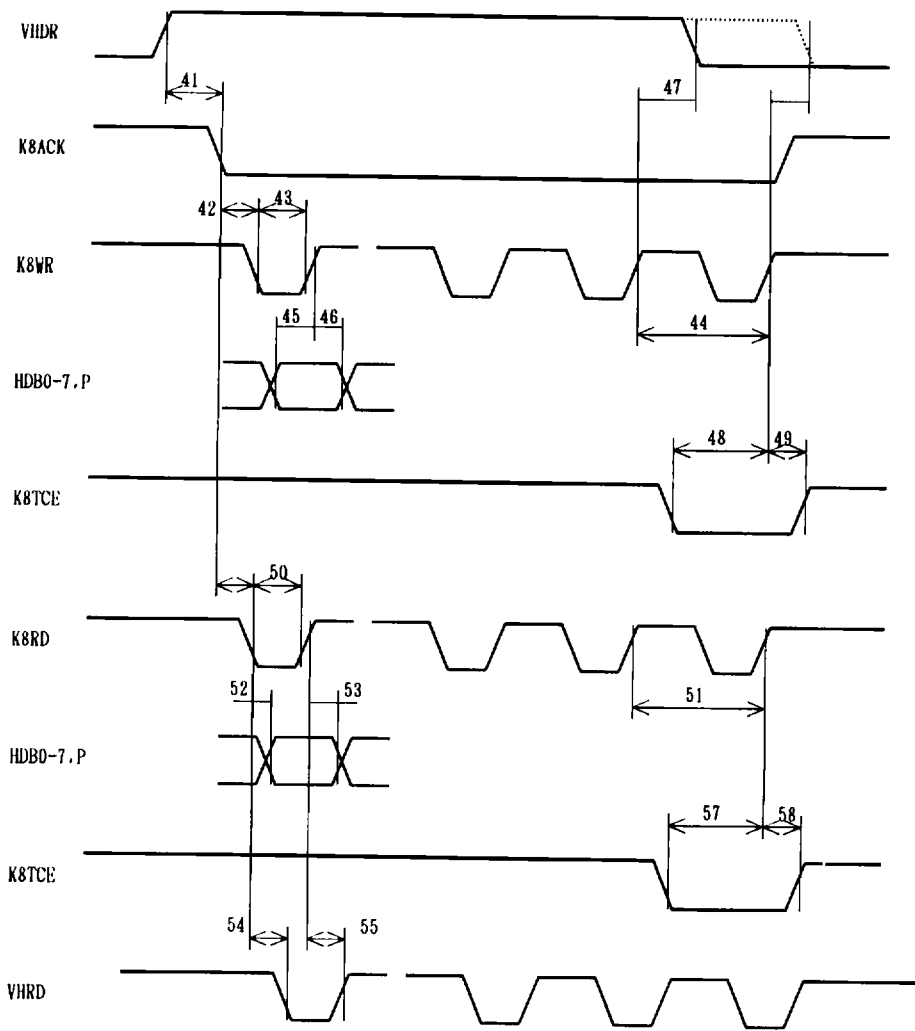
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6.3.1 AC Timing

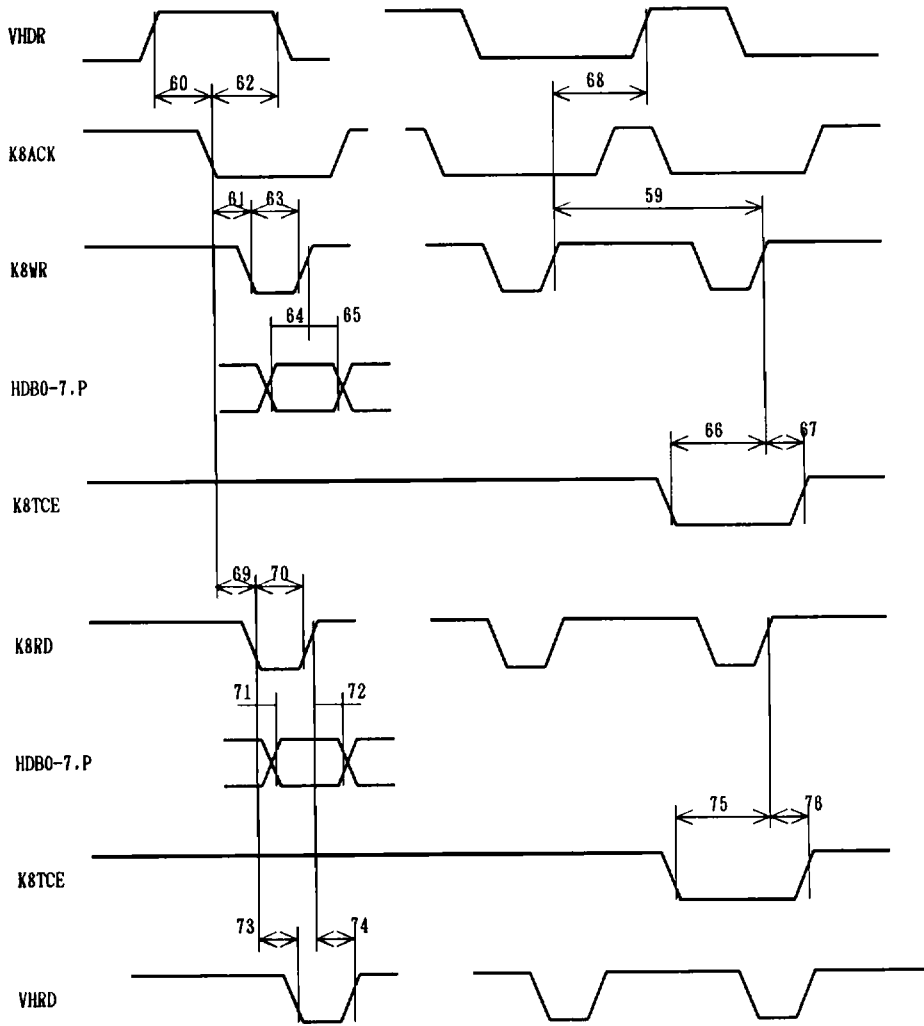


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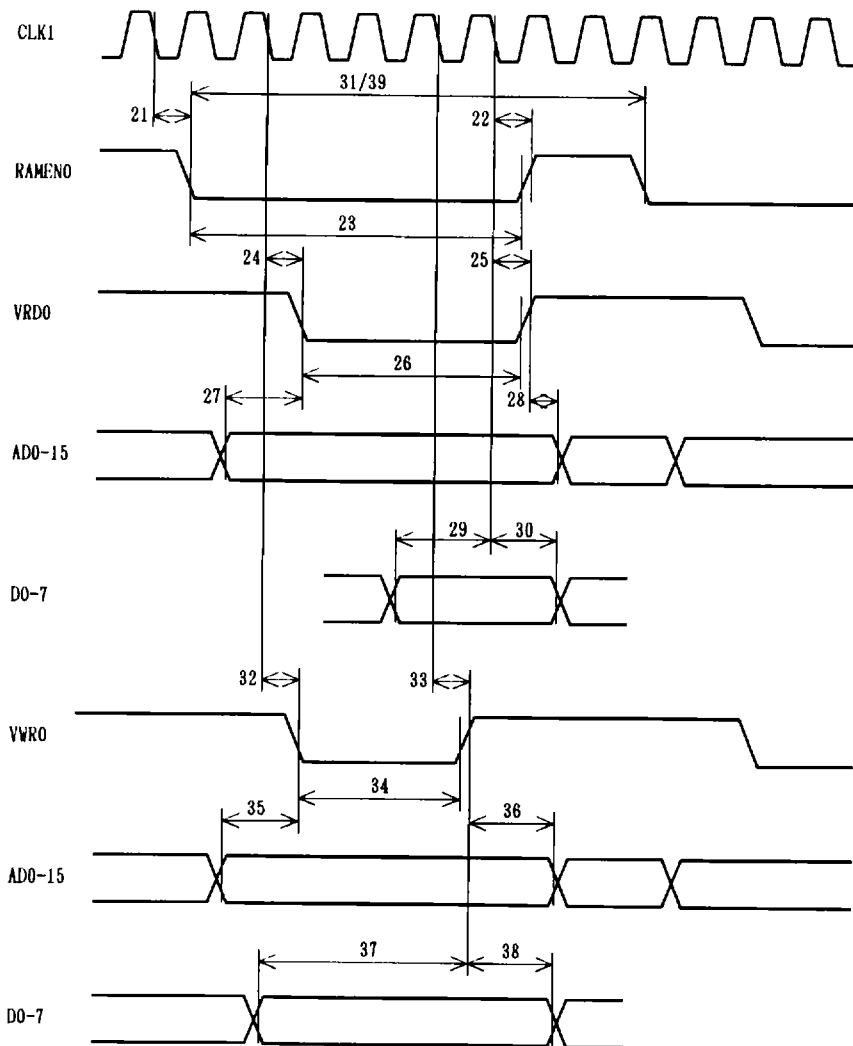
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