74S225/A

Asynchronous First-In First-Out Memory (FIFO) 16 x 5

Advanced Micro Devices

Features/Benefits

- DC to 20-MHz shift-in/shift-out rates
- Fully expandable by word width and depth
- Three-state outputs
- TTL-compatible inputs and outputs
- Functionally compatible with T.I. SN74S225
- Designed for extended testability

Description

The 74S225/A is a Schottky-clamped transistor-transistor logic (STTL) 16x5 First-In-First-Out memory (FIFO) which operates from DC to 10/20 MHz. The data is loaded and emptied on a first-in-first-out basis through asynchronous input and output ports. These devices are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. Both word length and FIFO depth are expandable. Unload clock output (Pin 3) is designed for testability of V_{OL}.

Ordering Information

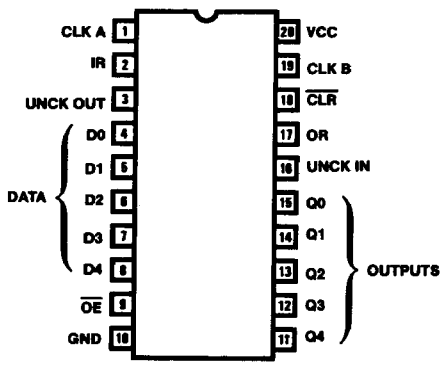
Part Number	Package	Temp	Description
74S225	CD 020, PD 020	Com	10 MHz in/out
74S225A	CD 020, PD 020	Com	20 MHz in/out

Pin Names

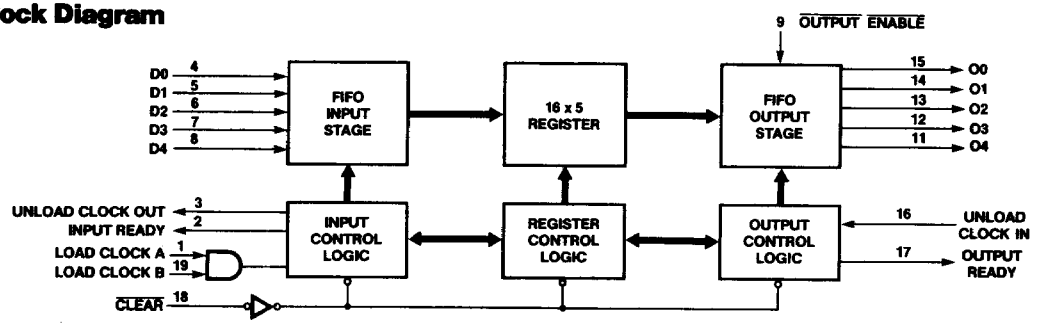
PIN #	PIN NAME	DESCRIPTION
1	CLK A	Load clock A
2	IR	Input ready
3	UNCK OUT	Unload clock output
4-8	D0-D4	Data inputs
9	$\overline{OE}$	Output enable
10	GND	Ground pin
11-15	Q4-Q0	Data outputs
16	UNCLK IN	Unload clock input
17	OR	Output ready
18	$\overline{CLR}$	Clear
19	CLK B	Load clock B
20	V_{CC}	Supply voltage

Pin Configuration

74S225/A . . J or N Package
(Top View)



Block Diagram



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Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65 to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225A MIN	74S225A TYP	74S225A MAX	74S225 MIN	74S225 TYP	74S225 MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
t_A	Operating free-air temperature		0		75	0		75	°C
t_{LCKH}	LOAD CLOCK pulse width, A or B, t_w (HIGH)	2	22		36	25			ns
t_{IDS}	Setup time, data to load clock	2	-20↑*			-20↑*			ns
t_{IDH}	Hold time, data from load clock	2	50↑			70↑			ns
t_{UCKL}	UNLOAD CLOCK INPUT pulse width, t_w (LOW)	4	7		36	7			ns
t_{CLW}	CLEAR pulse width, t_w (low)	2	20			40			ns
t_{CLCK}	Setup time, clear release to load clock, t_{su}	2	10			25↑			ns

* Data must be setup within 20 ns after valid Load Clock (A or B) pulse (positive transition).

↑ = Arrow indicates that it is referenced to the LOW-to-HIGH transition.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	74S225A MIN	74S225A TYP	74S225A MAX	74S225 MIN	74S225 TYP	74S225 MAX	UNIT
f_{IN}	Load clock A or clock B	Cascade Mode**	2	20	22		10	20		MHz
		Standalone Mode								
t_{LCIRL}	CLK A or CLK B to IR↓ **		2		43	55		55	75	ns
t_{LCCOL}	CLK A or CLK B to UNCK OUT↓		2		31	40		25	50	ns
f_{OUT}	Unload clock input	Cascade Mode***	4	20	22		10	20		MHz
		Standalone Mode								
t_{UCKORL}	UNCK IN ↑ to OR LOW		4		26	35		30	45	ns
t_{UCKORH}	UNCK IN ↑ to OR HIGH		4		32	45		40	60	ns
t_{ODH}	Output data hold, UNCK IN to output data		4	20	30		20	50		ns
t_{ODS}	Output data setup, UNCK IN to output data		4		41	55		50	75	ns
t_{RIP}	CLK A or CLK B to OR ↑		7		167	220		190	300	ns
t_{CLOL}	CLR to OR ↓		6		31	40		35	60	ns
t_{CLIH}	CLR to IR ↑		6		15	20		16	35	ns
t_{UCKOW}	Pulse width, UNCK OUT, t_w		2	7	11		7	14		ns
t_{ORD}	OR ↑ to output data		4		9	15		10	20	ns
t_{BUBI}	UNCK IN to IR ↑ (bubble-back time)		8		214	290		255	400	ns
t_{BUBC}	UNCK IN to UNCK OUT ↓ (bubble-back time)		8		226	290		270	400	ns

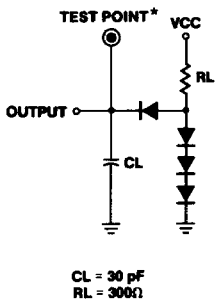
↓ Arrow indicates that it is referenced to the HIGH-to-LOW transition.

** 16th word only.

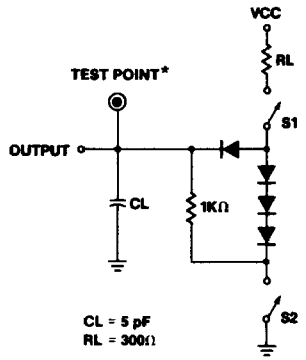
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225A MIN	74S225A TYP	74S225A MAX	74S225 MIN	74S225 TYP	74S225 MAX	UNIT
t_{PHZ}	Output disable delay, $\overline{OE}$ to Q_i, C_L = 5 pF	1		8	25		10	25	ns
t_{PLZ}				18	25				
t_{PZL}	Output enable delay, $\overline{OE}$ to Q_i, C_L = 5 pF	1		19	40		25	40	ns
t_{PZH}				23	40				

Test Load for Bi-State Output



Test Load for Three-State Output



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse Amplitude = 3.0 V
Input Rise and Fall Time (15%–90%) = 2.5 ns
Measurements made at 1.5 V

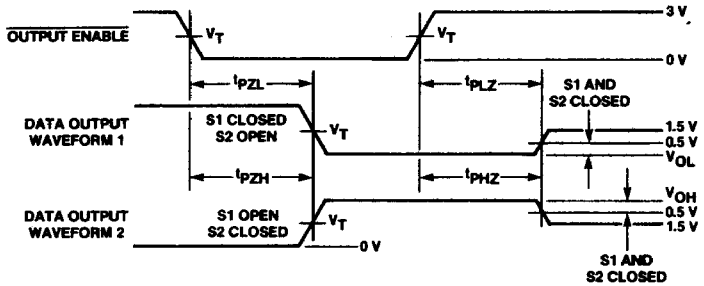


Figure 1. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled.

Waveform 2 is for an output with internal conditions such that the output is high

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8	V
V_{IH}	High-level input voltage					2.0			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL1}	Low-level input current	D_0–D_4	V_{CC} = MAX	V_I = 0.5 V				−1	mA
I_{IL2}		All others						−.25	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V	Data inputs			40	μA
					Others			25	
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage*		V_{CC} = MIN	I_{OL} = 16 mA (Data outputs)				0.5	V
				I_{OL} = 8 mA (All others)					
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −6.5 mA (Data outputs)		2.4			V
				I_{OH} = −3.2 mA (All others)					
I_{OS}	Output short-circuit current**		V_{CC} = MAX	V_O = 0 V		−30		−100	mA
I_{HZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V				50	μA
I_{LZ}			V_{CC} = MAX	V_O = 0.5 V				−50	μA
I_{CC}	Supply current		V_{CC} = MAX	Inputs low, All outputs open	74S225		80	120	mA
					74S225A		80	125	

* To measure V_{OL} on Pin 3, force 10 V on Pin 9 (Extended Testability).

** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Functional Description

Data Input

After power up the CLEAR is pulsed low (Figure 5) to prepare the FIFO to accept data in the first location. Clear must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH, the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when both Load Clocks (CLK A and CLK B) are brought HIGH. The CLK A HIGH and CLK B HIGH signal causes the IR and UNCK OUT to pulse LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{RIP} defines the time required for the first data to travel from input to the output of a previously empty device. When the sixteenth word is clocked into the device, the memory is full (sixteen words) and IR remains low. The Unload Clock Output is provided chiefly for use in cascading devices to extend FIFO depth (Figure 9). When Input Ready is Low, do not attempt to shift-in new data.

Data Output

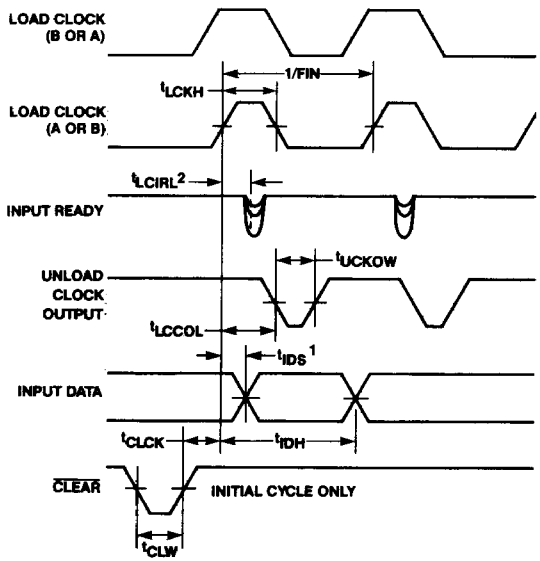
Data is read from the Q_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Unload Clock Input (UNCK IN) LOW. A LOW signal at UNCK IN causes the OR to go LOW. Valid data is maintained while the UNCK IN is LOW. When UNCK IN is brought HIGH the upstream data, provided that stage has valid data, is shifted to the output stage.

When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data remains valid for the last word.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BUBI}) or completely empty (Output Ready stays LOW for at least t_{RIP}).

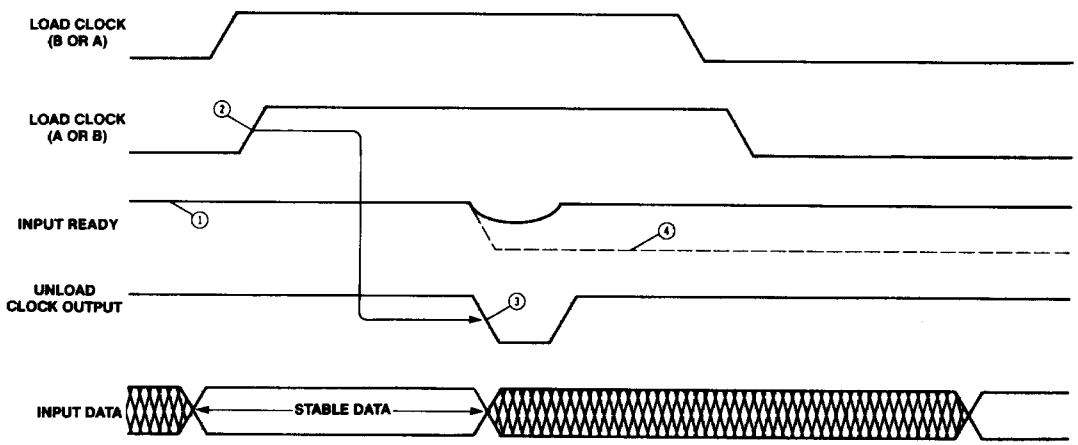
AC Test and High-Speed App. Notes

Since the FIFO is a high-speed device, care must be exercised in the design of the hardware and the timing utilized within the PC board design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Load Clocks (A, B) — Unload Clock Output-Input Ready combination, as well as the Unload Clock Input-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Load Clock pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or affected by ($\overline{CLR}$), the LOAD-CK activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (t_{IDH}) and the next activity of Input Ready (t_{LCIRL}) to be extended relative to Load Clock (A or B) going HIGH.



NOTES: 1. Permissible negative setup time for input data
2. Measure t_{LCIRL} for 16th input word only

Figure 2. Input Timing



NOTES: 1. Input Ready HIGH indicates space is available and a Load Clock (A and B) pulse may be applied.
2. Input Data is loaded into the first word.
3. Unload Clock Output pulses indicating the first word is full and the Data from the first word is released for "fall-through" to second word.
4. If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains LOW.

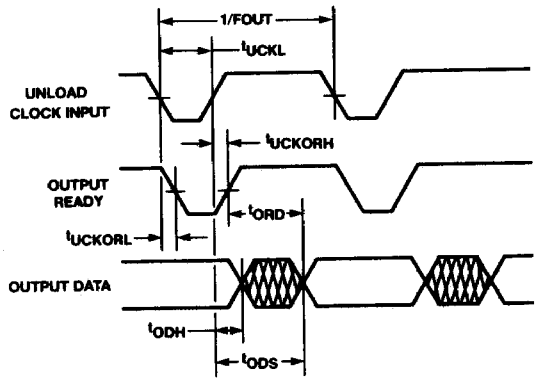
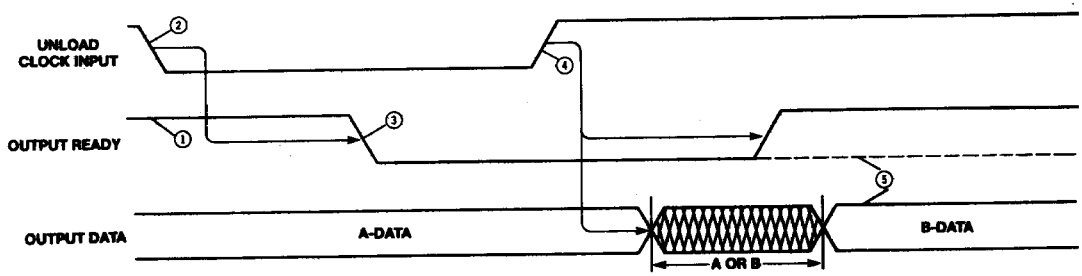


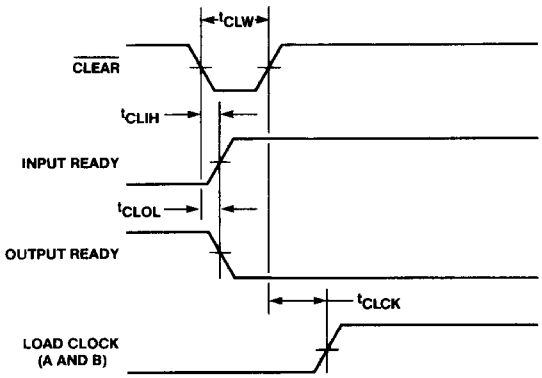
Figure 4. Output Timing



NOTES: 1. Output Ready HIGH indicates that data is available and an Unload Clock Input pulse may be applied.
2. Unload Clock Input goes LOW creating an empty position at word 16 for word 15 to "fall-through" to.
3. Output Ready goes LOW.
4. Unload Clock Input goes HIGH, causing Output Ready to go HIGH, indicating that new data (B) is now available at the FIFO outputs.
5. If the FIFO has only one word loaded (A-DATA), then Output Ready stays LOW and the A-DATA remains on the outputs.

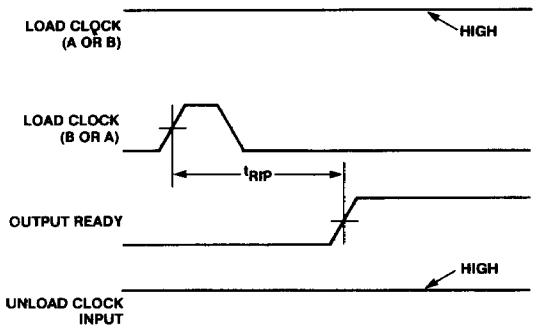
NOTE: Assume FIFO initially contains at least two words.

Figure 5. The Mechanism of Shifting Data Out of the FIFO



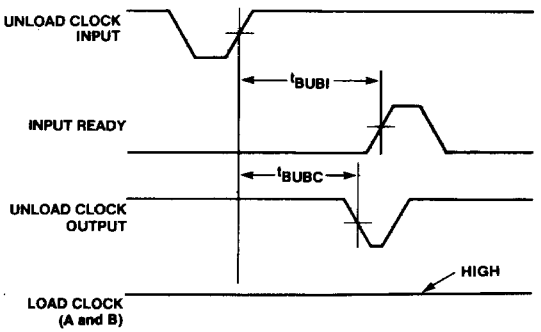
NOTE: Assume FIFO is full before $\overline{\text{CLEAR}}$ goes active.

Figure 6. Clear Timing



NOTES: 1. FIFO is initially empty.
2. Unload Clock Input and one Load Clock held HIGH throughout.

Figure 7. t_{RIP} Specifications



NOTES: 1. FIFO is initially full.
2. Load Clock (A and B) held HIGH throughout.

Figure 8. t_{BUBI}, t_{BUBC} Specifications

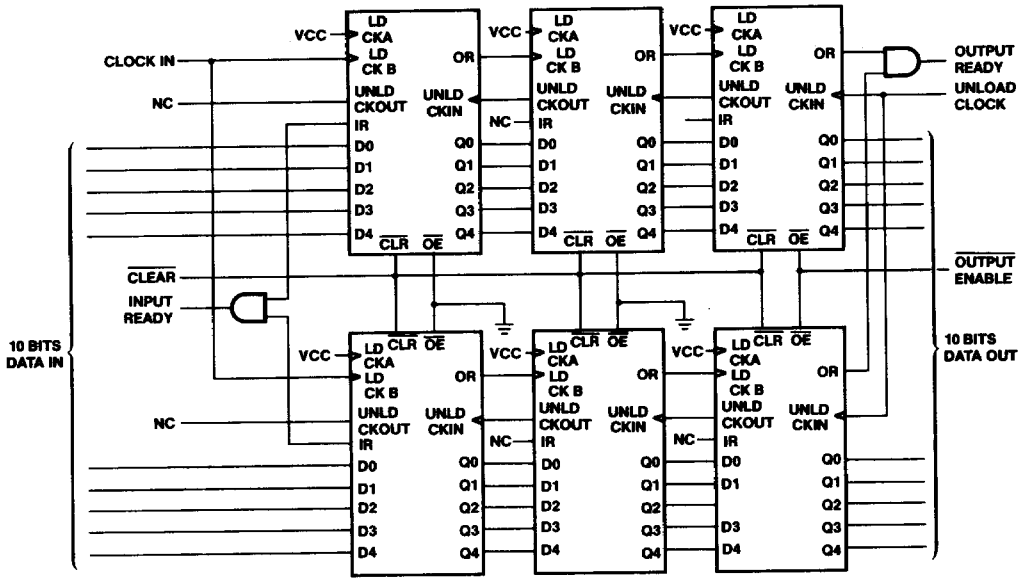


Figure 9. 48x10 FIFO with 74S225/A