

Part 1 Introduction to the MC68183

Refer to Section 1.1 for information on this data sheet and on the MC68183.

1.1 Content Organization

This section outlines the information contained in this document.

Part 1, “Introduction to the MC68183”	1-2
1.1, “Content Organization”	1-2
1.2, “Data Conventions”	1-3
1.3, “Features”	1-4
1.4, “Summary of Changes”	1-4
1.5, “Additional Support”	1-5
1.6, “Documentation”	1-5
1.7, “Ordering Information”	1-6
Part 2, “Signal/Connection Descriptions”	2-1
2.1, “Signal Groupings”	2-1
2.2, “Power Input and Monitoring”	2-1
2.3, “Processor Clock”	2-2
2.4, “Reset”	2-2
2.5, “Current Symbol Inputs”	2-2
2.6, “Serial Peripheral Interface”	2-3
2.7, “Receiver Control Lines”	2-3
Part 3, “Specifications”	3-1
3.1, “Maximum Ratings”	3-1
3.2, “Thermal Characteristics”	3-1
3.3, “DC Electrical Characteristics”	3-2
3.4, “AC Electrical Characteristics”	3-3
3.5, “Initialization Timing”	3-3
3.6, “Reset Timing”	3-4
3.7, “Serial Peripheral Interface Timing”	3-4
Part 4, “Pin-Out and Package Information”	4-1
4.1, “TQFP Package Description”	4-1
4.2, “Ordering Drawings”	4-4
Part 5, “Design Considerations”	5-1
5.1, “Thermal Design Considerations”	5-1
5.2, “Application Design Considerations”	5-2
Appendix A, “FLEX Overview”	A-5
A.1, “FLEX Signal Structure”	A-5
A.2, “FLEX Frame Structure”	A-5
A.3, “FLEX Message Word Definitions”	A-9
Appendix B, “SPI Packets”	B-1
B.1, “Packet Communication Initiated by the Host”	B-1
B.2, “Packet Communication Initiated by MC68183”	B-2
B.3, “Host-to-Decoder Packet Map”	B-3
B.4, “Decoder-to-Host Packet Map”	B-4

Appendix C, “Host-to-Decoder Packet Descriptions”	C-1
C.1, “Checksum Packet”	C-1
C.2, “Configuration Packet”	C-3
C.3, “Control Packet”	C-5
C.4, “All Frame Mode Packet”	C-7
C.5, “Operator Messaging Address Enable Packet”	C-11
C.6, “Roaming Control Packet”	C-8
C.7, “Timing Control Packet”	C-10
C.8, “Receiver Line Control Packet”	C-11
C.9, “Receiver Control Configuration Packets”	C-12
C.10, “Receiver-Off Setting Packet”	C-12
C.11, “Frame Assignment Packets”	C-15
C.12, “User Address Enable Packet”	C-16
C.13, “User Address Assignment Packets”	C-17
Appendix D, “Decoder-to-Host Packet Descriptions”	D-1
D.1, “Block Information Word Packet”	D-1
D.2, “Address Packet”	D-3
D.3, “Vector Packet”	D-4
D.4, “Message Packet”	D-8
D.5, “Roaming Status Packet”	D-9
D.6, “Receiver Shut-Down Packet”	D-10
D.7, “Status Packet”	D-11
D.8, “Part ID Packet”	D-13
Appendix E, “Application Notes”	E-1
E.1, “Receiver Control”	E-1
E.2, “Receiver Settings at Reset”	E-1
E.3, “Message Building”	E-4
E.4, “Building a Fragmented Message”	E-6
E.5, “Operation of a Temporary Address”	E-9
E.6, “Using the Receiver Shut-Down Packet”	E-10

1.2 Data Conventions

This data sheet uses the following conventions:

- $\overline{\text{OVERBAR}}$: used to indicate a signal that is active when pulled low (e.g., “ $\overline{\text{RESET}}$ ”).
- “Asserted” means that a high true signal (i.e., an active high) is high or that a low true signal (i.e., an active low) is low.
- “Deasserted” means that a high true signal is low or that a low true signal is high.

Please refer to the examples in Table 1-1.

Table 1-1. Data Conventions

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	$V_{\text{IL}}/V_{\text{OL}}$
PIN	False	Deasserted	$V_{\text{IH}}/V_{\text{OH}}$

Table 1-1. Data Conventions (Continued)

Signal/Symbol	Logic State	Signal State	Voltage
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1.3 Features

The following list describes the features of the MC68183:

- FLEX paging protocol signal processor
- 16 programmable user address words
- 16 temporary addresses
- 16 operator-messaging addresses
- 1600, 3200, and 6400 bits-per-second (bps) decoding
- Any-phase or single-phase decoding
- Uses standard serial peripheral interface (SPI) in slave mode
- Allows low-current STOP mode operation of host processor
- Highly programmable receiver control
- Real-time clock time base
- FLEX message fragmentation and group messaging support
- Real-time clock over-the-air update support
- Compatible with synthesized receivers
- SSID and NID roaming support
- Low battery indication (external detector)
- 32-pin TQFP package
- Backward-compatible to the standard and roaming FLEXchip ICs
- Internal demodulator and data slicer
- Improved battery savings via partial address correlation and intermittent receiver clock
- Full support for revision G1.9 of the FLEX protocol

1.4 Summary of Changes

The following list summarizes the differences between the MC68181 and the MC68183. The two are very similar in operation and configuration; in fact, the MC68183's default mode of operation causes it to operate as a MC68181. Current users of the MC68181 should refer to the following list for a detailed understanding of the differences between the products.

- The MC68183 has an internal digital demodulator that accepts a 455 kHz or 140 kHz limited IF signal on the S0/IFIN pin. A 160 kHz crystal must be used, and EXTS0 and EXTS1 pins are tri-stated if the demodulator is enabled.

- When the internal digital demodulator is enabled, the CLKOUT can be programmed as either 38.4 kHz or 40 kHz.
- The MC68183 supports partial address correlation, which allows the FLEXchip II to shut down before the end of the last FLEX block containing an address, if no addresses match.
- The MC68183 supports an intermittent clock output that drives the CLKOUT pin low whenever the receiver is shut down.
- The configuration packet from the host MCU contains the following four new bits:
 - IDE enables the digital demodulator.
 - DEC selects the CLKOUT frequency when the digital demodulator is enabled.
 - PCE enables partial address correlation.
 - ICO enables the intermittent clock function.
- The part ID for the MC68183 is \$00 03 09
- Improvements to the host-to-decoder packets include
 - The MC68183 is sent an EAE bit in its control packet which can enable the MC68183 to control the end of address bit in its status packet.
 - The host MCU can send an operator messaging address enable packet that enables built-in FLEX operator addresses.
 - The host MCU can send a roaming control packet, allowing the MC68183 to implement a roaming pager.
 - The host MCU can send a timing control packet, allowing control of the system timing when the MC68183 is in asynchronous mode.
- Improvements to the decoder-to-host packets
 - Block information words have been added for system message and time zone information.
 - The MC68183 can send a roaming status packet, which can then be sent to the host MCU.
 - The MC68183 can send a receiver shutdown packet to inform the host MCU that the receiver is off.
 - The MC68183 sends an EA bit in its status packet indicating that the last address in a frame has been detected.

1.5 Additional Support

FLEX system software from Motorola is a family of software components for building world-class products incorporating messaging capabilities. FLEX Stack Software is specifically designed to support the MC68183. The software runs on a product's host processor and controls communication with the MC68183, acquisition of the proper FLEX channel, and full interpretation of the code-words that the MC68183 passes to the host. For information on how to obtain FLEX Stack Software, contact the Motorola wireless semiconductor help desk at the following address:

<http://www.mot.com/SPS/WIRELESS/download/>

1.6 Documentation

This is the primary support document for the MC68183. All Motorola documentation is available from the following sources:

- A local Motorola distributor

- A Motorola semiconductor sales office
- A Motorola literature distribution center

The source of all the latest information is the Motorola wireless semiconductor home page, which can be reached on the Internet at the following addresses:

<http://www.mot.com/flex> (FLEX)

<http://motorola.com/wireless-semi> (Wireless Semiconductor)

See the back cover for additional information.

1.7 Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and to place an order.

Table 1-2. Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (kHz)	Order Number
MC68183	2/3 V	Thin Quad Flat Pack (TQFP)	32	76.8 or 160	MC68183FA

Part 2 Signal/Connection Descriptions

This section presents descriptions of the MC68183 signals and their connections.

2.1 Signal Groupings

The input and output signals of the MC68183 are organized into six functional groups, as shown in Table 2-1 and illustrated in Figure 2-1.

Table 2-1. MC68183 Functional Signal Groupings

Functional Group	Number of Signals	Detailed Description
Power Input and Monitoring	7	Figure 2-2
Processor Clock	5	Figure 2-3
Reset	1	Figure 2-4
Current Symbol Inputs	2	Figure 2-5
Serial Peripheral Interface (SPI)	5	Figure 2-6
Receiver Control Lines	8	Figure 2-7

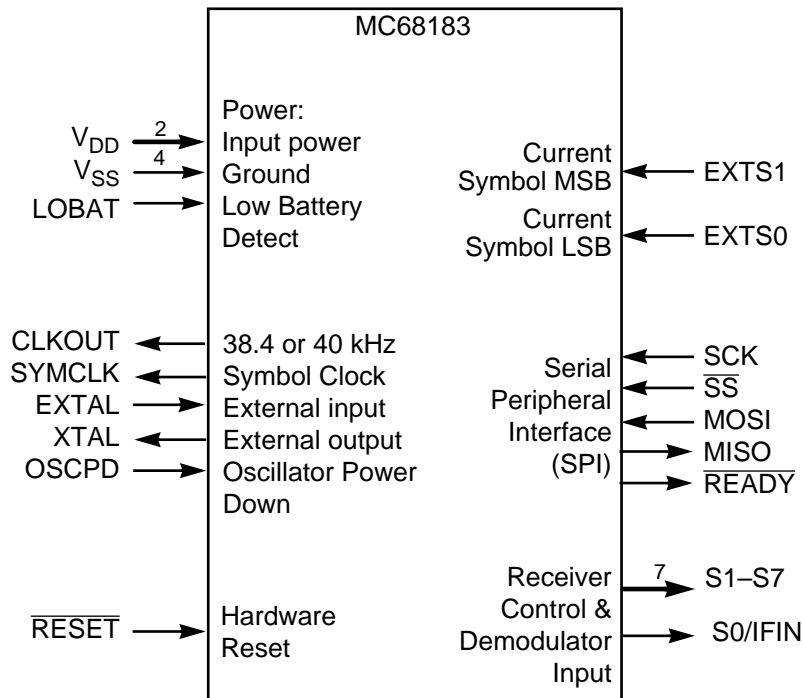


Figure 2-1. Signals Identified by Functional Group

2.2 Power Input and Monitoring

Refer to Table 2-2 for a description of the MC68183 power input and monitoring signals.

Table 2-2. Power Input, Monitoring, and Control Signals

Power Name	Description
V _{DD}	Power —V _{DD} is the input power for the MC68183.
V _{SS}	Ground —V _{SS} is ground connection for the MC68183.
LOBAT	Low Battery —LOBAT is an input signal to indicate to the MC68183 when external battery power is going low. (An external voltage sensing circuit is required.)

2.3 Processor Clock

The MC68183 processor clock signals are described in Table 2-3.

Table 2-3. Processor Clock Signals

Signal Name	Type	State during Reset	Signal Description
CLKOUT	Output	Indeterminate	Clock Output —Programmable as a 38.4 or 40 kHz clock output (derived from oscillator).
SYMCLK	Output	Indeterminate	Recovered Symbol Clock —Data is synchronized to the internal clock and this recovered clock output enhances lock-on capability by reducing jitter from cable-induced noise.
EXTAL	Input	Input	External Clock/Crystal Input —EXTAL interfaces the internal crystal oscillator input to a 76.8 kHz or 160 kHz crystal input or other external input clock.
XTAL	Output	Indeterminate	External Clock/Crystal Output —This is typically a 76.8 kHz or 160 KHz clock output.
OSCPD	Input	Input	Oscillator Power Down —This input determines whether the internal oscillator is used. Connect this pin to V _{SS} when using the 76.8 kHz crystal input. Connect this pin to V _{DD} when using an external input clock signal.

2.4 Reset

Table 2-4 describes the MC68183 test and reset signals.

Table 2-4. Test and Reset Signals

Signal Name	Type	State During Reset	Signal Description
RESET	Input	Input	Reset —This input is a direct hardware reset on the MC68183. When RESET is asserted low, the MC68183 is initialized and placed in the Reset state.

2.5 Current Symbol Inputs

Interrupt and mode control signals are described in Table 2-5.

Table 2-5. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
EXTS1	Input	Input	External Symbol 1 —This is the most significant bit (MSB) of the symbol being tested.
EXTS0	Input	Input	External Symbol 0 —This is the least significant bit (LSB) of the symbol being tested.

2.6 Serial Peripheral Interface

Refer to Table 2-6 for a description of the MC68183 SPI signals.

Table 2-6. SPI Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input	Input	SPI Serial Clock —The SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if the slave select (\overline{SS}) signal is not asserted.
\overline{SS}	Input	Input	SPI Slave Select —This signal is used to enable the SPI slave for transfer.
MOSI	Input	Input	SPI Master-Out-Slave-In —Because the MC68183 is always a slave device, this is the data input for SPI communications. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data.
MISO	Output	Tri-stated	SPI Master-In-Slave-Out —Because the MC68183 is always a slave device, this is the data output for SPI communications. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data.
\overline{READY}	Output	Output, driven high	SPI Ready —This signal is driven low when the MC68183 is ready for an SPI packet.

2.7 Receiver Control Lines

MC68183 receiver control lines signals are described in Table 2-7.

Table 2-7. Receiver Control Lines

Signal Name	Signal Type	State during Reset	Signal Description
S0/IFIN	Output/Input	Tri-stated/Input	S0 - This signal is a receiver control output when the IDE bit is clear (i.e., the internal demodulator is disabled). IFIN - This signal is a limited IF input when the IDE bit is set (i.e. the internal demodulator is enabled)
S1–S7	Output	Tri-stated	Control Line 1–Control Line 7 —These signals are the seven additional receiver control lines.

Part 3 Specifications

The MC68183 is fabricated in high-density CMOS with transistor-transistor-logic-compatible (TTL) inputs and outputs.

3.1 Maximum Ratings

Refer to Table 3-1 for a listing of the MC68183's maximum ratings.

Warning:

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or VDD).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst-case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 3-1. Maximum Ratings

Rating	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.5	3.6	V
All input voltages	V_{IN}	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Current drain per pin excluding V_{DD} and V_{SS}	I	—	10	mA
Operating temperature range	T_A	-30	+85	°C
Storage temperature	T_{STG}	-65	+150	°C

3.2 Thermal Characteristics

The MC68183's thermal characteristics are provided in Table 3-2.

Table 3-2. Thermal Characteristics

Characteristic	Symbol	TQFP Value	Unit
Junction-to-ambient thermal resistance ¹	$R_{\theta JA}$ or θ_{JA}	95	°C/W
Thermal characterization parameter	Ψ_{JT}	21	°C/W

1. Junction-to-ambient thermal resistance is based on measurements on a horizontal, single-sided printed circuit board per SEMI G38-87 in natural convection. (SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111) Values were measured with the parts mounted on thermal test boards meeting the specification EIA/JESD51-3.

3.3 DC Electrical Characteristics

Refer to Table 3-3 for a complete listing of MC68183 dc electrical characteristics.

Table 3-3. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	1.8	3.3	3.6	V
Input voltage	V_I	0	—	V_{DD}	V
Output voltage ¹	V_O	0	—	V_{DD}	V
Input high voltage RESET, \overline{SS} , SCK, MOSI All other inputs	V_{IH}	$0.75V_{DD}$ $0.7 V_{DD}$	— —	— —	V V
Input low voltage	V_{IL}	—	—	$0.2V_{DD}$	V
Input transition (rise and fall) time	t_t	0	—	25	ns
Input leakage current	I_{IN}	-0.25	—	0.25	μA
High impedance (off-state) input current (@ 1.44 V / 0.3 V)	I_{TSI}	-10	—	+10	μA
Output high voltage ($I_{OH} = -1.0$ mA)	V_{OH}	$0.8 V_{DD}$	—	—	V
Output low voltage ($I_{OL} = 2.8$ mA)	V_{OL}	—	—	0.3	V
Internal supply current ²	I_{DD}	—	100	—	μA
Input capacitance	C_{IN}	—	10	—	pF
Virtual junction temperature	T_j	-30	25	150	$^{\circ}C$
Positive-going threshold voltage ^{3,4}	V_{IT+}	—	—	$0.7V_{DD}$	V
Negative-going threshold voltage ^{3,4}	V_{IT-}	$0.2V_{DD}$	—	—	V
Hysteresis ($V_{IT+} - V_{IT-}$) ³	V_{hys}	$0.1V_{DD}$	—	$0.3V_{DD}$	V
3-state-output Hi-Z current ⁵	I_{OZ}	—	—	+/- 10	μA
Lower-level input current ⁶	I_{IL}	—	—	-1	μA
High-level input current ⁷	I_{IH}	—	—	1	μA

1. Applies to output buffers.
2. This value is for static I_{DD} .
3. Applies to input and bidirectional buffers with hysteresis.
4. Test condition = CMOS compatible.
5. 3-state or open-drain output must be in the high-impedance mode.
6. Specifications only apply with pull-up terminator turned off.
7. Specifications only apply with pull-down terminator turned off.

3.4 AC Electrical Characteristics

The timing wave-forms in the ac electrical characteristics are tested with a V_{IL} maximum of $0.2 \times V_{DD}$ in V and a V_{IH} minimum of $0.7 \times V_{DD}$ in V for all inputs. AC timing specifications referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. MC68183 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at $0.3 \times V_{DD}$ in V and $0.6 \times V_{DD}$ in V, respectively.

Note: All ac timings have been fully simulated during the design phase. The following specifications are guaranteed by design.

3.5 Initialization Timing

For the MC68183, $V_{DD} = 1.8$ to 3.6 V; $T_A = -30$ to $+85^\circ\text{C}$. Table 3-4 gives initialization timing information for the MC68183, and Figure 3-1 diagrams the start-up timing.

Table 3-4. Initialization Timing

Characteristic	Conditions	Symbol	Min	Max	Unit
Oscillator start-up time	—	t_{START}	—	5	sec
RESET hold time	—	t_{RESET}	200	—	ns
RESET high to $\overline{\text{READY}}$ low	—	t_{RHRL}	—	1	sec
Oscillator warmed up to $\overline{\text{READY}}$ low	$C_L = 50\text{pf}$	t_{OWRL}	—	1	sec

Note: From power-up, the oscillator start-up time can impact the availability and period of clock strobes. This can affect the actual RESET high to $\overline{\text{READY}}$ low timing.

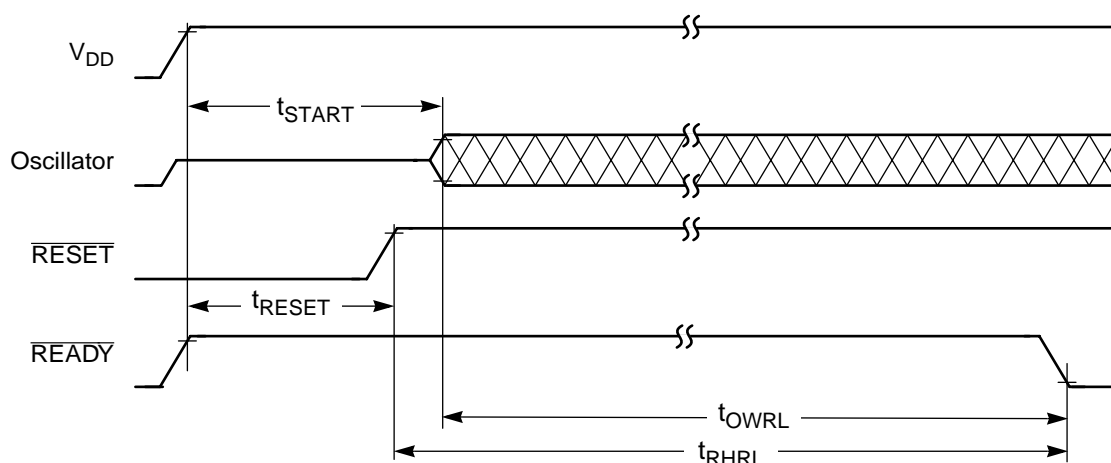


Figure 3-1. Start-Up Timing

3.6 Reset Timing

For the MC68183, $V_{DD} = 1.8$ to 3.6 V; $T_A = -30$ to 85°C . Refer to Table 3-5 for reset timing information, and consult Figure 3-2 for the reset timing diagram.

Table 3-5. Reset Timing

Characteristic	Conditions	Symbol	Min	Max	Unit
RESET pulse width	—	t_{RL}	200	—	ns
RESET low to READY high	—	t_{RLRH}	—	200	ns
RESET high to READY low	Requires stable clock source	t_{RHRL}	—	1	sec



Figure 3-2. Reset Timing

3.7 Serial Peripheral Interface Timing

For the MC68183, $V_{DD} = 1.8$ to 3.6 V; $T_A = -30$ to $+85^\circ\text{C}$. Refer to Table 3-6 for SPI timing information. Figure 3-3 diagrams SPI timing.

Table 3-6. SPI Timing

Characteristic	Conditions	Symbol	Min	Max	Unit
Operating frequency	—	f_{OP}	0	1	MHz
Cycle time	—	t_{CYC}	1000	—	ns
Select lead time	—	t_{LEAD1}	200	—	ns
Deselect lag time	—	t_{LAG1}	200	—	ns
Select-to-ready time	Previous packet did not program an address word; $C_L = 50$ pf	t_{RDY}	—	80	μs
Select-to-ready time	Previous packet programmed an address word; $C_L = 50$ pf	t_{RDY}	—	420	μs
Ready high time	—	t_{RH}	50	—	μs

Table 3-6. SPI Timing (Continued)

Characteristic	Conditions	Symbol	Min	Max	Unit
Ready lead time	—	t_{LEAD2}	200	—	ns
Not ready lag time	$C_L = 50\text{pf}$	t_{LAG2}	—	200	ns
MOSI data setup time	—	t_{SU}	200	—	ns
MOSI data hold time	—	t_{HI}	200	—	ns
MISO access time	$C_L = 50\text{pf}$	t_{AC}	0	200	ns
MISO disable time	—	t_{DIS}	—	300	ns
MISO data valid time	$C_L = 50\text{pf}$	t_V	—	200	ns
MISO data hold time	—	t_{HO}	0	—	ns
\overline{SS} high time	—	t_{SSH}	200	—	ns
SCK high time	—	t_{SCKH}	300	—	ns
SCK low time	—	t_{SCKL}	300	—	ns
SCK rise time	20% to 70% V_{DD}	t_R		1	μs
SCK fall time	20% to 70% V_{DD}	t_F		1	μs

Note: When the host reprograms an address word with a host-to-FLEXchip packet ID > 127 (decimal), there may be an added delay before FLEXchip is ready for another packet.

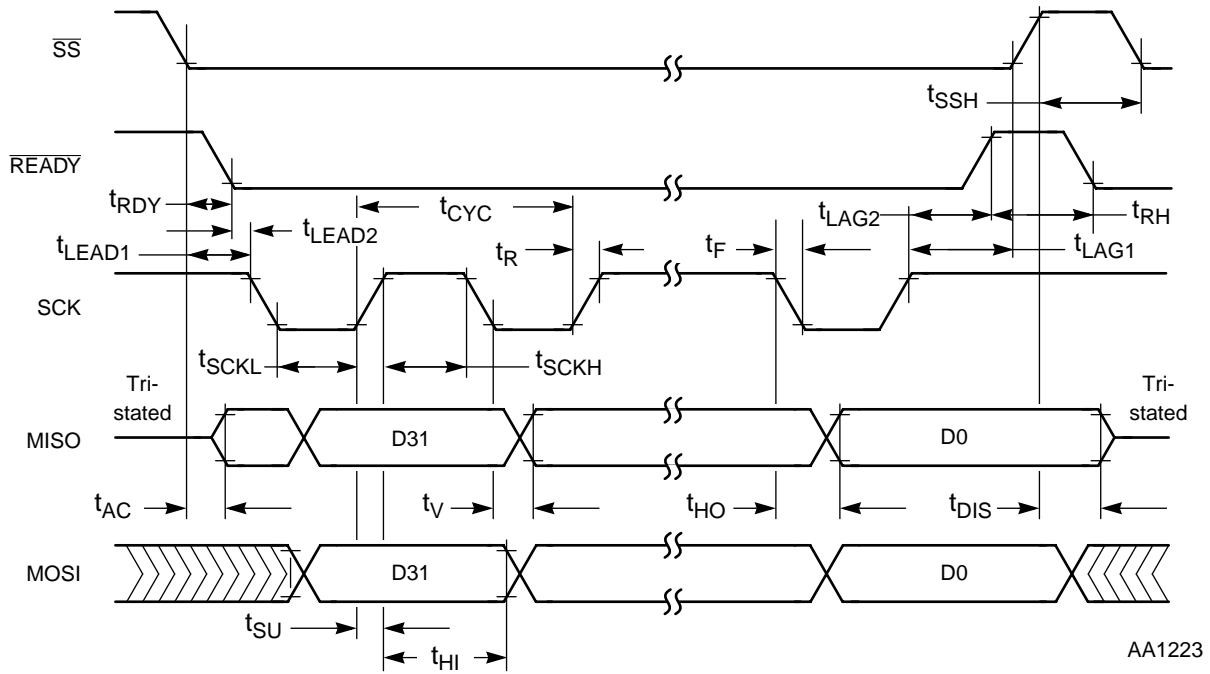


Figure 3-3. SPI Timing

Part 4 Pin-Out and Package Information

This section provides information about the available packages for this product, including diagrams of the package pinouts and tables describing how the signals described in Part 2 are allocated. The MC68183 is available in a 32-pin thin quad flat-pack (TQFP) package.

4.1 TQFP Package Description

The TQFP package is shown in Figure 4-1 with its pin-outs. Table 4-1 correlates pin numbers with signal names, and Table 4-2 lists the MC68183 signals by name.

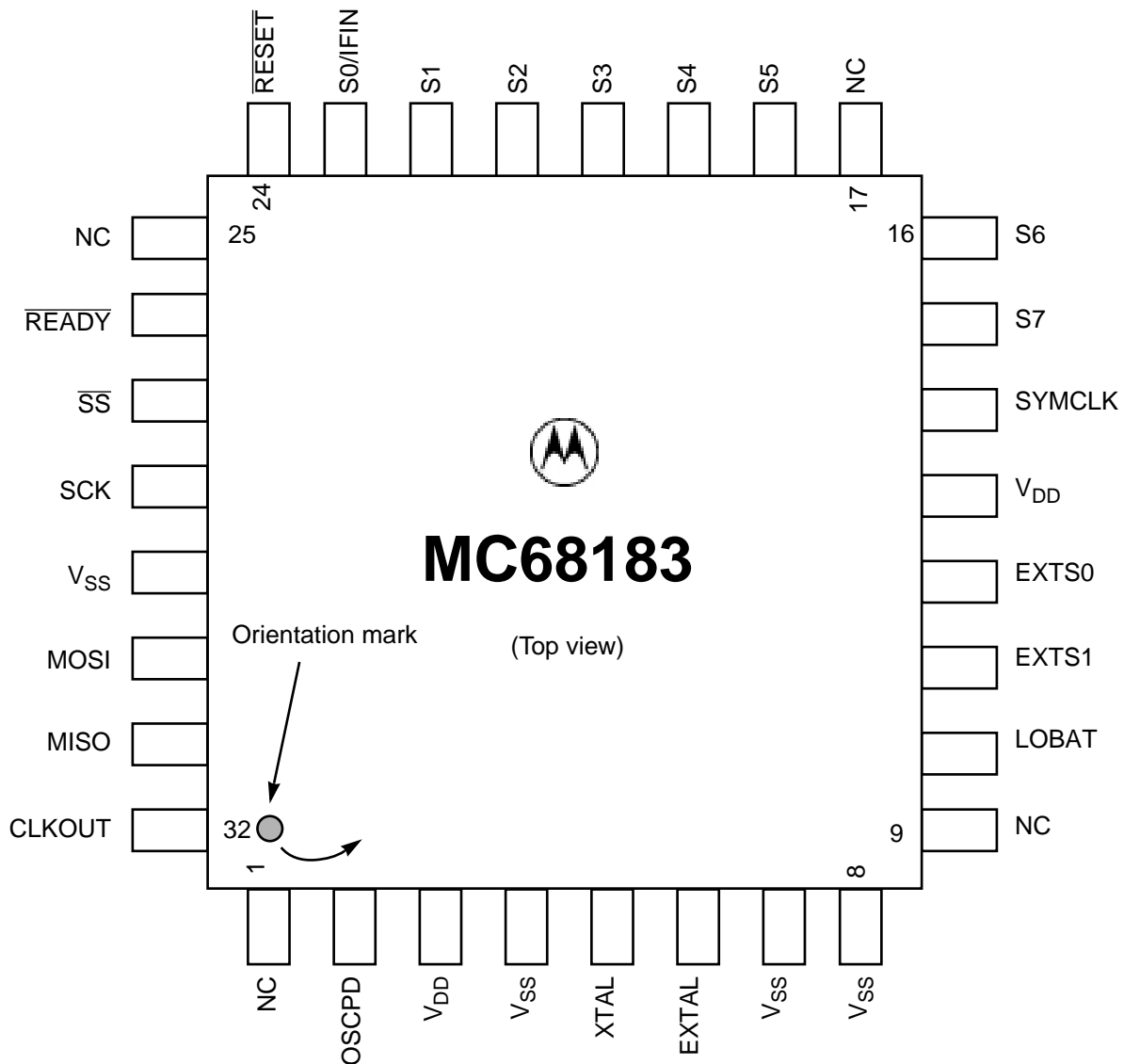


Figure 4-1. MC68183 Thin Quad Flat Pack (TQFP), Top View

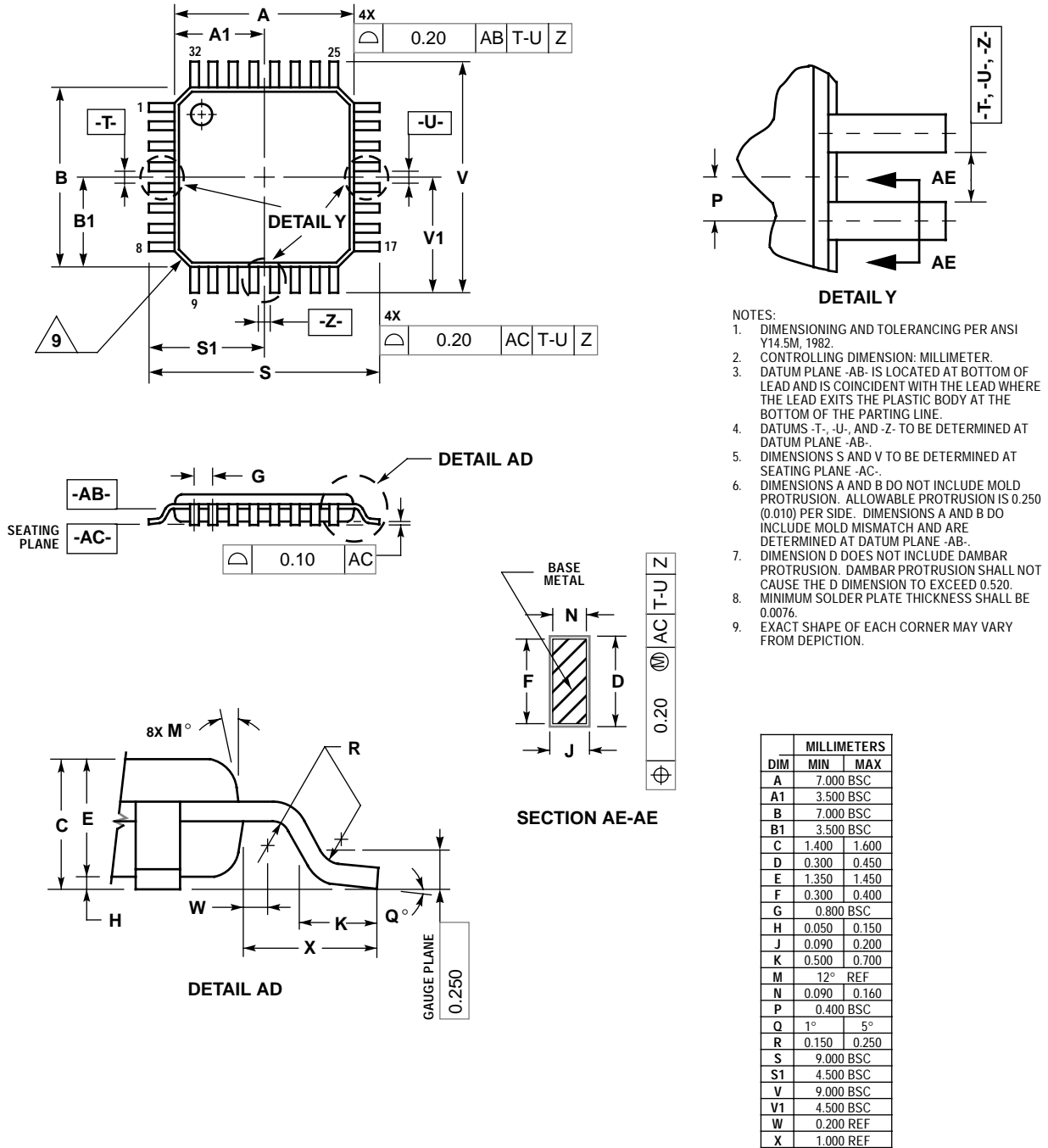
Table 4-1. Signal by Pin Number

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	NC ¹	9	NC ¹	17	NC ¹	25	NC ¹
2	OSCPD	10	LOBAT	18	S5	26	READY
3	V _{DD}	11	EXTS1	19	S4	27	SS
4	V _{SS} ²	12	EXTS0	20	S3	28	SCK
5	XTAL	13	V _{DD}	21	S2	29	V _{SS} ²
6	EXTAL	14	SYMCLK	22	S1	30	MOSI
7	V _{SS} ²	15	S7	23	S0/IFIN	31	MISO
8	V _{SS} ²	16	S6	24	RESET	32	CLKOUT

1. NC indicates reserved pins. These pins must not be connected to any external line.
2. To ensure proper chip operation, all V_{SS} pins must be connected to GND.

Table 4-2. Signal by Name

Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
CLKOUT	32	NC	9	S2	21	SYMCLK	14
EXTAL	6	NC	17	S3	20	V _{DD}	3
EXTS0	12	NC	25	S4	19	V _{DD}	13
EXTS1	11	OSCPD	2	S5	18	V _{SS}	4
LOBAT	10	READY	26	S6	16	V _{SS}	7
MISO	31	RESET	24	S7	15	V _{SS}	8
MOSI	30	S0/IFIN	23	SCK	28	V _{SS}	29
NC	1	S1	22	SS	27	XTAL	5



**CASE 873A-02
ISSUE A**

DATE 12/16/93

Figure 4-2. 32-Pin Thin Quad Flat Pack (TQFP) Mechanical Information

4.2 Ordering Drawings

Complete mechanical information on MC68183 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number for facsimile:

(602) 244-6591

The Mfax automated system requests the following information:

- The receiving facsimile telephone number, including area code or country code
- The caller's personal identification number (PIN)

Note: For first-time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number. The following types of information may be requested:

- Instructions for using the system
- A literature order form
- Specific part technical information or data sheets
- Other information described by the system messages

A total of three documents may be ordered per call.

The MC68183 32-pin TQFP package mechanical drawing is referenced as 873A-02.

Part 5 Design Considerations

In this section, thermal and application design considerations are described.

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J , can be obtained in °C from the equation

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where

T_A = ambient temperature °C

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W

P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W

$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W

$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or otherwise change the thermal dissipation capability of the area surrounding the device on a printed circuit board.

This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the printed circuit board to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system-level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages:

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature.

Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT} , has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

5.2 Application Design Considerations

The operation of the MC68183 is determined by its mode of operation. While working in default mode, it operates identically to the MC68181. Figure 5-1 shows a block diagram of a system designed using the MC68183. When connected to a receiver capable of converting a 4-level audio signal to a 2-bit digital signal, the MC68183 provides eight receiver control lines used for warming up and shutting down a receiver in stages.

The MC68183 offers dual bandwidth control for two post-detection filter bandwidths allowing reception of two symbol rates of the FLEX signal. Other features include the ability to detect a low battery signal during receiver control sequences and the use of an industry standard SPI interface for communication with a host MCU. The MC68183 provides a 38.4 kHz clock output capable of driving other devices. A 1-minute timer offers support for a time-of-day function on the host.

The MC68183 features internal demodulator that works with a limited (i.e., 1-bit digitized) 455 kHz or 140 kHz IF signal. When this mode of operation is selected via a command from the host, the IF signal from the receiver is input into the MC68183 via the S0/IFIN pin. When using the internal demodulator, the oscillator frequency (or external clock) must be 160 kHz. The CLKOUT signal can be programmed to be either a 38.4 kHz signal, created by fractionally dividing the oscillator clock, or a 40 kHz signal, created by dividing the oscillator clock by 4.

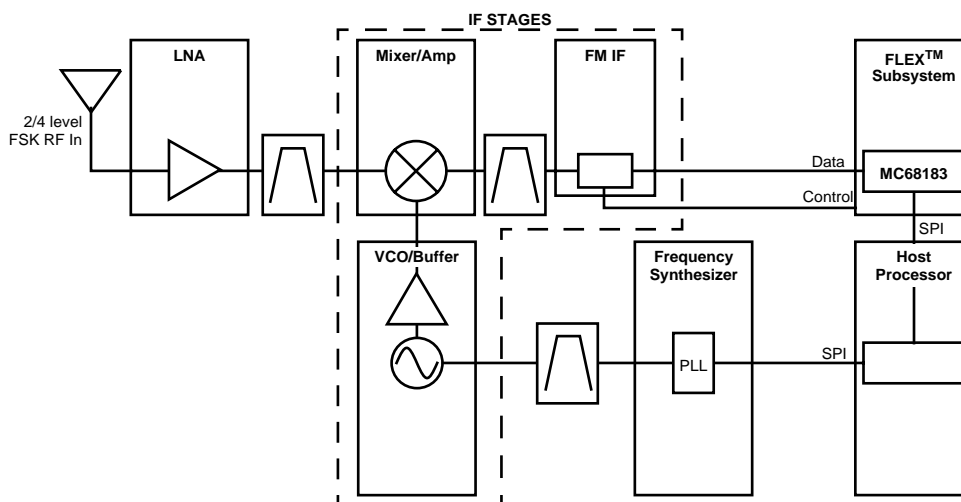
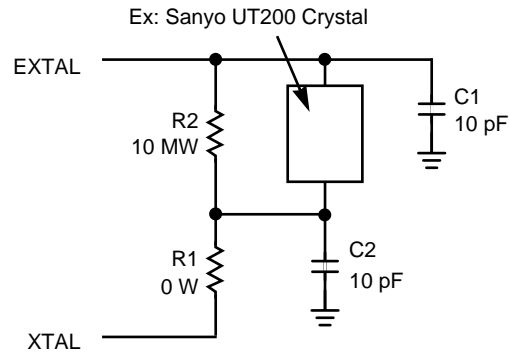


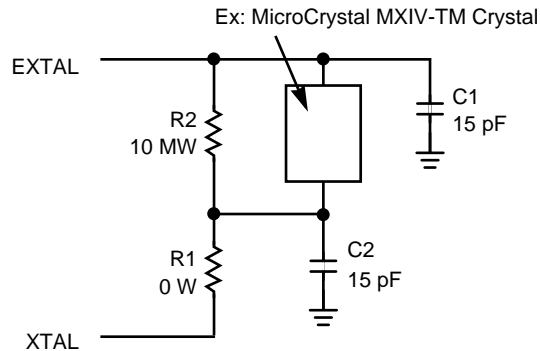
Figure 5-1. MC68183 System Block Diagram

Suggested crystal oscillator circuits for use with the MC68183 are shown below. Figure 5-2 shows a recommended circuit for a 76.8 kHz crystal input and Figure 5-3 shows the circuit for a 160kHz crystal input.



Note: R1 can be increased in size to be used as a current limiter, if needed.

Figure 5-2. Input Circuit for 76.8 kHz Crystal



Note: R1 can be increased in size to be used as a current limiter, if needed.

Figure 5-3. Input Circuit for a 160 kHz Crystal Output

Appendix A FLEX Overview

This appendix gives an overview of the FLEX protocol as it pertains to the MC68183. As this is only an overview (derived from Issue G1.9 of the FLEX protocol specification), the FLEX protocol specification prevails in case of contradiction.

A.1 FLEX Signal Structure

As shown in Figure A-1, a FLEX signal consists of a series of 4-minute cycles, each of 128 frames at 1.875 seconds per frame. The signal is transmitted on a radio channel. A pager may be assigned to process any number of these frames. Any unassigned frames are not processed, thus reducing power required for signal processing and extending battery life. If required, however, the pager may temporarily process more complex information. This temporary processing capability is possible because individual FLEX cycles can dynamically assign additional frames using collapse, fragmentation, temporary addressing, or carry-on information within the FLEX signal.

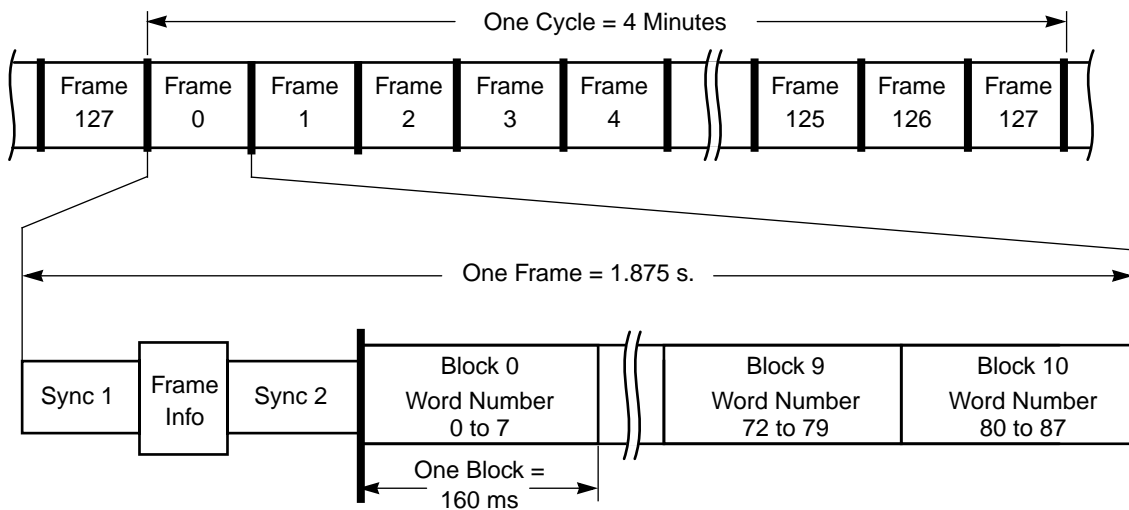


Figure A-1. FLEX Signal Structure

A.2 FLEX Frame Structure

Each FLEX frame consists of the following two elements:

- Synchronization portion.
- Data portion—11 data blocks lasting 160 milliseconds each.

A.2.1 Frame Synchronization Portion

The synchronization portion consists of the following elements:

- First synchronization signal at 1600 bps
- Frame information word, including
 - Frame number 0–127 (7 bits)
 - Cycle number 0–14 (4 bits)

- Second synchronization signal at the data rate of the interleaved portion.

A.2.1.1 First Synchronization Signal

The first synchronization signal is transmitted at 1600 bps and provides a signal to lock onto the specific frame.

A.2.1.2 Frame Information Word

The frame information word transmits 11 bits that are divided into a 7-bit frame number and a 4-bit cycle number. This allows the pager to identify the frame and the cycle in which it resides uniquely.

A.2.1.3 Second Synchronization Signal

The second synchronization signal indicates the rate at which the data portion is transmitted (i.e., 1600, 3200 or 6400 bits per second).

The 1600 bps rate is transmitted as a single phase of information (A), as shown in Figure A-2, at 1600 symbols per second using 2-level frequency shift keyed (FSK) modulation.

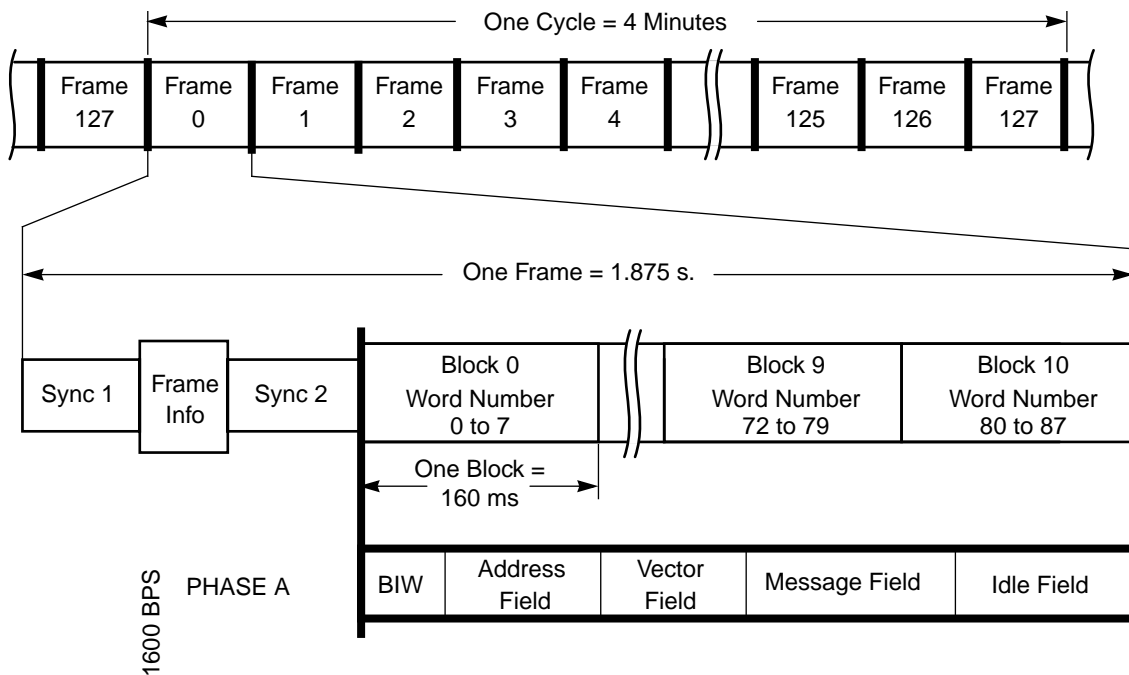


Figure A-2. FLEX Signal Structure for 1600 BPS

The 3200 bps rate is transmitted as two concurrent phases of information (A and C), as shown in Figure A-3, at either of the following data rates:

- 1600 symbols per second using 4-level FSK modulation, or
- 3200 symbols per second using 2-level FSK modulation.

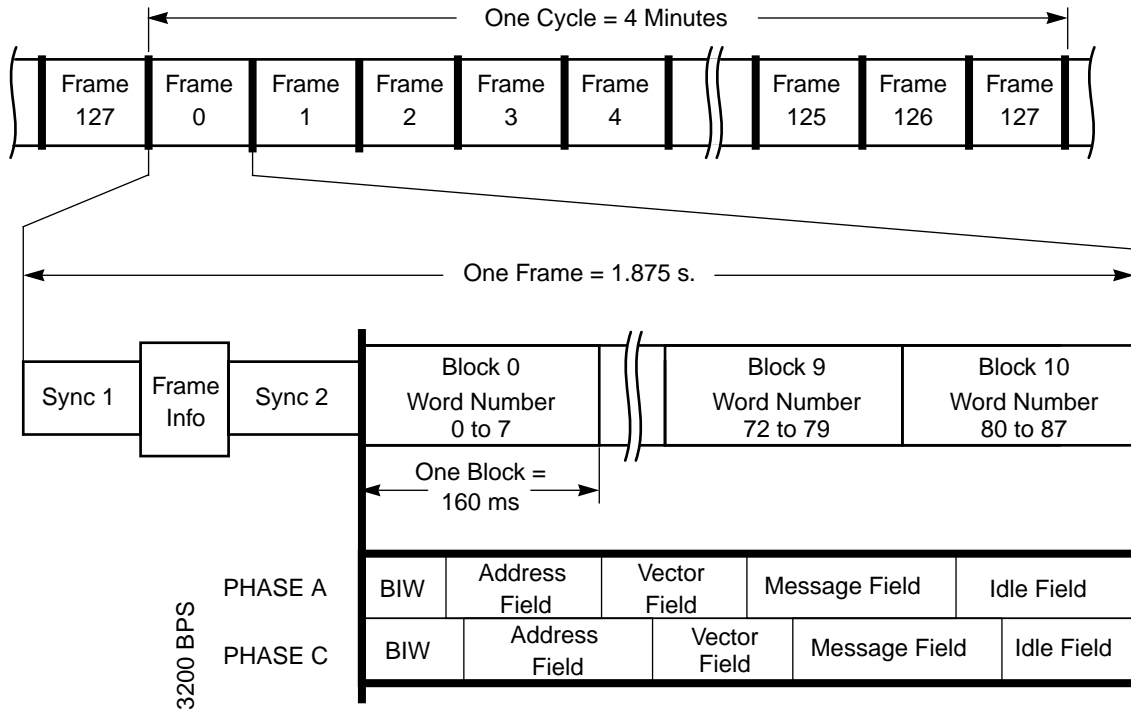


Figure A-3. FLEX Signal Structure for 3200 BPS

The 6400 bps rate is transmitted as four concurrent phases of information (A,B, C, and D), as shown in Figure A-4, at 3200 symbols per second using 4-level FSK modulation.

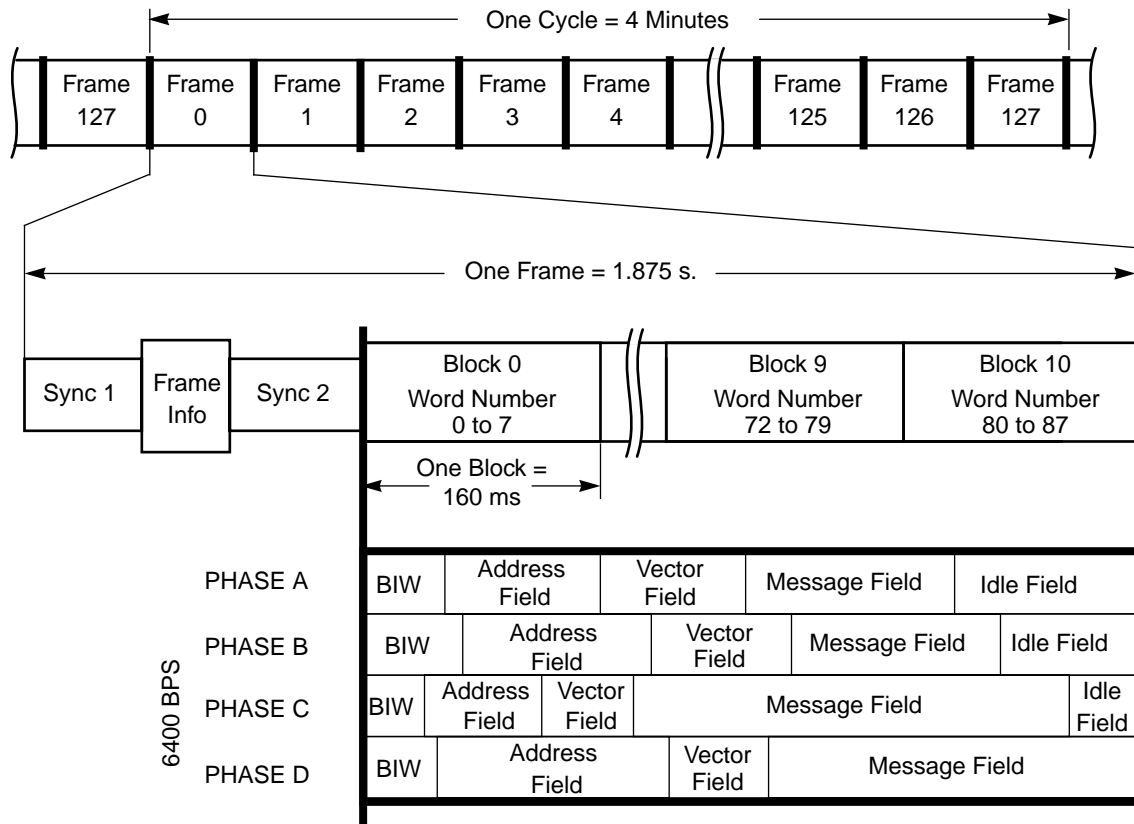


Figure A-4. FLEX Signal Structure for 6400 BPS

A.2.2 Frame Data Portion

As noted above, there are 11 data blocks following the frame synchronization portion of each frame. Each block has eight interleaved words per phase, numbered 0–87 contiguously for all 11 blocks, in every frame. Each word has information that allows for bit-error correction and detection contained within an error correcting code.

All the 88 words in each phase are organized into the following five fields:

- Block information field
- Address field
- Vector field
- Message field
- Idle field

The boundaries between the fields are independent of the block boundaries. Furthermore, at 3200 and 6400 bps, the information in one phase is independent of the information in a concurrent phase, and the boundaries between the fields of one phase are unrelated to the boundaries between the fields in a concurrent phase.

A.2.2.1 Block Information Field

The block information field may contain information words for determining time and date information and certain paging system information.

A.2.2.2 Address Field

The address field contains addresses assigned to paging devices. Addresses are used to identify information sent to individual paging devices and/or groups of paging devices. An address may be either a “short” one-word address or a “long” two-word address. Information in the FLEX signal may indicate that an address is a priority address. An address may be a “tone only” address, in which case no additional information is associated with the address.

A.2.2.3 Vector Field

The vector field consists of a series of vector words. Depending upon the type of message, a vector word (or words, in the case of a long address) may either contain all information necessary for the message or indicate the location of message words in the message field comprising the message information. If an address is not a tone-only address, an associated vector word is in the vector field. Information in the FLEX signal indicates the location of the vector word. Short addresses have one associated vector word; long addresses have two associated vector words. To enhance battery savings, a pager may go to low-power mode at the end of the address field if its address(es) is (are) not detected.

A.2.2.4 Message Field

The message field consists of a series of information words containing message information. The message information may be formatted in ASCII, BCD, or binary code, depending upon the message type. The following sections provide a detailed description of the various types of information words that may be used in the message field.

A.2.2.5 Idle Field

The idle field is used to separate blocks.

A.3 FLEX Message Word Definitions

This section provides definitions of numeric, hex/binary, alphanumeric, and secure message bits.

A.3.1 Numeric Data Message

The following tables describe the bit format of the numeric messages. The 4-bit numeric characters of the message are designated as lower-case letters “a,” “b,” “c,” “d,” etc. Refer to Table A-1 for standard or special-format numeric vectors and to Table A-2 for numeric vectors. Table A-3 gives definitions of numeric message bits.

Table A-1. Standard (V = 011) or Special-Format (V = 100) Numeric Vectors

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
1st	K ₄	K ₅	a ₀	a ₁	a ₂	a ₃	b ₀	b ₁	b ₂	b ₃	c ₀	c ₁	c ₂	c ₃	d ₀	d ₁	d ₂	d ₃	e ₀	e ₁	e ₂

Table A-1. Standard (V = 011) or Special-Format (V = 100) Numeric Vectors (Continued)

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
2nd	e ₃	f ₀	f ₁	f ₂	f ₃	g ₀	g ₁	g ₂	g ₃	h ₀	h ₁	h ₂	h ₃	i ₀	i ₁	i ₂	i ₃	j ₀	j ₁	j ₂	j ₃
3rd	k ₀	k ₁	k ₂	k ₃	l ₀	l ₁	l ₂	l ₃	m ₀	m ₁	m ₂	m ₃	n ₀	n ₁	n ₂	n ₃	o ₀	o ₁	o ₂	o ₃	q ₀
4th	q ₁	q ₂	q ₃	r ₀	r ₁	r ₂	r ₃	s ₀	s ₁	s ₂	s ₃	t ₀	t ₁	t ₂	t ₃	u ₀	u ₁	u ₂	u ₃	v ₀	v ₁
5th	v ₂	v ₃	w ₀	w ₁	w ₂	w ₃	y ₀	y ₁	y ₂	y ₃	z ₀	z ₁	z ₂	z ₃	A ₀	A ₁	A ₂	A ₃	B ₀	B ₁	B ₂
6th	B ₃	C ₀	C ₁	C ₂	C ₃	D ₀	D ₁	D ₂	D ₃	E ₀	E ₁	E ₂	E ₃	F ₀	F ₁	F ₂	F ₃	G ₀	G ₁	G ₂	G ₃
7th	H ₀	H ₁	H ₂	H ₃	l ₀	l ₁	l ₂	l ₃	J ₀	J ₁	J ₂	J ₃	V ₀	V ₁	V ₂	V ₃	L ₀	L ₁	L ₂	L ₃	M ₀
8th	M ₁	M ₂	M ₃	O ₀	O ₁	O ₂	O ₃	P ₀	P ₁	P ₂	P ₃	Q ₀	Q ₁	Q ₂	Q ₃	T ₀	T ₁	T ₂	T ₃	U ₀	U ₁

Table A-2. Numbered (V = 111) Numeric Vector

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
1st	K ₄	K ₅	N ₀	N ₁	N ₂	N ₃	N ₄	N ₅	R ₀	S ₀	a ₀	a ₁	a ₂	a ₃	b ₀	b ₁	b ₂	b ₃	c ₀	c ₁	c ₂
2nd	c ₃	d ₀	d ₁	d ₂	d ₃	e ₀	e ₁	e ₂	e ₃	f ₀	f ₁	f ₂	f ₃	g ₀	g ₁	g ₂	g ₃	h ₀	h ₁	h ₂	h ₃
3rd	i ₀	i ₁	i ₂	i ₃	j ₀	j ₁	j ₂	j ₃	k ₀	k ₁	k ₂	k ₃	l ₀	l ₁	l ₂	l ₃	m ₀	m ₁	m ₂	m ₃	n ₀
4th	n ₁	n ₂	n ₃	o ₀	o ₁	o ₂	o ₃	q ₀	q ₁	q ₂	q ₃	r ₀	r ₁	r ₂	r ₃	s ₀	s ₁	s ₂	s ₃	t ₀	t ₁
5th	t ₂	t ₃	u ₀	u ₁	u ₂	u ₃	v ₀	v ₁	v ₂	v ₃	w ₀	w ₁	w ₂	w ₃	y ₀	y ₁	y ₂	y ₃	z ₀	z ₁	z ₂
6th	z ₃	A ₀	A ₁	A ₂	A ₃	B ₀	B ₁	B ₂	B ₃	C ₀	C ₁	C ₂	C ₃	D ₀	D ₁	D ₂	D ₃	E ₀	E ₁	E ₂	E ₃
7th	F ₀	F ₁	F ₂	F ₃	G ₀	G ₁	G ₂	G ₃	H ₀	H ₁	H ₂	H ₃	l ₀	l ₁	l ₂	l ₃	J ₀	J ₁	J ₂	J ₃	V
8th	V ₁	V ₂	V ₃	L ₀	L ₁	L ₂	L ₃	M ₀	M ₁	M ₂	M ₃	O ₀	O ₁	O ₂	O ₃	P ₀	P ₁	P ₂	P ₃	Q ₀	Q ₁

Table A-3. Numeric Message Bit Definitions

Symbol	Definition
K	6-bit message check character (first 4 bits are in the vector word) —This check character is calculated by initializing the message check character (K) to 0 and summing the information bits of each code-word in the message, (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: the first is the 8 bits comprising i ₀ through i ₇ , the second group comprises bits i ₈ through i ₁₅ , and the third group comprises bits i ₁₆ through i ₂₀ . Bits i ₀ , i ₈ , and i ₁₆ are the LSBs of each group. The binary sum is calculated, and the result is shortened to the eight LSBs. The two MSB are shifted 6 bits to the right and summed with the six LSBs to form a new sum. This resultant sum is one's complemented with the six LSBs of the result being transmitted as the message check character.

Table A-3. Numeric Message Bit Definitions (Continued)

Symbol	Definition
N	Message number —When the system supports message retrieval, the system controller assigns message numbers separately for each paging address, starting at 0 and progressing in consecutive order to a maximum of 63. The actual maximum rol-over number is defined in the pager code-plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag = 0), it is not to be included in the missed message calculation.
R	Message retrieval flag —When this bit is set to 1, the pager expects to see messages numbered in order, with each address numbered separately. Detection of a missing number indicates a missed message. A message received with R = 0 is allowed to be out of order and shall not cause the pager to indicate that a message has been missed.
S	Special format —In the numbered message format, this bit set to 1 indicates that a special display format should be used.

A.3.1.1 Message Fill Rules

For numeric messages of 36 characters or less, or 34 characters if numbered, fewer than eight code-words on the channel are required. Only code-words containing the numeric message are to be transmitted. The space character (\$0C) should be used to fill any unused 4-bit characters in the last word, and zeros should be used to fill any remaining partial characters. The check sum is shortened correspondingly to include only the code-words that comprise the shortened message and the space and fill characters used to fill in the last word.

A.3.1.2 Special Format Numeric

Spaces and dashes as specified by the host are inserted into the received message. This feature in certain markets saves the transmission of an additional word on the channel. In the U.S. market, for example, a 10-character string (area code plus telephone number) fits into two message words. If the dashes or parentheses are to be included in the message, a third message word on the channel is required. The actual placement can be programmed into the paging device and can vary between markets.

A.3.2 Hex/Binary Message

The following tables describe the bit format of the hex/binary messages. The data of the message is designated as lower-case letters “a,” “b,” “c,” “d,” etc. Hex/binary messages can be sent as fragments. The service provider has the option of dividing the message into several pieces and sending the separate pieces at any time within a given time period. Table A-4 shows first-only fragments for vector type V = 110; Table A-5 shows all other fragments for the same vector type; and Table A-6 gives bit definitions for the hex/binary message.

Table A-4. Vector Type V = 110 First-Only Fragment

Message Word	i ₀	i ₁	i ₂	i ₃	i ₄	i ₅	i ₆	i ₇	i ₈	i ₉	i ₁₀	i ₁₁	i ₁₂	i ₁₃	i ₁₄	i ₁₅	i ₁₆	i ₁₇	i ₁₈	i ₁₉	i ₂₀
1st	K ₀	K ₁	K ₂	K ₃	K ₄	K ₅	K ₆	K ₇	K ₈	K ₉	K ₁₀	K ₁₁	C ₀	F ₀	F ₁	N ₀	N ₁	N ₂	N ₃	N ₄	N ₅

Table A-4. Vector Type V = 110 First-Only Fragment (Continued)

Message Word	i ₀	i ₁	i ₂	i ₃	i ₄	i ₅	i ₆	i ₇	i ₈	i ₉	i ₁₀	i ₁₁	i ₁₂	i ₁₃	i ₁₄	i ₁₅	i ₁₆	i ₁₇	i ₁₈	i ₁₉	i ₂₀
2nd	R ₀	M ₀	D ₀	H ₀	B ₀	B ₁	B ₂	B ₃	s ₀	s ₁	s ₂	s ₃	s ₄	S ₀	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇
3rd	a ₀	a ₁	a ₂	a ₃	b ₀	b ₁	b ₂	b ₃	c ₀	c ₁	c ₂	c ₃	d ₀	d ₁	d ₂	d ₃	e ₀	e ₁	e ₂	e ₃	f ₀
4th	f ₁	f ₂	f ₃	g ₀	g ₁	g ₂	g ₃	h ₀	h ₁	h ₂	h ₃	i ₀	i ₁	i ₂	i ₃	j ₀	j ₁	j ₂	j ₃	k ₀	k ₁
5th	k ₂	k ₃	l ₀	l ₁	l ₂	l ₃	m ₀	m ₁	m ₂	m ₃	n ₀	n ₁	n ₂	n ₃	o ₀	o ₁	o ₂	o ₃	q ₀	q ₁	q ₂
6th	q ₃	r ₀	r ₁	r ₂	r ₃	s ₀	s ₁	s ₂	s ₃	t ₀	t ₁	t ₂	t ₃	u ₀	u ₁	u ₂	u ₃	v ₀	v ₁	v ₂	v ₃
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table A-5. Vector Type V=110 All Other Fragments

Message Word	i ₀	i ₁	i ₂	i ₃	i ₄	i ₅	i ₆	i ₇	i ₈	i ₉	i ₁₀	i ₁₁	i ₁₂	i ₁₃	i ₁₄	i ₁₅	i ₁₆	i ₁₇	i ₁₈	i ₁₉	i ₂₀
1st	K ₀	K ₁	K ₂	K ₃	K ₄	K ₅	K ₆	K ₇	K ₈	K ₉	K ₁₀	K ₁₁	C ₀	F ₀	F ₁	N ₀	N ₁	N ₂	N ₃	N ₄	N ₅
2nd	a ₀	a ₁	a ₂	a ₃	b ₀	b ₁	b ₂	b ₃	c ₀	c ₁	c ₂	c ₃	d ₀	d ₁	d ₂	d ₃	e ₀	e ₁	e ₂	e ₃	f ₀
3rd	f ₁	f ₂	f ₃	g ₀	g ₁	g ₂	g ₃	h ₀	h ₁	h ₂	h ₃	i ₀	i ₁	i ₂	i ₃	j ₀	j ₁	j ₂	j ₃	k ₀	k ₁
4th	k ₂	k ₃	l ₀	l ₁	l ₂	l ₃	m ₀	m ₁	m ₂	m ₃	n ₀	n ₁	n ₂	n ₃	o ₀	o ₁	o ₂	o ₃	q ₀	q ₁	q ₂
5th	q ₃	r ₀	r ₁	r ₂	r ₃	s ₀	s ₁	s ₂	s ₃	t ₀	t ₁	t ₂	t ₃	u ₀	u ₁	u ₂	u ₃	v ₀	v ₁	v ₂	v ₃
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table A-6. Hex/Binary Message Bit Definitions

Symbol ¹	Definition
K	12-bit fragment check sum —This check sum is calculated by initializing the fragment check sum field (K) to 0 and calculating a sum over the information bits of each code-word in the message fragment (including control information and termination characters/bits in the last fragment word). This sum requires that the information bits of each word be broken into three groups: the first is the 8 bits comprising i ₀ through i ₇ , the second group comprises bits i ₈ through i ₁₅ , and the third group comprises bits i ₁₆ through i ₂₀ . Bits i ₀ , i ₈ , and i ₁₆ are the LSBs of each group. The binary sum is calculated over all code-words in the fragment, the one's complement of the sum is determined, and the twelve LSBs of the result is placed into the fragment check sum field to be transmitted at the beginning of the fragment.
C	1-bit message continued flag —When set to 1, this flag indicates fragments of this message are to be expected in any or possibly all of the following frames until a fragment with C = 0 is found. The longest message that fits into a frame is eighty-four code-words. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.

Table A-6. Hex/Binary Message Bit Definitions (Continued)

Symbol ¹	Definition
F	2-bit message fragment number —This is a modulo 3 message fragment number that is incremented by 1 in successive message fragments. The initial fragment starts at 11 and each following fragment is incremented by 1 modulo 3, (11, 00, 01, 10, 00, 01, 10, 00, etc.). The 11 state (after the initial fragment) is skipped in this process to avoid confusion with the single fragment of a non-continued message. The final fragment is indicated by the message continued flag being reset to 0.
N	Message number —When the system supports message retrieval the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers. An exception to this rule is the header message tied to a transparent message, each with the same message number.
R	Message retrieval flag —When this bit is set to 1, the pager expects to see messages numbered in order, with each address numbered separately. Detection of a missing number indicates a missed message. A message received with R = 0 is allowed to be out of order and not cause the pager to indicate that a message has been missed.
M	1-bit mail drop flag —When set to 1, this bit indicates the message is to be stored in a special area in memory. It automatically writes over existing data in that memory space.
D	1-bit display direction field: D = 0—Display left to right. D = 1—Display right to left (valid only when data sent as characters [i.e., blocking length not equal 0001]).
H	1-bit header message: H = 1—Indicates that this message is a header to a following transparent message of the same message number. H = 0—Implies message is not a header.
B	4-bit blocking length —This bit field indicates the number of bits per character. B ₃ B ₂ B ₁ B ₀ = 0001—1 bit per character (binary/transparent data). B ₃ B ₂ B ₁ B ₀ = 1111—15 bits per character. B ₃ B ₂ B ₁ B ₀ = 0000—16 bits per character. Data with blocking length other than 1 is assumed to be displayed on a character by character basis. (Default value = 0001)
s	5-bit field reserved for future use —Default value = 00000
S	8-bit Signature Field —The signature is defined to be the one's complement of the binary sum over the total message taken 8 bits at a time prior to formatting into fragments. It would be equivalent to a binary sum starting with the first 8 bits directly following the signature field (b ₃ b ₂ b ₁ b ₀ a ₃ a ₂ a ₁ a ₀ + d ₃ d ₂ d ₁ d ₀ c ₃ c ₂ c ₁ c ₀ and so on) and continuing all the way to the last valid data bit in the last word of the last fragment. The 8 LSB of the result are inverted (one's complement) and transmitted as the message signature. ²

1. Fields R through S are only in the first fragment of a message. The fields K through N make up the first word of every fragment in a long message.
2. This sum does not include any termination bits and should be calculated directly on the message as received by the terminal. The device generating the signature should be able to calculate before the fragmenting boundaries are determined.

A.3.2.1 Message Content

Starting with the first character of the third word in the message (second word in the remaining fragments), each 4-bit field represents one of any of the 16 possible combinations with no restrictions (data may be binary).

A.3.2.2 Fragment Termination

Unused bits in the last message word of a fragment are filled with all 0s or all 1s, depending on the last valid data bit. This choice is always the opposite polarity of the last valid data bit. For first fragments and inner fragments of a multifragment message, the message is interrupted (stopped) on the last full character boundary in the last code-word in the fragment. Any unused bits follow the rule just stated. The final fragment follows the above rules except when the last character is all 1s or all 0s and it exactly fills the last code-word. In this case, an additional word must be sent of opposite polarity of all 1s or all 0s to signify the position of the last character, thus allowing that last character to be an all 1s or an all 0s character pattern.

Note: This is always the case when a binary message ends in the last bit of the last word.

A.3.2.3 Message Header

A message header is designated by setting the H bit to 1. This is a displayable tag associated with a transparent nondisplayable data message. The tag and the associated message are complete in themselves. The pager associates the header message with the data file based on the two having the same message number and being sent in sequence (header first, followed by data file).

A.3.3 Alphanumeric Message

The following tables describe the bit format of the alphanumeric messages. The 7-bit characters of the message are designated as lower-case letters such as “a,” “b,” “c,” or “d.” Alphanumeric messages can be sent as fragments. The service provider has the option of dividing the message into several pieces and sending the separate pieces at any time within a given time period. Table A-7 shows first-only fragments for vector type V = 110; Table A-8 shows all other fragments for the same vector type; and Table A-9 gives bit definitions for the alphanumeric message.

Table A-7. Vector Type V = 101 First-Only Fragment

Message Word	i ₀	i ₁	i ₂	i ₃	i ₄	i ₅	i ₆	i ₇	i ₈	i ₉	i ₁₀	i ₁₁	i ₁₂	i ₁₃	i ₁₄	i ₁₅	i ₁₆	i ₁₇	i ₁₈	i ₁₉	i ₂₀
1st	K ₀	K ₁	K ₂	K ₃	K ₄	K ₅	K ₆	K ₇	K ₈	K ₉	C ₀	F ₀	F ₁	N ₀	N ₁	N ₂	N ₃	N ₄	N ₅	R ₀	M ₀
2nd	S ₀	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	a ₀	a ₁	a ₂	a ₃	a ₄	a ₅	a ₆	b ₀	b ₁	b ₂	b ₃	b ₄	b ₅	b ₆
3rd	c ₀	c ₁	c ₂	c ₃	c ₄	c ₅	c ₆	d ₀	d ₁	d ₂	d ₃	d ₄	d ₅	d ₆	e ₀	e ₁	e ₂	e ₃	e ₄	e ₅	e ₆
4th	f ₀	f ₁	f ₂	f ₃	f ₄	f ₅	f ₆	g ₀	g ₁	g ₂	g ₃	g ₄	g ₅	g ₆	h ₀	h ₁	h ₂	h ₃	h ₄	h ₅	h ₆

Table A-7. Vector Type V = 101 First-Only Fragment (Continued)

Message Word	i ₀ i ₁ i ₂ i ₃ i ₄ i ₅ i ₆ i ₇ i ₈ i ₉ i ₁₀ i ₁₁ i ₁₂ i ₁₃ i ₁₄ i ₁₅ i ₁₆ i ₁₇ i ₁₈ i ₁₉ i ₂₀
5th	i ₀ i ₁ i ₂ i ₃ i ₄ i ₅ i ₆ j ₀ j ₁ j ₂ j ₃ j ₄ j ₅ j ₆ k ₀ k ₁ k ₂ k ₃ k ₄ k ₅ k ₆
...	
nth	i i

Table A-8. Vector Type V = 101 Other Fragment

Message Word	i ₀ i ₁ i ₂ i ₃ i ₄ i ₅ i ₆ i ₇ i ₈ i ₉ i ₁₀ i ₁₁ i ₁₂ i ₁₃ i ₁₄ i ₁₅ i ₁₆ i ₁₇ i ₁₈ i ₁₉ i ₂₀
1st	K ₀ K ₁ K ₂ K ₃ K ₄ K ₅ K ₆ K ₇ K ₈ K ₉ C ₀ F ₀ F ₁ N ₀ N ₁ N ₂ N ₃ N ₄ N ₅ U ₀ V ₀
2nd	a ₀ a ₁ a ₂ a ₃ a ₄ a ₅ a ₆ b ₀ b ₁ b ₂ b ₃ b ₄ b ₅ b ₆ c ₀ c ₁ c ₂ c ₃ c ₄ c ₅ c ₆
3rd	d ₀ d ₁ d ₂ d ₃ d ₄ d ₅ d ₆ e ₀ e ₁ e ₂ e ₃ e ₄ e ₅ e ₆ f ₀ f ₁ f ₂ f ₃ f ₄ f ₅ f ₆
4th	g ₀ g ₁ g ₂ g ₃ g ₄ g ₅ g ₆ h ₀ h ₁ h ₂ h ₃ h ₄ h ₅ h ₆ i ₀ i ₁ i ₂ i ₃ i ₄ i ₅ i ₆
5th	j ₀ j ₁ j ₂ j ₃ j ₄ j ₅ j ₆ k ₀ k ₁ k ₂ k ₃ k ₄ k ₅ k ₆ l ₀ l ₁ l ₂ l ₃ l ₄ l ₅ l ₆
...	
nth	i i

Table A-9. Alphanumeric Message Bit Definitions

Symbol	Definition
K	10-bit fragment check character —This check character is calculated by initializing the fragment check character (K) to 0 and summing the information bits of each code-word in the message fragment (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: the first is the 8 bits comprising i ₀ through i ₇ , the second group comprises bits i ₈ through i ₁₅ , and the third group comprises bits i ₁₆ through i ₂₀ . Bits i ₀ , i ₈ , and i ₁₆ are the LSBs of each group. The binary sum is calculated, the one's complement of the sum is determined, and the 10 LSBs of the result is transmitted as the message check character.
C	1-bit message continued flag —When set, this flag indicates fragments of this message are to be expected in following frames. The longest message that fits into a frame is 84 code-words total. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.
F	2-bit message fragment number —This is a modulo 3 message fragment number that is incremented by 1 in successive message fragments. Initial fragments start at 11 and increment 1 for each successive fragment. The 11 state (after the start fragment) is skipped in this process to avoid confusion with an initial fragment of a noncontinued message. The final fragment is indicated by message continued flag being cleared.

Table A-9. Alphanumeric Message Bit Definitions (Continued)

Symbol	Definition
N	Message number —When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s), allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.
R	Message retrieval flag —When this bit is set, the pager expects to see messages numbered in order (each address numbered separately). Detection of a missing number indicates a missed message. A message received with R = 0 is allowed to be out of order and not cause the pager to indicate that a message has been missed.
M	1-bit mail drop flag —When set, this flag indicates the message is to be stored in a special area in memory. It automatically writes over existing data in that memory space.
S	7-bit signature field —The signature is defined to be the one's complement of the binary sum over the total message (all fragments) taken 7 bits at a time (on alpha character boundary) starting with the first 7 bits directly following the signature field (a6a5a4a3a2a1a0, b6b5b4b3b2b1b0, etc.). The seven LSBs of the result are transmitted as the message signature.
U, V	Fragmentation control bits —This field exists in all fragments except the first fragment. It is used to support character position tracking in each fragment when symbolic characters (characters made up of 1, 2, or 3 ASCII characters) are transmitted using the Alphanumeric message type. The default value for the U, V pair is 0, 0. See Section A.3.3.4, "Enhanced Fragmentation Rules," for more information.

A.3.3.1 Message Content

Starting with the second character of the second word in the message (first character of the second word in all remaining fragments), each 7-bit field represents standard ASCII (ISO 646-1983E) characters with options for certain international characters.

A.3.3.2 Message Termination

The ASCII character ETX (\$03) should be used to fill any unused 7-bit characters in a word. In the case where symbolic characters are being transmitted, special rules for fragment and message termination are defined in the following information on alphanumeric message rules for symbolic characters sets.

A.3.3.3 Alphanumeric Message Rules for Symbolic Characters Sets

In the past, paging protocols have supported symbolic characters (e.g., Chinese, Kanji, etc.) using a 7-bit ASCII protocol. When the FLEX alphanumeric mode is used to carry this same signaling format, special fragmenting rules are required to maintain character boundaries, so performance is optimized under poor signal conditions. The following rules allow character positions within a fragment to be determined when prior fragments are missing.

A.3.3.4 Enhanced Fragmentation Rules

The following list explains the MC68183's rules for enhanced fragmentation.

- The pager must recognize <NUL> characters only at the end of fragments where they are used as fill characters. The pager must remove these characters so that the displayed message is not affected. In all other positions the <NUL> character must be considered a result of channel errors. (This provides a method to end each fragment with a complete character and does not disrupt the pager that is not capable of following all of the enhanced fragmenting (EF)).
- The last fragment is to be completed by filling unused character positions with <ETX> characters or <NUL> characters. (Original FLEX alphanumeric message definition (<ETX>) plus the new <NUL> requirement.) When the message ends exactly in the last character position in the last BCH code-word, no additional <ETX> is required.
- The U and V bits in the message header are available in all fragments following the initial fragment to aid in decoding. In the first fragment, the pager must assume the message starts in the default character mode. For the second and remaining fragments, the definition of the (U,V) field is shown in Table A-10.

Table A-10. U and V Field Definition

U ₀	V ₀	Definition
0	0	EF not supported in controller
0	1	Reserved (for a second alternate character mode)
1	0	Default character mode—start position 1
1	1	Alternate character mode—start position 1

When the EF field is 00, the pager decodes messages, allowing characters to be split between fragments. When the U, V field is not 0, 0, each fragment starts on a character boundary with the character mode defined by the above table.

A.3.3.5 Secure Message

The following tables describe the bit format of the secure messages. The 7-bit characters of the message are designated as lower-case letters “a,” “b,” “c,” “d,” etc. Secure messages can be sent as fragments. The service provider has the option of dividing the message into several pieces and sending the separate pieces at any time within a given time period. Table A-11 shows all fragments for vector type V = 000, and Table A-12 gives secure message bit definitions.

Table A-11. Vector Type V = 000 All Fragments

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
1st	K ₀	K ₁	K ₂	K ₃	K ₄	K ₅	K ₆	K ₇	K ₈	K ₉	C ₀	F ₀	F ₁	N ₀	N ₁	N ₂	N ₃	N ₄	N ₅	s ₀	s ₁
2nd	a ₀	a ₁	a ₂	a ₃	a ₄	a ₅	a ₆	b ₀	b ₁	b ₂	b ₃	b ₄	b ₅	b ₆	c ₀	c ₁	c ₂	c ₃	c ₄	c ₅	c ₆
3rd	d ₀	d ₁	d ₂	d ₃	d ₄	d ₅	d ₆	e ₀	e ₁	e ₂	e ₃	e ₄	e ₅	e ₆	f ₀	f ₁	f ₂	f ₃	f ₄	f ₅	f ₆

Table A-11. Vector Type V = 000 All Fragments (Continued)

Message Word	i0	i1	i2	i3	i4	i5	i6	i7	i8	i9	i10	i11	i12	i13	i14	i15	i16	i17	i18	i19	i20
4th	g ₀	g ₁	g ₂	g ₃	g ₄	g ₅	g ₆	h ₀	h ₁	h ₂	h ₃	h ₄	h ₅	h ₆	i ₀	i ₁	i ₂	i ₃	i ₄	i ₅	i ₆
5th	j ₀	j ₁	j ₂	j ₃	j ₄	j ₅	j ₆	k ₀	k ₁	k ₂	k ₃	k ₄	k ₅	k ₆	l ₀	l ₁	l ₂	l ₃	l ₄	l ₅	l ₆
...																					
nth	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i	i

Table A-12. Secure Message Bit Definitions

Symbol	Definition
K	10-bit fragment check character —This check character is calculated by initializing the fragment check character (K) to 0 and summing the information bits of each code-word in the message fragment (including control information and termination characters and bits in the last message word) to a check sum register. The information bits of each word are broken into three groups: the first is the 8 bits comprising i ₀ through i ₇ , the second group comprises bits i ₈ through i ₁₅ , and the third group comprises bits i ₁₆ through i ₂₀ . Bits i ₀ , i ₈ , and i ₁₆ are the LSBs of each group. The binary sum is calculated, the one's complement of the sum is determined, and the ten LSBs of the result is transmitted as the message check character.
C	1-bit message continued flag —When set, the message continued flag indicates fragments of this message are to be expected in following frames. The longest message that fits into a frame is 84 code-words total. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.
F	2-bit message fragment number —This is a modulo 3 message fragment number that is incremented by 1 in successive message fragments. Initial fragments start at 11 and increment 1 for each successive fragment. The 11 state (after the start fragment) is skipped in this process to avoid confusion with an initial fragment of a non-continued message. The final fragment is indicated by message continued flag being cleared.
N	Message number —When the system supports message retrieval, the system controller assigns message numbers (for each paging address separately) starting at 0 and progressing up to a maximum of 63 in consecutive order. The actual maximum roll-over number is defined in the pager code plug to accommodate values set in the system infrastructure. When message numbers are not received in order, the subscriber should assume a message has been missed. The subscriber or the pager may determine the missing message number(s) allowing a request to be made for retrieval. When a normal unnumbered numeric message is received (message retrieval flag is equal to 0), it is not to be included in the missed message calculation. This number is also used to identify fragments of the same message. Multiple messages to the same address must have separate message numbers.
s	Spare bit —not used and set to 0.

A.3.3.6 Message Content

Starting with the first character of the second word in the message (and first character of all remaining fragments), each 7-bit field represents standard ASCII (ISO 646-1983E) characters with options for certain international characters.

A.3.3.7 Message Termination

The ASCII character ETX (\$03) should be used to fill any unused 7-bit characters in a word.

A.3.4 FLEX Encoding and Decoding Rules

The encoding and decoding rules identify the minimum requirements that must be met by the paging device, paging terminal, or other encoding equipment to properly format a FLEX data stream for RF transmission and to successfully decode it.

A.3.4.1 FLEX Encoding Rules

The following list explains the MC68183's rules concerning FLEX encoding.

- The stability of the encoder clock used to establish time positions of FLEX frames must be no worse than ± 25 ppm (including worst-case temperature and aging effects).
- A maximum of two occurrences of an identical individual or radio group address is allowed in any frame for unfragmented messages. This rule applies across all phases in a multiphase frame. For example, for decoding devices that support any-phase addressing, an any-phase address may appear at once in two different phases in a single multiphase frame.
- Once an individual or radio group address is used to begin transmitting a fragmented message, that same address must not be used to start a new fragmented transmission until the first fragmented transmission has been completed.
- For the duration of time that an individual or radio group address is being used to send a fragmented message, that same address must not appear more than once in any frame to send an unfragmented message.
- Once a specific dynamic group address (temporary address) is assigned to a group, it must not be reused until its associated message has been transmitted in its entirety. Given this constraint, the same dynamic group address can only appear once in any frame.
- A dynamic group address cannot be used to set up a second dynamic group.
- Messages using any of the three defined numeric vectors ($V_2V_1V_0 = 011, 100, \text{ and } 111$) cannot be fragmented and thus must be completely contained in a single frame.
- Fragments of the same message must be sent at a frequency of at least 1 every 32 frames (i.e., at least once a minute) or 1 every 128 frames (i.e., at least once every 4 minutes) as specified by the service provider.
- Enhanced message fragmenting for symbolic character transmission requires that the encoder track character boundaries within each fragment in order to avoid character splitting.
- Message numbering as an optional feature is offered by some carriers and available on an individual subscriber basis.
- Message numbers must be assigned sequentially in ascending order.
- Message number sequences must be separately maintained for each individual and radio group address.
- Message numbers are not used (retrieval message number disabled) in conjunction with a dynamic group address.
- When a missed message is retransmitted from message retrieval storage, the message must have $R = 0$ to avoid creating an out of sequence message that may cause the pager to indicate a missed message.

A.3.4.2 FLEX Decoding Rules

The following list explains the MC68183's rules concerning FLEX decoding.

- FLEX decoding devices may implement either single-phase addressing or any-phase addressing.
- FLEX decoding devices that support the numeric vector type ($V_2V_1V_0 = 011$) must also support the short message vector ($V_2V_1V_0 = 010$) with the message type (t_1t_0) set to 00.
- FLEX decoding devices that support the alphanumeric vector type ($V_2V_1V_0 = 101$) must support the numeric vector type ($V_2V_1V_0 = 011$) and the short message vector ($V_2V_1V_0 = 010$) with the message type (t_1t_0) set to 00. FLEX paging devices that implement any-phase and support the alphanumeric vector type ($V_2V_1V_0 = 101$) must also support the short instruction vector ($V_2V_1V_0 = 001$) with the instruction type ($i_2i_1i_0$) set to 000.
- FLEX decoding devices must be capable of decoding frames at all of the following combinations of data rate and modulation mode. They are 1600 bps, 2 level; 3200 bps, 2 level; 3200 bps, 4 level; 6400 bps, 4 level.
- FLEX decoding devices must be designed to tolerate 4-minute fragment separation times.

A.3.5 FLEX Character Sets and Rules

The alphanumeric, standard, and alternate character sets displayed in message mode are described here.

A.3.5.1 Alphanumeric Character Set

Table A-13 through Table A-15 define the characters to be displayed in the FLEX alphanumeric message mode. Control characters that are not acted upon by the pager are ignored in the display process (do not require display space), but are stored in memory for possible download to an external device

Table A-13. Alphanumeric Character Set

Least Significant 4 bits of Character	Most Significant 3 Bits of Character							
	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	'	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	\$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(8	H	X	h	x
9	TAB	EM)	9	I	Y	i	y

Table A-13. Alphanumeric Character Set (Continued)

Least Significant 4 bits of Character	Most Significant 3 Bits of Character							
	0	1	2	3	4	5	6	7
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[k	{
C	FF	FS	,	<	L	\	l	
D	CR	GS	-	=	M]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

A.3.5.2 Numeric Character Set

Table A-14 and Table A-15 define the characters to be displayed in the FLEX numeric message mode.

Table A-14. Standard Character Set (Peoples-Republic-of-China Option Off)

Character	B ₃	B ₂	B ₁	B ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
Spare	1	0	1	0
U	1	0	1	1
Space	1	1	0	0
-	1	1	0	1
]	1	1	1	0
[1	1	1	1

Table A-15. Alternate Character Set (Peoples-Republic-of-China-Option On)

Character	B ₃	B ₂	B ₁	B ₀
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
Space	1	1	0	0
C	1	1	0	1
D	1	1	1	0
E	1	1	1	1

A.3.6 FLEX Local Time And Date

The FLEX protocol allows for systems to transmit time information in its block information field. When a system provider supports local time transmissions, the system provider is required, at a minimum, to transmit at least one-time related block information word in each phase transmitted in frame 0, cycle 0. The time transmitted is the local time for the transmitted time zone and refers to the actual time at the leading edge of the first bit of sync 1 of frame 0 of the current cycle. The information carried in the s bits of the block information word depend on the value of the f bits of the block information word. The following sections describe the bit definitions of the time-related block information words.

A.3.6.1 Month/Day/Year

Refer to Table A-16 for definition of month/day/year block information words.

Table A-16. Month/Day/Year Block Information Word Definition

$f_2f_1f_0$	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0
001	m_3	m_2	m_1	m_0	d_4	d_3	d_2	d_1	d_0	Y_4	Y_3	Y_2	Y_1	Y_0

Note: m = Month field—0001 through 1100 (binary) correspond to January through December, respectively.
 d = Day field—00001 through 11111 (binary) correspond to 1 through 31, respectively.
 Y = Year field—This represents the year with modulo arithmetic. 00000 through 11111 (binary) representing 1994 through 2025, 2026 through 2057, etc.

A.3.6.2 Second/Minute/Hour

Table A-17 defines the second/minute/hour block information words.

Table A-17. Second/Minute/Hour Block Information Word Definition

$f_2f_1f_0$	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0
010	S_5	S_4	S_3	M_5	M_4	M_3	M_2	M_1	M_0	H_4	H_3	H_2	H_1	H_0

Note: S = Second field—This represents a coarse value of the seconds field. These bits represent the seconds in eighth of a minute (7.5 second) increments. 000 through 111 (binary) correspond to 0 through 52.5 seconds, respectively
 M = Minute field—000000 through 111011 (binary) correspond to 0 through 59, respectively
 H = Hour field—00000 through 10111 (binary) correspond to 0 through 23, respectively.

A.3.6.3 Accurate Seconds/Daylight Savings Time/Time Zone

Refer to Table A-18 for a definition of the system message block information words.

Table A-18. System Message Block Information Word Definition

$f_2f_1f_0$	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0	Description
101	S_2	S_1	S_0	x	L_0	z_4	z_3	z_2	z_1	z_0	0	1	0	X	System Message

Note: When the $s_3 s_2 s_1 s_0$ field is set to 0100 or 0101, the other s_4 through s_{13} are defined as above. The system messages with the $s_3 s_2 s_1 s_0$ field set to some other value do not contain time related information.
 S = Accurate Seconds—This field provides a more accurate seconds reference and can be used to adjust the seconds to within 1 second. This field represents how much time should be added to the coarse seconds in 64^{th} - of-a-minute increments.
 L = Daylight Savings Time—When this bit is set, the time being transmitted is local standard time. When it is clear, the time being transmitted is Daylight Savings Time.
 z = Time Zone—These bits indicate the time zone for which the time is being transmitted. The offset from GMT is the offset for local standard time. Table A-19 describes the values for z .

Table A-19. Time-Zone Values

Z ₄ Z ₃ Z ₂ Z ₁ Z ₀	Time Zone	Z ₄ Z ₃ Z ₂ Z ₁ Z ₀	Time Zone	Z ₄ Z ₃ Z ₂ Z ₁ Z ₀	Time Zone
00000	GMT	01011	GMT + 1100	10110	GMT – 1000
00001	GMT + 0100	01100	GMT + 1200	10111	GMT – 0900
00010	GMT + 0200	01101	GMT + 0330	11000	GMT – 0800
00011	GMT + 0300	01110	GMT + 0430	11001	GMT – 0700
00100	GMT + 0400	01111	GMT + 0530	11010	GMT – 0600
00101	GMT + 0500	10000	RESERVED	11011	GMT – 0500
00110	GMT + 0600	10001	GMT + 0545	11100	GMT – 0400
00111	GMT + 0700	10010	GMT + 0630	11101	GMT – 0300
01000	GMT + 0800	10011	GMT + 0930	11110	GMT – 0200
01001	GMT + 0900	10100	GMT – 0330	11111	GMT – 0100
01010	GMT + 1000	10101	GMT – 1100		

A.3.7 FLEX CAPCODEs

In order to send messages to a FLEX decoding device, the FLEX service provider must know the device's address, the address type (single-phase, any-phase, or all-phase), the address's assigned phase, the address's assigned frame, and the address's battery cycle. This information is typically included in a FLEX CAPCODE. The assignment of CAPCODEs is regulated to prevent duplication of addresses on a system. Check with your FLEX service provider or other appropriate regulatory body for FLEX CAPCODE assignments. The following paragraphs describe what these parameters define.

The device address consists of one or two 21-bit words. A one-word address is called a short address, while a two-word address is called a long address. Address words are separated into ranges in accordance with Table A-20.

Table A-20. Address Word Range Definition

Type	Hexadecimal Value
Idle word (illegal address)	000000
Long address 1	000001–008000
Short address	008001–1E0000
Long address 3	1E0001–1E8000
Long address 4	1E8001–1F0000
Short address (reserved)	1F0001–1F27FF
Info service address	1F2800–1F67FF

Table A-20. Address Word Range Definition (Continued)

Type	Hexadecimal Value
Network address	1F6800–1F77FF
Temporary address	1F7800–1F780F
Operator messaging address	1F7810–1F781F
Short address (reserved)	1F7820–1F7FFE
Long address 2	1F7FFF–1FFFFE
Idle word (illegal address)	1FFFFFF

Long addresses are grouped into the sets listed in Table A-21.

Table A-21. Long Address Sets

Long Address Set	First Word	Second Word
1–2	Long address 1	Long address 2
1–3	Long address 1	Long address 3
1–4	Long address 1	Long address 4
2–3	Long address 2	Long address 3
2–4	Long address 2	Long address 4

The address type indicates how messages on a particular address can be delivered in multiphase FLEX frames. Messages sent on single-phase addresses can only be delivered in a particular phase (a, b, c, or d). Messages sent on any-phase addresses can be delivered in any phase, but a single message is limited to a single phase per frame. Messages sent on all-phase addresses can be delivered in any phase, and a single message can be spread across multiple phases in a single frame. All-phase messaging is a future feature of FLEX and has not been completely defined.

The assigned phase is required only for single-phase devices. It determines the phase (a, b, c, or d) in which the messages is sent.

The assigned frame and battery cycle determine the frames in which the decoding device typically looks for messages (other system factors can cause the decoding device to look in other frames in addition to the typical frames).

The battery cycle is a number between 0 and 7 and defines how often the decoding device looks for messages on the FLEX channel. For a given battery cycle “b,” the decoding device looks in every 2^b frames. Thus, an address with an assigned frame of 3 and a battery cycle of 5 typically looks for messages in frame 3 and every 32 frames thereafter (i.e., frames 3, 35, 67, and 99).

The FLEX CAPCODE is defined to represent either a short or a long address. The short address is defined in the FLEX protocol as one code-word on the RF channel and is represented by a 7-digit decimal field. The long address is defined in the FLEX protocol as two code-words on the RF channel and is represented by a 9- or 10-digit decimal field. The long addresses in set 1–2 are represented by a 9-digit decimal field. The long addresses in sets 1–3, 1–4, 2–3, and 2–4 are represented by a 10-digit

decimal field. An alphabetic character known as the “CAPCODE type” always precedes the 7-, 9-, or 10-digit decimal address field. The CAPCODE type indicates the type of address and distinguishes FLEX CAPCODEs from CAPCODEs of other paging protocols.

A.3.7.1 CAPCODE Type

Example CAPCODEs are shown in Table A-22. The CAPCODE type can be any of “A” through “L” or “U” through “Z”. The CAPCODE types “A” through “L” indicate that the standard rules are used to derive the assigned frame and phase information from the address field. Section A.3.7.2, “Standard Frame and Phase Embedding Rules.” For these CAPCODE types, the battery cycle (indicated as a “b” in example 1, Table A-22) is indicated by a single decimal digit “0” through “7” preceding the CAPCODE type. When the FLEX standard battery cycle of 4 (16-frame cycle) is used, the battery-cycle digit is not required. (See example 2 in Table A-22.)

The CAPCODE types “U” through “Z” indicate that the standard frame and phase embedding rules were not used and additional information is required. The phase assignment can be derived from the CAPCODE type, as described in Table A-24 on page -29. The 3-digit decimal frame assignment “000” through “127” (indicated by “fff” in example 3, Table A-22) and single-digit decimal battery cycle “0” through “7” (indicated as a “b” in example 3 in Table A-22) may precede this CAPCODE type. The frame and battery cycle fields are not required. When they are not included. (See example 4 in Table A-22.) the paging device or the subscriber database must be accessed to determine the assigned frame and battery cycle.

The extended CAPCODE is a regular CAPCODE with a 10-digit address field and preceded by an extra alphabetic character “P” through “S.” These CAPCODEs are used to provide additional information required for roaming devices. See Table A-22 for FLEX CAPCODE examples.

Table A-22. FLEX CAPCODE Examples

Example	Short	Long	Extended
1	bA1234567	bA123456789	RbA1234567890
2	A1234567	A123456789	RA1234567890
3	fffbU1234567	fffbU123456789	RfffbU1234567890
4	U1234567	U123456789	RU1234567890

By using the convention of seven digits to represent short addresses, nine digits to represent some of the long addresses in set 1–2, and 10 digits to represent the balance of long addresses, it is possible to differentiate between the different types of addresses. The range of the decimal address field consists of the numbers 1 through 5,370,810,366 where short and other single code-word addresses fall below 2,031,615 and long addresses are above 2,101,248. The goal in displaying a CAPCODE is to use the shortest form possible. Even though the nonstandard form could represent a standard assignment, the standard form is chosen to indicate that it is a standard assignment. All CAPCODE forms, except example 4 in Table A-22, contain the information required to send a message to a subscriber unit.

A.3.7.2 Standard Frame and Phase Embedding Rules

Maximum battery life in a FLEX decoding device is achieved when all of the addresses assigned to a device are in the same frame. For single-phase decoding devices, all assigned addresses are required to be in the same phase.

Normally, it is very desirable to spread the population of FLEX subscriber units on a system across all four phases of all 128 frames. Frame- and phase-spreading can be performed automatically as addresses are assigned sequentially by embedding that information into the 7-, 9-, and 10-digit decimal FLEX address.

The standard procedure for deriving the phase and frame values from the CAPCODE starts by separating the 7-, 9-, or 10-digit decimal address portion (field to the right of the CAPCODE type) and performing a decimal to binary conversion. The LSB is labeled bit “0”. The following bits “2 and 3” in order, specify phases 00, 01, 10, or 11 for phase 0,1,2,3 (a, b, c, d), and bits “4–10” represent frames “000” through “127”.

The frame and phase can also be derived from the 7-, 9-, or 10-digit decimal address by using modulo arithmetic (base 10) where the following is true:

$$\text{Phase} = (\text{Integer}(\text{Addr}/4)) \text{ Modulo } 4$$

$$\text{Frame} = (\text{Integer}(\text{Addr}/16)) \text{ Modulo } 128$$

When these rules are used, and addresses are assigned in order, the phase increments after four consecutive addresses are assigned, while the frame is incremented after 16 addresses are assigned.

A.3.7.3 CAPCODE Alpha Character Definition

The alpha character in the FLEX CAPCODE indicates the type of decoding device to which the address is assigned. The types include single-phase, any-phase, or all-phase. It also indicates whether the address is the first, second, third, or fourth address in the subscriber unit (when addresses are assigned in order and follow standard rules). Finally, the alpha character specifies the rules for determining in which phase and frame the address is active. Refer to Table A-23 for alpha character codes.

Table A-23. Alpha Character Codes

Standard Rules	No Rules (Nonstandard Form)
A—Single-phase subtract 0	U—Single-phase, phase 0
B—Single-phase subtract 1	V—Single-phase, phase 1
C—Single-phase subtract 2	W—Single-phase, phase 2
D—Single-phase subtract 3	X—Single-phase, phase 3
E—Any-phase, subtract 0	Y—Any-phase
F—Any-phase subtract 1	—
G—Any-phase subtract 2	—
H—Any-phase subtract 3	—
I—All-phase subtract 0	Z—All-phase
J—All-phase subtract 1	—
K—All-phase subtract 2	—
L—All-phase subtract 3	—

The following rules apply:

- The character “A” represents a single-phase subscriber unit using the standard rules for embedding phase and frame. The character “B” is similar to “A”, except that 1 is subtracted from the CAPCODE before the standard rule is applied. Likewise, the characters “C” and “D” indicate that 2 or 3 is to be subtracted before applying the rule. Using these CAPCODE characters ensures that sequentially numbered CAPCODEs are assigned to a common phase and frame. These procedures modify the standard rules and are intended to simplify the order-entry process for multiple address subscriber units. When addresses are assigned in order, the subtraction of 1, 2, or 3 ensures that the calculation for each additional address in a decoding device is referenced to the first address. Thus, all A, B, C, and D addresses are assigned to the same frame and phase.
- Alpha characters “E” through “H” and “I” through “L” represent any-phase and all-phase subscriber units where the subtract rule is modified to ensure that all addresses of a multiple address subscriber unit are in the same frame.
- For the cases where no rule is defined, the letters “U” through “X” indicate single-phase subscriber units assigned to phases 0 through 3 (phases a through d) with the frame and battery cycle explicitly displayed. “Y” and “Z” indicate non-standard addresses for any-phase and all-phase subscriber units.
- If the subscriber unit contains only a single individual address and the user is content with the recommended 30-second battery cycle, letter “A”, “E”, or “I” is added as a prefix to the 7-, 9-, or 10-digit address, where the following holds true:
 - “A” indicates a single-phase device.
 - “E” indicates an any-phase device.
 - “I” indicates an all-phase device.
- If the unit were a two-address unit where both addresses are individual addresses, then “A”, “E”, or “I” would again preface the address field of the first address. “B”, “F”, or “J” would preface the second address.

The “B”, “F”, or “J” indicates that the address is a second address and it is to have the properties of the first address. This rule eliminates the need for an administrative operator or a salesperson to calculate a starting address, which would allow standard rules to always apply.
- In other cases, especially where a group address is to be included, it is very likely that the “U” through “Z” forms of the CAPCODE will be used so that the frame can be explicitly chosen to provide best battery life, and the required “same phase” operation can be met in the case of the single-phase units.

A.3.7.4 CAPCODE to Binary Conversion

A.3.7.4.1 Short CAPCODE

To convert a short address CAPCODE, the number 32,768 is added to the 7- digit decimal CAPCODE address (or to any CAPCODE less than 2,031,615). The resultant number is then converted to a 21-bit binary number, which then becomes the information bits of the (31,21) BCH code-word transmitted over the air.

A.3.7.4.2 Long CAPCODE 2,101,249 to 1,075,843,072

Long address set 1–2 is in this range. To convert a long address CAPCODE, the number 2,068,481 is subtracted from the CAPCODE address. The resultant number is then divided by 32,768 with the remainder, incremented by 1, being the first word of the long address. This is the same as calculating

the $((\text{CAPCODE} - 2,068,481) \text{ modulo } 32768) + 1$. This value is converted to a 21-bit binary number, which becomes the information bits in the (31,21) BCH code-word transmitted over the air as the first address word.

The second word of the long address is determined by first calculating the integer portion of the $(\text{CAPCODE} - 2,068,481)$ divided by 32,768. This value is then subtracted from 2,097,151 (equivalent to the one's complement of the value in binary), and converted to a 21-bit binary number, which becomes the information bits in the (31, 21) BCH code-word transmitted over the air as the second address word.

A.3.7.4.3 Long CAPCODE 1,075,843,073 to 3,223,326,720

Long address sets 1–3 and 1–4 are in this range. The first word of the long address is calculated following the same rules for the long addresses set 1–2. The second long address word is determined by subtracting 2,068,481 from the CAPCODE, the resultant number is divided by 32,768 with the integer portion added to 1,933,312. This value is converted to a 21-bit binary number, which becomes the (31,21) BCH code-word transmitted over the air as the second address word.

A.3.7.4.4 Long CAPCODE 3,223,326,721 to 4,297,068,542

Long address set 2–3 is in this range. The first word is determined by subtracting 2,068,479 from the CAPCODE. The remainder of dividing by 32,768 is retained (i.e., modulo 32,768). This value is then added to 2,064,383 with the result converted to a 21-bit binary number, which becomes the information bits in the (31,21) BCH code-word transmitted over the air as the 1st address word.

The second word is determined by subtracting 2,068,479 from the CAPCODE and finding the integer portion after dividing by 32,768. This value is then added to 1,867,776 and converted to a 21-bit binary number, which becomes the (31,21) BCH code-word transmitted over the air as the second address word.

A.3.7.5 Binary to CAPCODE Conversion

With the address code-word values that are transmitted over the air, the CAPCODE can be calculated by performing the inverse of the above-specified process. As an example, the short address code-word is converted to decimal and the number 32,768 is subtracted to arrive at the 7-digit address portion of the CAPCODE. For the two word long address set 1–2, the address word 1 is first converted from binary to decimal. The second address word is then complemented, (or subtracted from 2,097,151 decimal) and converted to a decimal. This value is multiplied by 32,768, added to 2,068,480, and then added to address word 1. The result is the address portion of the FLEX CAPCODE.

A.3.7.6 CAPCODE Assignments

Table A-24 defines the address usage assignment. All addresses not listed in this table are not defined and reserved for future use.

Table A-24. CAPCODE Assignment Table

CAPCODE Address Value	Description
0,000,000,000	Illegal
0,000,000,001 to 0,001,933,312	Short addresses
0,001,933,313 to 0,001,998,848	Illegal
0,001,998,849 to 0,002,009,087	Reserved for future use

Table A-24. CAPCODE Assignment Table (Continued)

CAPCODE Address Value	Description
0,002,009,088 to 0,002,025,471	Information service addresses
0,002,025,472 to 0,002,029,567	Network addresses
0,002,029,568 to 0,002,029,583	Temporary addresses
0,002,029,584 to 0,002,029,599	Operator messaging addresses
0,002,029,600 to 0,002,031,614	Reserved for future use
0,002,031,615 to 0,002,101,248	Illegal
0,002,101,249 to 0,102,101,250	Long address set 1–2 uncoordinated
0,102,101,251 to 0,402,101,250	Long address set 1–2 by country ¹
0,402,101,251 to 1,075,843,072	Long address set 1–2 global ²
1,075,843,073 to 2,149,584,896	Long address set 1–3 global ²
2,149,584,897 to 3,223,326,720	Long address set 1–4 global ²
3,223,326,721 to 3,923,326,750	Long address set 2–3 by country ¹
3,923,326,751 to 4,280,000,00	Long address set 2–3 reserved
4,280,000,001 to 4,285,000,000	Long address set 2–3 info service global ²
4,285,000,001 to 4,290,000,000	Long address set 2–3 info service ³ by country ¹
4,290,000,001 to 4,291,000,000	Long address set 2–3 info service ³ world-wide use ⁴
4,291,000,001 to 4,297,068,542	Reserved for future use

1. “By Country”—The addresses are coordinated within each country and with countries along borders.

2. “Global”—The address is coordinated to be unique worldwide.

3. “Info Service”—Rules governing the use of these addresses are not currently defined.

4. “World Wide Use”—1000 addresses are assigned to each country for worldwide use.

Appendix B SPI Packets

The SPI transmits all data communicated between the MC68183 and the host MCU in 32-bit packets. Each packet consists of an 8-bit ID followed by 24 bits of information. The MC68183 uses the SPI bus in full duplex mode. In other words, whenever a packet communication occurs, the data in both directions is valid packet data.

The SPI interface consists of a $\overline{\text{READY}}$ pin and four SPI pins ($\overline{\text{SS}}$, SCK, MOSI, and MISO). The $\overline{\text{SS}}$ is used as a chip-select for the MC68183. The SCK is a clock supplied by the host MCU. The data from the host is transmitted on the MOSI line. The data from the MC68183 is transmitted on the MISO line.

Timing requirements for SPI communication are specified in Section 3.7, “Serial Peripheral Interface Timing.”

B.1 Packet Communication Initiated by the Host

When the host sends a packet to the MC68183 (as shown in Figure B-1), it performs the following steps:

1. Selects the MC68183 by driving the SS pin low.
2. Waits for the MC68183 to drive the READY pin low.
3. Sends the 32-bit packet.
4. Deselects the MC68183 by driving the SS pin high.
5. Repeats steps 1 through 4 for each additional packet.

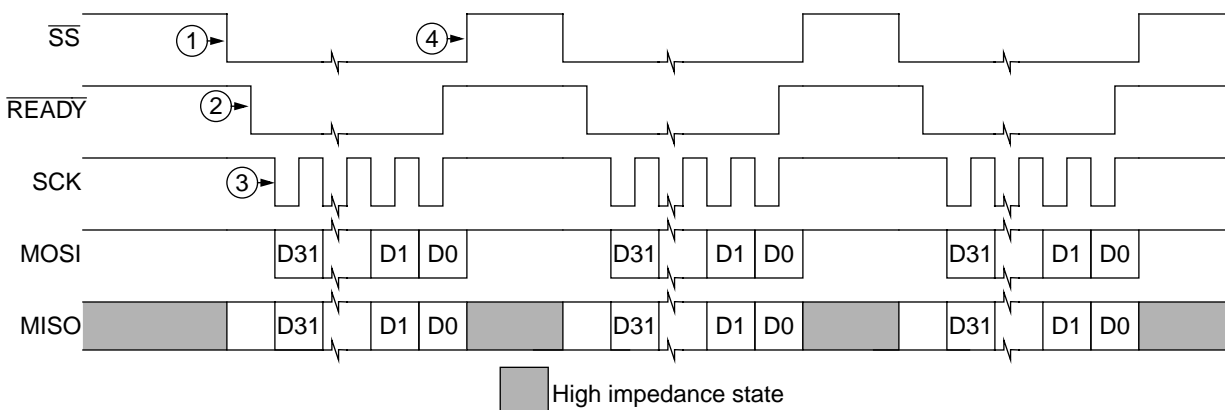


Figure B-1. Typical Multiple-Packet Communications Initiated by the Host

When the host sends a packet, it will also receive a valid packet from the MC68183. If the MC68183 is enabled and has no other packets waiting to be sent, MC68183 will send a status packet. (See Section C.1, “Checksum Packet,” for a definition of “enabled.”)

The host must transition the $\overline{\text{SS}}$ pin from high to low to begin each 32-bit packet. The MC68183 must see a negative transition on the $\overline{\text{SS}}$ pin in order for the host to initiate each packet communication.

B.2 Packet Communication Initiated by MC68183

When the MC68183 has a packet for the host to read, the following occurs:

1. The MC68183 drives the $\overline{\text{READY}}$ pin low.
2. If the MC68183 is not already selected, the host selects the MC68183 by driving the $\overline{\text{SS}}$ pin low.
3. The host receives (and sends) a 32-bit packet.
4. The host deselects the MC68183 by driving the $\overline{\text{SS}}$ pin high (optional).

See Figure B-2 for a diagram of this process.

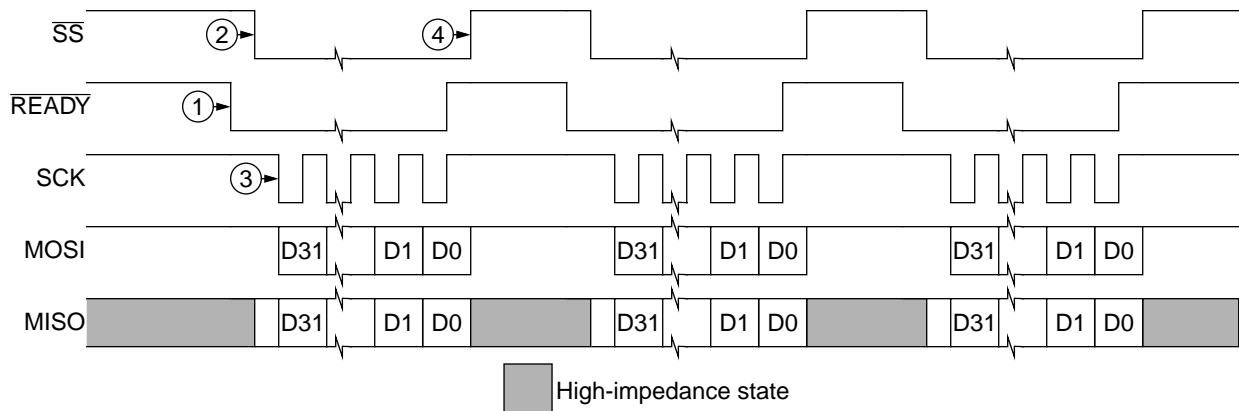


Figure B-2. Typical Multiple-Packet Communications Initiated by MC68183

When the host is reading a packet from the MC68183, it must send a valid packet to the MC68183. If the host has no data to send, it is suggested that the host send a checksum packet with all of the data bits set to 0 in order to avoid disabling the MC68183. See Section C.1, “Checksum Packet,” for more details on enabling and disabling the MC68183.

Figure B-3 illustrates that the MC68183 need not be deselected between packets when the packets are initiated by the MC68183.

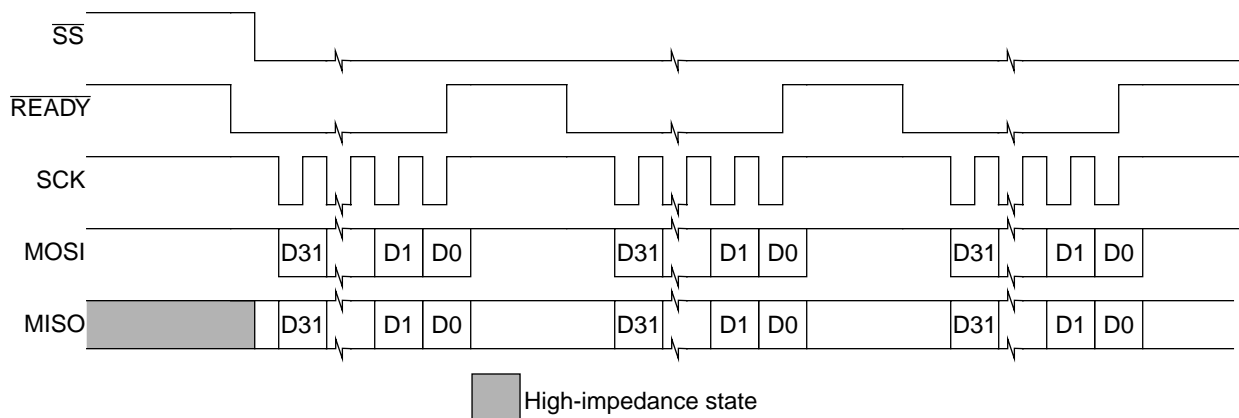


Figure B-3. Multiple-Packet Communications Initiated by the MC68183 with No Deselect

B.3 Host-to-Decoder Packet Map

The upper 8 bits of a packet comprise the packet ID. Table B-1 describes the packet IDs for all packets that can be sent to the MC68183 from the host.

Table B-1. Host-to-Decoder Packet ID Map

Packet ID (Hexadecimal)	Packet Type
00	Checksum
01	Configuration
02	Control
03	All frame mode
04	Operator message address enables (new in MC68183)
05	Roaming control packet (new in MC68183)
06	Timing control packet (new in MC68183)
07 - 0E	Reserved (host should never send)
0F	Receiver line control
10	Receiver control configuration (off setting)
11	Receiver control configuration (warm-up 1 setting)
12	Receiver control configuration (warm-up 2 setting)
13	Receiver control configuration (warm-up 3 setting)
14	Receiver control configuration (warm-up 4 setting)
15	Receiver control configuration (warm-up 5 setting)
16	Receiver control configuration (3200sps sync setting)
17	Receiver control configuration (1600sps sync setting)
18	Receiver control configuration (3200sps data setting)
19	Receiver control configuration (1600sps data setting)
1A	Receiver control configuration (shut-down 1 setting)
1B	Receiver control configuration (shut-down 2 setting)
1C–1F	Special (ignored by MC68183)
20	Frame assignment (frames 112 through 127)
21	Frame assignment (frames 96 through 111)
22	Frame assignment (frames 80 through 95)

Table B-1. Host-to-Decoder Packet ID Map (Continued)

Packet ID (Hexadecimal)	Packet Type
23	Frame assignment (frames 64 through 79)
24	Frame assignment (frames 48 through 63)
25	Frame assignment (frames 32 through 47)
26	Frame assignment (frames 16 through 31)
27	Frame assignment (frames 0 through 15)
28–77	Reserved (host should never send)
78	User address enable
79–7F	Reserved (host should never send)
80	User address assignment (user address 0)
81	User address assignment (user address 1)
82	User address assignment (user address 2)
83	User address assignment (user address 3)
84	User address assignment (user address 4)
85	User address assignment (user address 5)
86	User address assignment (user address 6)
87	User address assignment (user address 7)
88	User address assignment (user address 8)
89	User address assignment (user address 9)
8A	User address assignment (user address 10)
8B	User address assignment (user address 11)
8C	User address assignment (user address 12)
8D	User address assignment (user address 13)
8E	User address assignment (user address 14)
8F	User address assignment (user address 15)
90 - FF	Reserved (host should never send)

B.4 Decoder-to-Host Packet Map

Table B-2 describes the packet IDs for all of the packets that can be sent to the host from the MC68183.

Table B-2. Decoder-to-Host Packet ID Map

Packet ID (Hexadecimal)	Packet Type
00	Block information word
01	Address
02–57	Vector or message (ID is word number in frame)
58–5F	Reserved
60	Roaming status packet (new in MC68183)
61–7D	Reserved
7E	Receiver shut-down (new in MC68183)
7F	Status
80–FE	Reserved
FF	Part ID

Appendix C Host-to-Decoder Packet Descriptions

The following sections describe the packets of information sent from the host to the MC68183. In all cases the packets should be sent MSB first (bit 7 of byte 3 = bit 31 of the packet = MSB).

C.1 Checksum Packet

The checksum packet is used to ensure proper communication between the host and the MC68183. The MC68183 “exclusive-or’s” the 24 data bits of every packet it receives (except the checksum packet and the special packet IDs 1C through 1F hexadecimal) with an internal checksum register.

Upon reset and whenever the host writes a packet to the MC68183, the MC68183 is disabled from sending any information to the host processor until the host processor sends a checksum packet with the proper checksum value (CV) to the MC68183. When the MC68183 is disabled in this way, it prompts the host to read the part ID packet.

Note: All other operation continues normally when the MC68183 is “disabled.” Disabled implies only that data cannot be read. All other internal operations continue to function.

When the MC68183 is reset, it is disabled and the internal checksum register is initialized to the 24-bit part ID defined in the part ID packet. See Section D.8, “Part ID Packet,” for a description of the part ID. Every time a packet other than the checksum packet and special packets 1C through 1F are sent to the decoder IC, the value sent in the 24 information bits is “exclusive-or’ed” with the internal checksum register, the result is stored back to the checksum register, and the MC68183 is disabled.

If a checksum packet is sent and the CV bits match the bits in the checksum register, the MC68183 is enabled. If a checksum packet is sent when the MC68183 is already enabled, the packet is ignored by the MC68183. If a packet other than the checksum packet is sent when the MC68183 is enabled, the decoder IC will be disabled until a checksum packet is sent with the correct CV bits.

When the host reads a packet out of the MC68183 but has no data to send, the checksum packet should be sent so the MC68183 will not be disabled. The data in the checksum packet could be a null packet (32-bit stream of all zeros) since a checksum packet will not disable the MC68183. When the host reconfigures the MC68183, the MC68183 will be disabled from sending any packets other than the part ID packet until the MC68183 is enabled with a checksum packet having the proper data. The ID of the checksum packet is 0. Figure C-1 shows the checksum flow chart. Refer to Table C-1 for bit assignments.

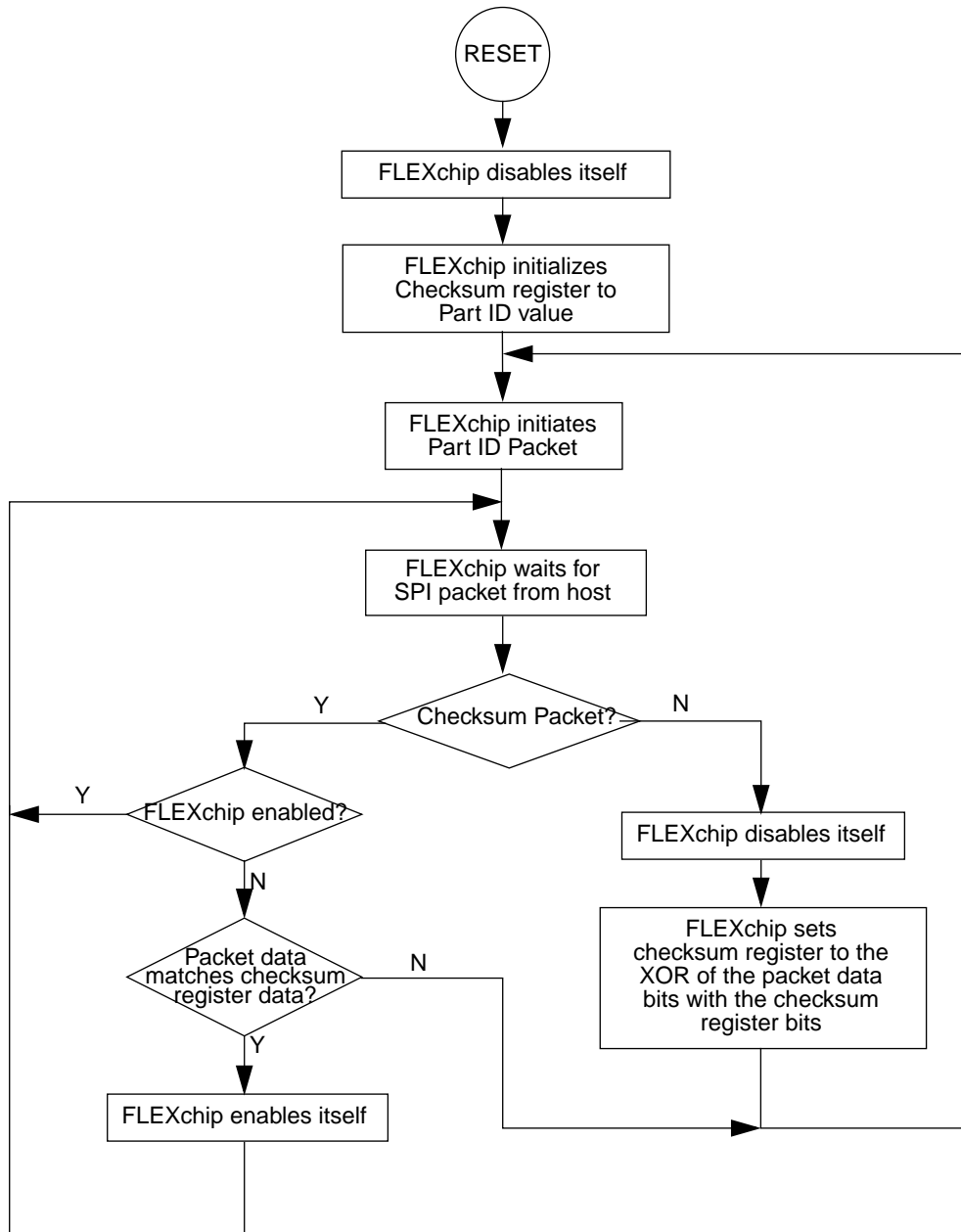


Figure C-1. MC68183 Checksum Flow Chart

Table C-1. Checksum Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	0
Byte 2	CV ₂₃	CV ₂₂	CV ₂₁	CV ₂₀	CV ₁₉	CV ₁₈	CV ₁₇	CV ₁₆
Byte 1	CV ₁₅	CV ₁₄	CV ₁₃	CV ₁₂	CV ₁₁	CV ₁₀	CV ₉	CV ₈

Table C-1. Checksum Packet Bit Assignments (Continued)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	CV ₇	CV ₆	CV ₅	CV ₄	CV ₃	CV ₂	CV ₁	CV ₀

Note: CV = Checksum value

C.2 Configuration Packet

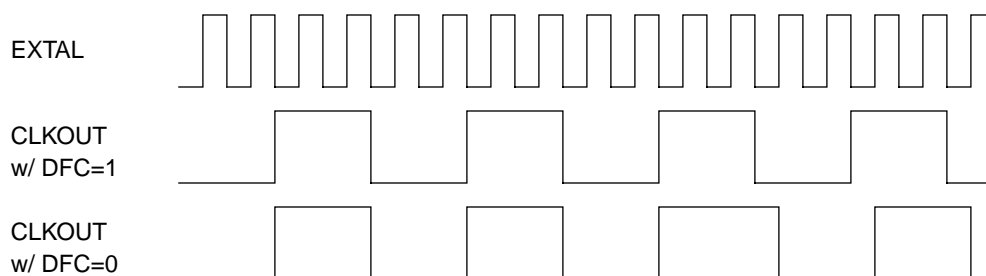
The configuration packet defines a number of different configuration options for the MC68183. Proper operation is not guaranteed if these settings are changed when decoding is enabled (i.e. the ON bit in the control packet is set). The ID of the configuration packet is 1. Table C-2 shows bit assignments.

Table C-2. Configuration Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	1
Byte 2	0	DFC	0	0	0	IDE	OFD ₁	OFD ₀
Byte 1	0	0	0	0	0	PCE	SP ₁	SP ₀
Byte 0	SME	MOT	COD	MTE	LBP	ICO	0	0

C.2.1 Bit Descriptions

DFC: Disable Fractional Clock. When DFC and IDE are set, the CLKOUT signal will generate a 40 kHz signal (EXTAL divided by 4),. When DFC is cleared and IDE is set, the CLKOUT signal will generate 38.4 kHz signal (EXTAL fractionally divided by 25/6; see Figure C-2). This bit has no effect when IDE is cleared. (Value after reset = 0.)

**Figure C-2. Disable Fraction Clock**

IDE: Internal Demodulator Enable. When IDE is set, the internal demodulator is enabled and the clock frequency at EXTAL is expected to be 160 kHz. When this bit is cleared, the internal demodulator is disabled and the clock frequency at EXTAL is expected to be 76.8 kHz. (Value after reset = 0.)

OFD: Oscillator Frequency Difference. The OFD bits describe the maximum difference in the frequency of the 76.8 kHz oscillator crystal with respect to the frequency of the transmitter. (Refer to Table C-3). These limits should be the worst-case difference in frequency due to all conditions including but not limited to aging, temperature, and manufacturing tolerance. Using a smaller frequency difference in this packet will result in lower power consumption due to higher receiver battery save ratios. Note that this value is not the absolute error of the oscillator frequency provided to the MC68183. The absolute error of the clock used by the FLEX transmitter must be taken into account. (For example, if the transmitter tolerance is +/- 25 ppm and the oscillator tolerance is +/-140 ppm, the oscillator frequency difference is +/- 165 ppm and OFD should be set to 0.)(Value after reset = 0.)

Table C-3. Oscillator Frequency Difference

OFD ₁ OFD ₀	Frequency Difference
00	+/- 300 ppm
01	+/- 150 ppm
10	+/- 75 ppm
11	+/- 0 ppm

PCE: Partial Correlation Enable. When PCE is set, partial correlation of addresses is enabled. When partial correlation is enabled, the MC68183 will shut down the receiver before the end of the last FLEX block that contains addresses, but only if it can determine that none of the addresses in that FLEX block will match any enabled address in the MC68183. When this bit is cleared, the receiver will be controlled as it was in previous versions of the IC. (Value after reset = 0.)

SP: Signal Polarity. The SP bits set the polarity of EXTS1 and EXTS0 input signals. (Refer to Table C-4.) Their value after reset is 0. The polarity of the EXTS0 and EXTS1 bits will be determined by the receiver design.

Table C-4. Polarity Settings for EXTS Signals

SP ₁ SP ₀	Signal Polarity		FSK Modulation @ SP = 0,0	EXTS1	EXTS0
	EXTS1	EXTS0			
00	Normal	Normal	+ 4800 Hz	1	0
01	Normal	Inverted	+1600 Hz	1	1
10	Inverted	Normal	- 1600 Hz	0	1
11	Inverted	Inverted	- 4800 Hz	0	0

SME: Synchronous Mode Enable. When SME is set, a status packet will be automatically sent whenever the synchronous mode update (SMU) bit in the status packet is set. The host can use the synchronous mode (SM) bit in the status packet as an in-range/out-of-range indication. (Value after reset = 0).

- MOT:** Maximum Off-Time. MOT has no effect if AST in the timing control packet is non-zero. When AST=0 and MOT=0, asynchronous A-word searches will time-out in 4 minutes. When AST=0 and MOT=1, asynchronous A-word searches will time-out in 1 minute. (Value after reset = 0.)
- COD:** Clock Output Disable. When COD is clear, a 38.4 kHz or 40 kHz signal (depending on the values of IDE and DFC) will be output on the CLKOUT pin. When COD is set, the CLKOUT pin will be driven low. Note that setting and clearing COD can cause pulses on the CLKOUT pin that are less than one-half the clock period. Also note that when the clock output is enabled and not set for intermittent operation (e.g., ICO in this packet), the CLKOUT pin will always output the clock signal even when the MC68183 is in reset (as long as the MC68183 oscillator is seeing clocks). Further note that when the FLEXchip is used in internal demodulator mode (i.e., when it uses a 160 kHz oscillator), the CLKOUT pin will be 80 kHz from reset until the IDE bit is set. This is because the MC68183 defaults to external demodulator mode at reset. (Value after reset = 0.)
- MTE:** Minute Timer Enable. When MTE is set, a status packet will be sent at 1-minute intervals with the minute time-out (MT) bit in the status packet set. When this bit is clear, the internal 1-minute timer stops counting. The internal 1-minute timer is reset when this bit is changed from 0 to 1 or when the minute timer clear (MTC) bit in the control packet is set. Note that the minute timer will not be accurate using a 160 kHz oscillator until the IDE bit is set. (Value after reset = 0.)
- LBP:** Low Battery Polarity. LBP defines the polarity of the MC68183's LOBAT pin. The LB bit in the status packet is initialized to the inverse value of this bit when the MC68183 is turned on (by setting the ON bit in the control packet). When the MC68183 is turned on, the first low-battery update in the status packet will be sent to the host when a low-battery condition is detected on the LOBAT pin. Setting this bit means that a high on the LOBAT pin indicates a low-voltage condition. (value after reset = 0)
- ICO:** Intermittent Clock Out. When ICO is clear and COD is clear, a 38.4 kHz or 40 kHz signal (depending on the values of IDE and DFC) will be output on the CLKOUT pin. When ICO is set and COD is clear, the clock will only be output on the CLKOUT pin while the receiver is not in the off state. The clock will be output for a few cycles before the receiver transitions from the off state and for a few cycles after the receiver transitions to the off state. This ensures that the receiver receives enough clocks to detect and process the changes to and from the off state). The CLKOUT pin will be driven low when it is not driving a clock. Note that when the clock is automatically enabled and disabled (i.e., when ICO is set), the CLKOUT signal transitions will be clean (i.e., no pulses of less than half the clock period) when it transitions between no-clock and clocked output. This bit has no effect when COD is set. (Value after reset = 0.)

C.3 Control Packet

The control packet defines a number of different control bits for the MC68183. The ID of the control packet is 2. See Table C-5 for bit assignments.

Table C-5. Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	1	0

Table C-5. Control Packet Bit Assignments (Continued)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 2	FF ₇	FF ₆	FF ₅	FF ₄	FF ₃	FF ₂	FF ₁	FF ₀
Byte 1	0	SPM	PS ₁	PS ₀	0	0	0	0
Byte 0	0	SBI	0	MTC	0	0	EAE	ON

FF: Force Frame 0-7. The FF bits enable and disable forcing the MC68183 to look in frames 0 through 7. When an FF bit is set, the MC68183 will decode the corresponding frame. Unlike the AF bits in the frame assignment packets, the system collapse of a FLEX system will not affect frames assigned using the FF bits. For example, setting AF₀ to 1 when the system collapse is 5 will cause the decoder to decode frames 0, 32, 64, and 96, whereas setting FF₀ to 1 when the system collapse is 5 will only cause the decoder to decode frame 0. This may be useful for acquiring transmitted time information or channel attributes (e.g., local ID). (Value after reset = 0.)

SPM: Single Phase Mode. When SPM is set, the MC68183 will decode only one phase of the transmitted data. When SPM is clear, the MC68183 will decode all phases it receives. A change to this bit while the MC68183 is on will not take effect until the next block 0 of the next decoded frame. (Value after reset = 0.)

PS: Phase Select. When the SPM bit is set, the PS bits define what phase the MC68183 should decode, in accordance with Figure C-6. This value is determined by the service provider. A change to the PS bits while the MC68183 is on will not take effect until the next block 0 of a frame. (Value after reset = 0.) Table C-6 shows PS values and phase decodes.

Table C-6. Phase Select

PS Value	Phase Decoded (Based on FLEX Data Rate)		
	PS ₁ PS ₀	1600bps	3200bps
00	a	a	a
01	a	a	b
10	a	c	c
11	a	c	d

SBI: Send Block Information, words 2–4. When SBI is set, any errored or time-related block information words 2–4 will be sent to the host. See Figure D-1 for a description of the words sent. (Value after reset = 0.)

MTC: Minute Timer Clear. Setting MTC will cause the 1-minute timer to restart from 0.

EAE: End of Addresses Enable. When EAE is set, the EA bit in the status packet will be set immediately after FLEXchip decodes the last address word in the frame if any of the enabled FLEXchip addresses was detected in the frame. When EAE is cleared, the EA bit will never be set.

ON: Turn On Decoder. ON is set if the MC68183 should be decoding FLEX signals. ON is clear if signal processing should be off (very low-power mode). If the ON bit is changed twice, and control packets making the changes are received within 2ms of each other, FLEXchip may ignore the double change and stay in its original state; for example, if ON is turned off, then on again within 2ms, ON may stay on and ignore the off pulse. It is therefore recommended that the host ensure a minimum of 2ms between changes in the ON bit. (Value after reset = 0.)

C.4 All Frame Mode Packet

The all frame mode packet is used to decrement temporary address enable counters by one, decrement the all frame mode counter by one, and/or enable or disable forcing all frame mode. All frame mode is enabled if any temporary address enable counter is nonzero, the all frame mode counter is nonzero, or the force all frame mode bit is set.

If all frame mode is enabled, the MC68183 will attempt to decode every frame and send a status packet with the end-of-frame (EOF) bit set at the end of every frame. Both the all frame mode counter and the temporary address enable counters can only be incremented internally by the MC68183 and can only be decremented by the host.

The MC68183 will increment a temporary address enable counter whenever a short instruction vector is received assigning the corresponding temporary address. See Section E.5, “Operation of a Temporary Address,” for details. The MC68183 will increment the all frame mode counter whenever an alphanumeric, HEX / binary, or secure vector is received.

When the host determines that a message associated with a temporary address or a fragmented message has ended, then the appropriate temporary address counter or all frame mode counter should be decremented by writing an all frame mode packet to the MC68183 in order to exit the all frame mode, thereby improving battery life. Neither the temporary address enable counters nor the all frame mode counter can be incremented past the value 127 (will not roll-over) or decremented past the value 0. The temporary address enable counters and the all frame mode counter are initialized to 0 at reset and when the decoder is turned off. The ID of the All Frame Mode Packet is 3. Table C-7 shows bit assignments for this packet.

Table C-7. All Frame Mode Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	1	1
Byte 2	DAF	FAF	0	0	0	0	0	0
Byte 1	DTA ₁₅	DTA ₁₄	DTA ₁₃	DTA ₁₂	DTA ₁₁	DTA ₁₀	DTA ₉	DTA ₈
Byte 0	DTA ₇	DTA ₆	DTA ₅	DTA ₄	DTA ₃	DTA ₂	DTA ₁	DTA ₀

DAF: Decrement All Frame counter. Setting DAF decrements the all frame mode counter by one. If a packet is sent with DAF clear, the all frame mode counter is not affected. (Value after reset = 0.)

FAF: Force All Frame mode. Setting FAF forces the MC68183 to enter all frame mode. If FAF is clear, the MC68183 may or may not be in all frame mode depending on the status of the all frame mode counter and the temporary address enable counters. This may be useful in acquiring transmitted time information. (Value after reset = 0.)

DTA: Decrement Temporary Address enable counter. When a bit in DTA is set, the corresponding temporary address enable counter is decremented by one. When a bit is cleared, the corresponding temporary address enable counter is not affected. When a temporary address enable counter reaches zero, the temporary address is disabled. (Value after reset = 0.)

C.5 Operator Messaging Address Enable Packet

The operator messaging address enable packet is used to enable and disable the built-in FLEX operator messaging addresses. Enabling and disabling operator messaging addresses does not affect what frames the decoder IC decodes. To decode the proper frames, the host must modify the FF bits in the control packet or the AF bits in the frame assignment packets. The ID of the operator messaging address enable packet is 4. See Table C-8 for bit assignments.

Table C-8. System Address Enable Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	1	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	OAE ₁₅	OAE ₁₄	OAE ₁₃	OAE ₁₂	OAE ₁₁	OAE ₁₀	OAE ₉	OAE ₈
Byte 0	OAE ₇	OAE ₆	OAE ₅	OAE ₄	OAE ₃	OAE ₂	OAE ₁	OAE ₀

OAE: Operator messaging Address Enable. When a bit is set, the corresponding operator messaging address is enabled. When it is cleared, the corresponding operator messaging address is disabled. OAE₀ through OAE₁₅ correspond to the hexadecimal operator messaging address values of 1F7810 through 1F781F, respectively. (Value after reset = 0.)

C.6 Roaming Control Packet

The roaming control packet controls the features of the MC68183 that allow implementation of a roaming device. The ID of the roaming control packet is 5. See Table C-9 for bit assignments.

Table C-9. Roaming Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	1	0	1
Byte 2	IRS	NBC	MCM	IS1	SDF	RSP	SND	CND
Byte 1	RND	ABI	SAS	DAS	0	0	0	0
Byte 0	0	0	MFC ₁	MFC ₀	0	0	MCO ₁	MCO ₀

IRS: Ignore Resynchronization Signal. When IRS is set, FLEXchip will not go asynchronous when detecting an Ar or $\overline{\text{Ar}}$ signal during searches for A-words. It will merely report that the resynchronization signal was received by setting RSR to 1 in the roaming status packet. This

- allows the host to decide what to do when the paging device is synchronous to more than one channel and only one channel is sending the resynchronization signal. It also prevents the FLEXchip from losing synchronization when it detects the resynchronization signal while the paging device is checking an unknown channel. This bit is set and cleared by the host. (Value after reset = 0.)
- NBC:** Network Bit Check. Setting NBC will enable reporting of the received network bit value (NBU and n) in the roaming status packet. Setting NBC also makes the FLEXchip abandon a frame after the frame info word without synchronizing to the frame if the frame information word is uncorrectable or if the n bit in the frame information word is not set.
- If the MC68183 was in synchronous mode when the abandon occurred (probably due to synchronizing to a second channel), it will maintain synchronization to the original channel. If the MC68183 was in asynchronous mode, it will stay in asynchronous mode and end the A-word search. to avoid synchronizing to a nonroaming channel when searching for roaming channels. This bit is set and cleared by the host. (Value after reset = 0.)
- MCM:** Manual Collapse Mode. When MCM is set, FLEXchip behaves as if the system collapse were 7. FLEXchip will not apply the received system collapse to the AF bits. When MCM is set, the received system collapse is reported to the host via SCU and RSC in the roaming status packet so the host can modify the AF bits based on the system collapse of the channel. MCM is set and cleared by the host. (Value after reset = 0)
- IS1:** Invert EXTS1. Setting IS1 inverts the expected polarity of the EXTS1 pin from the way it is configured by SP₁ in the configuration packet. For example, if both IS1 and SP₁ are set, the polarity of the EXTS1 pin is untouched. IS1 is intended to be changed when a change in a channel changes the polarity of the received signal. IS1 is set and cleared by the host and has the equivalent effect when using the internal demodulator. (Value after reset = 0.)
- SDF:** Stop Decoding Frame. Setting SDF causes the FLEXchip to stop decoding a frame without losing frame synchronization. SDF is set by the host and cleared by FLEXchip once it has been processed. The packet with the SDF bit set must be sent after receiving the status packet with EA bit set. It must be sent within 40ms of the end of block in which FLEXchip set the EA bit. (Value after reset = 0.)
- RSP:** Receiver Shutdown Packet enable. When RSP is set, a receiver shutdown packet will be sent whenever the receiver is shut down. The receiver shutdown packet informs the host both that the receiver has shut down and of the time it will take for FLEXchip to automatically warm up the receiver. (Value after reset = 0.)
- SND:** Start Noise Detect. Setting SND while the FLEXchip is battery saving will cause it to warm up the receiver, run a noise detect, and report the result of the noise-detect via NDR in the roaming status packet. SND is set by the host and cleared by FLEXchip once it has been processed. If the time comes for FLEXchip to warm up automatically, or if the SAS bit is set while an SND is being processed, the noise-detect will be abandoned and the abandoned noise-detect result (NDR = 01) will be sent in the roaming status packet. (Value after reset = 0.)
- CND:** Continuous Noise Detect. Setting CND will cause FLEXchip to do continuous noise detects during the decoded block data of a frame. The results of the noise-detect will only be reported if noise is detected (NDR = 11). Only one noise-detected result (NDR=11) will be sent per block. If the FLEXchip has not completed a noise-detect when it shuts down for the frame, that noise-detect will be abandoned, but no abandon result (NDR=01) will be sent. This bit is set and cleared by the host. (Value after reset = 0.)

- RND:** Report Noise Detects. Setting RND will cause FLEXchip to report the results of the noise-detects it does under normal asynchronous operation (when first turned on and when asynchronous). The results of the noise-detect will be reported via NDR in the roaming status packet. This bit is set and cleared by the host. (Value after reset = 0.)
- ABI:** All Block Information words. When ABI is set, FLEXchip will send all received block information words 2-4 to the host. Note that setting the SBI bit only in the control packet enables errored and real-time clock-related block info words. (Value after reset = 0.)
- SAS:** Start A-word Search. Setting SAS while in asynchronous battery save mode will cause FLEXchip to warm up the receiver and run an A-word search. If, during the A-word search, the MC68183 finds sufficient FLEX signal, it will enter synchronous mode and start decoding the frame. If the A-word search times-out without finding sufficient FLEX signal, it will battery-save and continue periodic noise detects.
- The time-out for the A-word searches is controlled by the AST bits in the timing control packet and the MOT bit in the configuration packet. The A-word search takes priority over noise-detects. Therefore, if FLEXchip is performing an A-word search and the time comes to do automatic noise-detect, the noise-detect will not be performed. This bit is set by the host and cleared by FLEXchip once it has been acted on. (Value after reset = 0.)
- DAS:** Disable A-word Search. When DAS is set, an A-word search will not automatically occur after a noise-detect in asynchronous mode finds FLEX signal. This includes automatic noise-detects and noise-detects initiated by the host by setting SND. FLEXchip will shut down the receiver after the noise-detect completes regardless of the result. When this bit is cleared, A-word searches will occur after a noise-detect finds signal in asynchronous mode. (Value after reset = 0.)
- MFC:** Missed Frame Control. The MFC bits control the frames for which missing frame data (MS1, MFI, MS2, MBI, and MAW) is reported in the roaming status packet, as shown in Table C-10. (Value after reset = 0.)

Table C-10. Missing Frame Control

MFC₁MFC₀	Missing Frame Data Reported
00	Never
01	Only during frames 0 through 3
10	Only during frames 0 through 7
11	Always

- MCO:** Maximum Carry On. The value of the MCO bits sets the maximum carry on that FLEXchip will follow. For example, if FLEXchip receives a carry-on of 3 over the air and MCO is set to 1, FLEXchip will only carry on for one frame. (Value after reset = 3.)

C.7 Timing Control Packet

The timing control packet gives the host control of the timing used when FLEXchip is in asynchronous mode. The packet ID for the timing control packet is 6. See Table C-11 for bit assignments in this packet.

Table C-11. Timing Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	1	1	0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	AST ₇	AST ₆	AST ₅	AST ₄	AST ₃	AST ₂	AST ₁	AST ₀
Byte 0	ABT ₇	ABT ₆	ABT ₅	ABT ₄	ABT ₃	ABT ₂	ABT ₁	ABT ₀

AST: A-word Search Time. The value of the AST bits sets the A-word search time for all asynchronous A-word searches in units of 80ms (value of 1 is 80ms, value of 2 is 160ms, etc.) If the value is 0, FLEXchip defaults to the 1-minute (MOT=1) or 4-minute (MOT=0) A-word search time controlled by the MOT bit in the configuration packet. (Value after reset = 0.)

ABT: Asynchronous Battery-save Time. The value of the ABT bits sets the battery-save time (time measured from beginning of one automatic noise detect to beginning of the next) in asynchronous mode in units of 80ms (value of 1 is 80ms, value of 2 is 160ms, etc.) If the value is 0, the battery-save time is set to the default value of 1.5 seconds. Because the minimum allowed ABT is 320ms, values of 1, 2, 3, and 4 are invalid. (Value after reset = 0.)

C.8 Receiver Line Control Packet

This packet gives the host control over the settings on the receiver control lines (S0-S7) in all modes except reset. In reset, the receiver control lines are in high impedance settings. The ID for the receiver line control packet is 15 (decimal). Refer to Table C-12 for receiver line control packet bit assignments.

Table C-12. Receiver Line Control Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	1	1	1	1
Byte 2	0	0	0	0	0	0	0	0
Byte 1	FRS ₇	FRS ₆	FRS ₅	FRS ₄	FRS ₃	FRS ₂	FRS ₁	FRS ₀
Byte 0	CLS ₇	CLS ₆	CLS ₅	CLS ₄	CLS ₃	CLS ₂	CLS ₁	CLS ₀

FRS: Force Receiver Setting. Setting a bit to 1 will cause the corresponding CLS bit in this packet to override the internal receiver control settings on the corresponding receiver control line (S0-S7). Clearing a bit gives control of the corresponding receiver control lines (S0-S7) back to the MC68183. (Value after reset = 0.)

CLS: Control Line Setting. If the corresponding FRS bit was set in the receiver line control packet, the CLS bits define the setting that should be applied to corresponding receiver control lines. (Value after reset = 0.)

C.9 Receiver Control Configuration Packets

These packets allow the host to configure which setting is applied to receiver control lines S0-S7, how long to apply the setting, and when to read the value of the LOBAT input pin. The MC68183 defines 12 different receiver control settings.

Note: Proper operation is not guaranteed if these settings are changed when decoding is enabled (i.e., when ON in the control packet is set).

The IDs for these packets range from 16 to 27 (decimal).

C.10 Receiver-Off Setting Packet

Refer to Table C-13 for bit assignments for this packet.

Table C-13. Receive-Off Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	0	0	0	0
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS ₇	CLS ₆	CLS ₅	CLS ₄	CLS ₃	CLS ₂	CLS ₁	CLS ₀
Byte 0	ST ₇	ST ₆	ST ₅	ST ₄	ST ₃	ST ₂	ST ₁	ST ₀

LBC: Low Battery Check. If LBC is set, the MC68183 will check the status of the LOBAT port just before leaving this receiver state. (Value after reset = 0.)

CLS: Control Line Setting. CLS is the value to be output on the receiver control lines (S0-S7) for this receiver state. (Value after reset = 0.)

ST: Step Time. ST is the time the MC68183 is to keep the receiver off before applying the first warm-up state's receiver control value to the receiver control lines. The setting is in steps of 625us. Valid values are 625us (ST=01) to 159.375ms (ST=FF in hexadecimal). (Value after reset = 625us)

C.10.1 Receiver Warm-Up Setting Packets

Refer to Table C-14 for bit assignments for this packet.

Table C-14. Receiver Warm-Up Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	0	s ₂	s ₁	s ₀
Byte 2	SE	0	0	0	LBC	0	0	0
Byte 1	CLS ₇	CLS ₆	CLS ₅	CLS ₄	CLS ₃	CLS ₂	CLS ₁	CLS ₀

Table C-14. Receiver Warm-Up Setting Packet Bit Assignments (Continued)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	0	ST ₆	ST ₅	ST ₄	ST ₃	ST ₂	ST ₁	ST ₀

s: Setting Number. This receiver-control setting determines which of the receiver warm-up setting packet's values are to be applied. Table C-15 shows the names for each value of s that applies to this packet.

Table C-15. Receiver Warm-Up Setting Names

S ₂ S ₁ S ₀	Setting Name
001	Warm-up 1
010	Warm-up 2
011	Warm-up 3
100	Warm-up 4
101	Warm-up 5

- SE:** Step Enable. The receiver setting is enabled when the bit is set. If a step in the warm-up sequence is disabled, the disabled step and all remaining steps will be skipped. (Value after reset = 0.)
- LBC:** Low Battery Check. If LBC is set, the MC68183 will check the status of the LOBAT port just before leaving this receiver state. (Value after reset = 0.)
- CLS:** Control Line Setting. CLS is the value to be output on the receiver control lines (S₀–S₇) for this receiver state. (Value after reset = 0.)
- ST:** Step Time. ST is the time the MC68183 is to wait before applying the next state's receiver control value to the receiver control lines. The setting is in steps of 625us. Valid values are 625us (ST=01) to 79.375ms (ST=7F in hexadecimal). (Value after reset = 625us.)

C.10.2 3200sps Sync-Setting Packets

Refer to Table C-16 for bit assignments.

Table C-16. 3200sps Sync-Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	0	1	1	0
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS ₇	CLS ₆	CLS ₅	CLS ₄	CLS ₃	CLS ₂	CLS ₁	CLS ₀
Byte 0	0	ST ₆	ST ₅	ST ₄	ST ₃	ST ₂	ST ₁	ST ₀

- LBC:** Low Battery Check. If LBC is set, the MC68183 will check the status of the LOBAT port just before leaving this receiver state. (Value after reset = 0.)
- CLS:** Control Line Setting. CLS is the value to be output on the receiver control lines (S0-S7) for this receiver state. (Value after reset = 0.)
- ST:** Step Time. ST is the time the MC68183 is to wait before expecting good signals on the EXTS1 and EXTS0 signals after warming up. The setting is in steps of 625us. Valid values are 625us (ST=01) to 79.375ms (ST=7F in hexadecimal). (Value after reset = 625us.)

C.10.3 Receiver-On Setting Packets

Refer to Table C-17 for bit assignments.

Table C-17. Receiver-On Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	s ₃	s ₂	s ₁	s ₀
Byte 2	0	0	0	0	LBC	0	0	0
Byte 1	CLS ₇	CLS ₆	CLS ₅	CLS ₄	CLS ₃	CLS ₂	CLS ₁	CLS ₀
Byte 0	0	0	0	0	0	0	0	0

s: Setting Number. This is the receiver control setting for which this packet's values are to be applied. Table C-18 shows the names for each value of s that applies to this packet.

Table C-18. Receiver On Setting Name

s ₃ s ₂ s ₁ s ₀	Setting Name
0111	1600sps sync
1000	3200sps data
1001	1600sps data

- LBC:** Low Battery Check. If LBC bit is set, the MC68183 will check the status of the LOBAT port just before leaving this receiver state. (Value after reset = 0.)
- CLS:** Control Line Setting. CLS is the value to be output on the receiver control lines (S0-S7) for this receiver state. (Value after reset = 0.)

C.10.4 Receiver Shut-Down Setting Packets

Refer to Table C-19 for bit assignments.

Table C-19. Receiver Shut-Down Setting Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	1	1	0	1	s
Byte 2	SE	0	0	0	LBC	0	0	0
Byte 1	CLS ₇	CLS ₆	CLS ₅	CLS ₄	CLS ₃	CLS ₂	CLS ₁	CLS ₀
Byte 0	0	0	ST ₅	ST ₄	ST ₃	ST ₂	ST ₁	ST ₀

s: Setting Number. Receiver control setting for which this packet's values are to be applied. The following truth table shows the names of each of the values for s that apply to this packet.

Table C-20. Receiver Shut-Down Setting Names

s	Setting Name
0	Shut-down 1
1	Shut-down 2

SE: Step Enable. The receiver setting is enabled when the bit is set. If a step in the shut-down sequence is disabled, all steps following the disabled step will be ignored. (Value after reset = 0.)

LBC: Low Battery Check. If this bit is set, the MC68183 will check the status of the LOBAT port just before leaving this receiver state. (Value after reset = 0.)

CLS: Control Line Setting. CLS is the value to be output on the receiver control lines (S0-S7) for this receiver state. (Value after reset = 0.)

ST: Step Time. ST is the time the MC68183 is to wait before applying the next state's receiver control value to the receiver control lines. The setting is in steps of 625us. Valid values are 625us (ST=01) to 39.375ms (ST=3F in hexadecimal). (Value after reset = 625us.)

C.11 Frame Assignment Packets

The FLEX protocol defines that each address of a FLEX pager is assigned a home frame and a battery cycle. The MC68183 must be configured so a frame that is assigned by one or more of the addresses' home frames and battery cycles has its corresponding configuration bit set. For example, if the MC68183 has one enabled address and it is assigned to frame 3 with a battery cycle of 4, the AF bits for frames 3, 19, 35, 51, 67, 83, 99, and 115 should be set and the AF bits should be cleared for all other frames.

When the MC68183 is configured for manual collapse mode by setting the MCM bit in the roaming control packet, the MC68183 will not apply the received system collapse to the AF bits. The host should set the AF bits for all frames that should be decoded on all channels. For example, if frames 0 and 64 should be decoded on one channel and frames 4, 36, 68, and 100 should be decoded on another channel, all six of the corresponding AF bits should be set. The host can then change the receiver's carrier frequency after the MC68183 decodes frames 0, 36, 64, and 100.

There are eight frame assignment packets. See Table C-21 for the packet bit assignments. The packet IDs for these packets range from 32 to 39 (decimal).

Table C-21. Frame Assignment Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	1	0	0	f_2	f_1	f_0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	AF_{15}	AF_{14}	AF_{13}	AF_{12}	AF_{11}	AF_{10}	AF_9	AF_8
Byte 0	AF_7	AF_6	AF_5	AF_4	AF_3	AF_2	AF_1	AF_0

f: Frame range. This value determines which 16 frames correspond to the 16 AF bits in the packet, in accordance with Table C-22. At least one of these bits must be set when the MC68183 is turned on by setting ON in the control packet. (Value after reset = 0.)

Table C-22. AF Bit/Frame Correspondence

$f_2f_1f_0$	AF_{15}	AF_0
000	Frame 127	Frame 112
001	Frame 111	Frame 96
010	Frame 95	Frame 80
011	Frame 79	Frame 64
100	Frame 63	Frame 48
101	Frame 47	Frame 32
110	Frame 31	Frame 16
111	Frame 15	Frame 0

AF: Assigned Frame. If a bit is set, the MC68183 will consider the corresponding frame to be assigned via an address's home frame and pager collapse. (Value after reset = 0.)

C.12 User Address Enable Packet

The user address enable packet is used to enable and disable the 16 user address words. Although the host is allowed to change the user address words while the MC68183 is decoding FLEX signals, the host must disable a user address word before changing it. The ID of the user address enable packet is 120 (decimal). Refer to Table C-23 for bit assignments.

Table C-23. User Address Enable Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	1	1	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 1	UAE ₁₅	UAE ₁₄	UAE ₁₃	UAE ₁₂	UAE ₁₁	UAE ₁₀	UAE ₉	UAE ₈
Byte 0	UAE ₇	UAE ₆	UAE ₅	UAE ₄	UAE ₃	UAE ₂	UAE ₁	UAE ₀

UAE: User Address Enable. When a bit is set, the corresponding user address word is enabled. When it is cleared, the corresponding user address word is disabled. UAE₀ corresponds to the user address word configured using a packet ID of 128, and UAE₁₅ corresponds to the user address word configured using a packet ID of 143. (Value after reset = 0.)

C.13 User Address Assignment Packets

The MC68183 has 16 user address words. Each word can be programmed to be a short address, part of a long address, or the first part of a network ID. The addresses are configured using the address assignment packets. Each user address can be configured as long or short and tone-only or regular (network IDs are short and regular).

Although the host is allowed to send these packets while the MC68183 is on, the host must disable the user address word by clearing the corresponding UAE bit in the user address enable packet before changing any of the bits in the corresponding user address assignment packet. This method allows for easy reprogramming of user addresses without disrupting normal operation. The IDs for these packets range from 128 to 143 (decimal). Refer to Table C-24 for bit assignments.

Table C-24. User Address Assignment Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	1	0	0	0	a ₃	a ₂	a ₁	a ₀
Byte 2	0	LA	TOA	A ₂₀	A ₁₉	A ₁₈	A ₁₇	A ₁₆
Byte 1	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈
Byte 0	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀

- a: User Address Word Number. Specifies which address word is being configured. A zero in this field corresponds to address index zero (AI = 0) in the address packet received from the MC68183 when an address is detected. See Section C.13, “User Address Assignment Packets,” for a description of the address index field.
- LA: Long address. When LA is set, the address is considered a long address. Both words of a long address must have this bit set. The first word of a long address must have an even address index and the second word must be in the address index immediately following the first word.

- TOA: Tone-Only Address. When this bit is set, the MC68183 will consider this address a tone-only address and will not decode a vector word when the address is received. If the TOA bit of a long address word is set, the TOA bit of the other word of the long address must also be set.
- A: Address word. This is the 21 bit value of the address word. Valid FLEX messaging addresses or network IDs may be used.

Appendix D Decoder-to-Host Packet Descriptions

The following sections describe the packets of information that will be sent from the MC68183 to the host. In all cases the packets are sent MSB first (bit 7 of byte 3 = bit 31 of the packet = MSB). The MC68183 decides what data should be sent to the host. If the MC68183 is disabled through the checksum feature the Part ID Packet will be sent. (See Section C.1, “Checksum Packet,” for a description of the checksum feature.) Data packets relating to data received over the air are buffered in the 32-packet transmit buffer. The data packets include block information word packets, address packets, vector packets, and message packets.

If the MC68183 is enabled and a receiver shut-down packet is pending, the receiver shut-down packet will be sent. If no receiver shut-down packet is pending, but there is a pending roaming status packet, the roaming status packet will be sent. If neither the receiver shutdown packet nor the roaming status packet is pending and there is data in the transmit buffer, a packet from the transmit buffer will be sent. Otherwise, the MC68183 will send the status packet (which is not buffered). In the event of a buffer overflow, the MC68183 will automatically stop decoding and clear the buffer.

It is recommended that the host be designed to empty the FIFO buffer every block with enough time left over to read a status packet. This would ensure that any applicable status packet would be received within 1 block of the new status being available. Figure D-1 diagrams the MC68183 SPI transmit functional block.

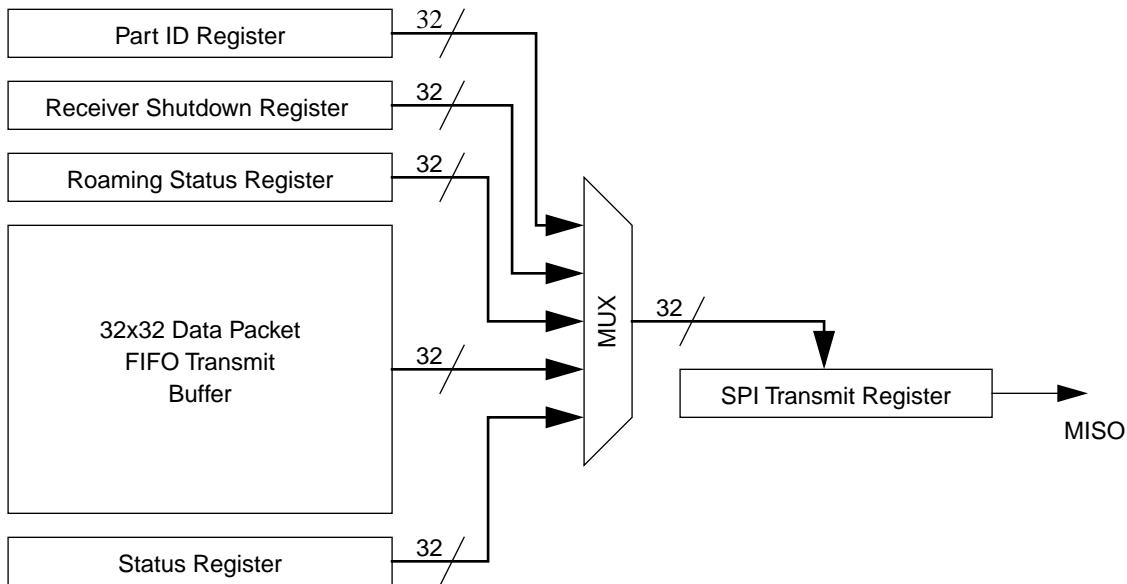


Figure D-1. MC68183 SPI Transmit Functional Block Diagram

D.1 Block Information Word Packet

The block information field is the first field following the synchronization codes of the FLEX protocol. This field contains information about the frame such as number of addresses and messages, information about current time, the channel ID, channel attributes, and so on. The first block

information word of each phase is used internally to the MC68183 and is never transmitted to the host, with the exception of the system collapse, which is sent to the host when FLEXchip is in manual collapse mode.

Time block information words 2-4 can be optionally sent to the host by setting the SBI bit in the control packet. (See Section C.3, "Control Packet.") All block information words 2-4 can be optionally sent to the host by setting the ABI bit in the roaming control packet.

When the SBI or ABI bit is set and any block information word 2-4 is received with an uncorrectable number of bit errors, the FLEXchip will send the block information word to the host with the e bit set regardless of the value of the f field in the block information word. The MC68183 does not support decoding of the vector and message words associated with the data/system message block info word (f=101). The ID of a block information word packet is 0 (decimal). See Table D-1 for bit assignments.

Table D-1. Block Information Word Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	0
Byte 2	e	p ₁	p ₀	x	x	f ₂	f ₁	f ₀
Byte 1	x	x	s ₁₃	s ₁₂	s ₁₁	s ₁₀	s ₉	s ₈
Byte 0	s ₇	s ₆	s ₅	s ₄	s ₃	s ₂	s ₁	s ₀

- e: Set if more than 2 bit errors are detected in the word or if the check character calculation fails after error correction has been performed.
- p: Phase on which the block information word was found (0 = a, 1 = b, 2 = c, 3 = d)
- x: Unused bits. The value of these bits is not guaranteed.
- f: Word Format Type. The value of these bits modify the meaning of the s bits in this packet as described in the BIW word descriptions in the s bit definition below.
- s: These are the information bits of the block information word. The definition of these bits depend on the f bits in this packet. Table D-2 describes the block information words.

Table D-2. Block Information Words

f ₂ f ₁ f ₀	s ₁₃ s ₁₂ s ₁₁ s ₁₀ s ₉ s ₈ s ₇ s ₆ s ₅ s ₄ s ₃ s ₂ s ₁ s ₀	Description
000 ¹	i ₈ i ₇ i ₆ i ₅ i ₄ i ₃ i ₂ i ₁ i ₀ C ₄ C ₃ C ₂ C ₁ C ₀	Local ID, coverage zone
001 ²	m ₃ m ₂ m ₁ m ₀ d ₄ d ₃ d ₂ d ₁ d ₀ Y ₄ Y ₃ Y ₂ Y ₁ Y ₀	Month, day, year
010 ²	S ₂ S ₁ S ₀ M ₅ M ₄ M ₃ M ₂ M ₁ M ₀ H ₄ H ₃ H ₂ H ₁ H ₀	Second, minute, hour
011 ¹	Reserved by FLEX protocol for future use	
100 ¹	Reserved by FLEX protocol for future use	
101 ²	z ₉ z ₈ z ₇ z ₆ z ₅ z ₄ z ₃ z ₂ z ₁ z ₀ A ₃ A ₂ A ₁ A ₀	System message

Table D-2. Block Information Words (Continued)

$f_2f_1f_0$	$S_{13} S_{12} S_{11} S_{10} S_9 S_8 S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0$	Description
110 ¹	Reserved by FLEX protocol for future use	
111 ¹	$C_9 C_8 C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0 T_3 T_2 T_1 T_0$	Country code, traffic management flags

1. Will be decoded only if the ABI bit is set.
2. Will be decoded only if the SBI or ABI bit is set.

D.2 Address Packet

The address field follows the block information field in the FLEX protocol and contains all addresses in the frame.

If fewer than three bit errors are detected in a received address word, and if it matches an enabled address assigned to the MC68183, an address packet will be sent to the host processor. The address packet contains assorted data about the address and its associated vector and message. The ID of an address packet is 1 (decimal). See Table D-3 for bit assignments.

Table D-3. Address Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	0	0	0	0	0	0	1
Byte 2	PA	p_1	p_0	LA	x	x	x	x
Byte 1	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0
Byte 0	TOA	WN_6	WN_5	WN_4	WN_3	WN_2	WN_1	WN_0

PA: Priority Address. Set if the address was received as a priority address.

p: Phase on which the address was detected (0=a, 1=b, 2=c, 3=d)

LA: Long Address type. Set if the address was programmed in the MC68183 as a long address.

AI: Address Index (valid values are 0 through 15 and 128 through 159). The index identifies which of the addresses was detected. Values 0 through 15 correspond to the 16 programmable address words. Values 128 through 143 correspond to the 16 temporary addresses. Values 144 through 159 correspond to the 16 operator messaging addresses. For long addresses, the address detect packet will only be sent once and the index will refer to the second word of the address.

TOA: Tone Only Address. Set if the address was programmed in the MC68183 as a tone-only address. This bit will never be set for temporary or operator messaging addresses. No vector word will be sent for tone-only addresses.

WN: Word number of vector (2 - 87). Describes the location in the frame of the vector word for the detected address. This value is invalid for this packet if the TOA bit is set.

x: Unused bits. The value of these bits is not guaranteed.

D.3 Vector Packet

The vector field follows the address field in the FLEX protocol. Each vector packet must be matched to its corresponding address packet. The ID of the vector packet is the word number where the vector word was received in the frame. This value corresponds to the WN bits sent in the associated address packet. The phase information in both the address packet and the vector packet must also match.

It is important to note that for long addresses, the first message word will be transmitted in the word location immediately following the associated vector. See Section E.3, “Message Building,” for a message-building example. In this case, the word number (identified by b_6 to b_0) in the vector packet will indicate the message start of the second message word if the message is longer than 1 word.

There are several types of vectors: three types of numeric vectors, a short message/tone-only vector, a hex/binary vector, an alphanumeric vector, a secure message vector, and a short instruction vector. Each is described in the following pages. Two of the modes of the short instruction vector is used for assigning temporary addresses that may be associated with a group call.

The numeric, hex/binary, alphanumeric, and secure message vector packets have associated message word packets in the message field. The host must use the n and b bits of the vector word to calculate what message word locations are associated with the vector. The message word locations and the phase must match.

Four of the vectors (hex/binary, alphanumeric, secure message, and the temporary address assignment modes of the short instruction) enable the MC68183 to begin the all frame mode. This mode is required to allow for the decoding of temporary addresses and / or fragmented messages. The host disables the all frame mode after the proper time by writing to the decoder via the all frame mode packet. See Section E.4, “Building a Fragmented Message,” and Section E.5, “Operation of a Temporary Address,” for more information.

For any address packet sent to the host (except tone-only addresses), a corresponding vector packet will always be sent. If more than two bit errors are detected in the vector word (via BCH calculations, parity calculations, check character calculations, or value validation) the e bit will be set and the message words will not be sent.

D.3.1 Numeric Vector Packet

Refer to Table D-4 for bit assignments and to Table D-5 for vector type identifiers.

Table D-4. Numeric Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN ₆	WN ₅	WN ₄	WN ₃	WN ₂	WN ₁	WN ₀
Byte 2	e	p ₁	p ₀	x	x	V ₂	V ₁	V ₀
Byte 1	x	x	K ₃	K ₂	K ₁	K ₀	n ₂	n ₁
Byte 0	n ₀	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	b ₀

V: Vector type identifier. See Table D-5 for names and descriptions of the vector identifiers.

Table D-5. Vector Type Identifiers

$V_2V_1V_0$	Name	Description
011	Standard numeric vector	No special formatting of characters is specified
100	Special format numeric vector	Formatting of the received characters is predetermined by special rules in the host.
111	Numbered numeric vector	The received information has been numbered by the service provider to indicate all messages have been properly received

WN: Word number of vector (2 - 87 decimal). Describes the location of the vector word in the frame.

e: Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.

p: Phase on which the vector was found (0=a, 1=b, 2=c, 3=d)

K: Beginning check bits of the message.

n: Number of message words in the message including the second vector word for long addresses (000 = 1 word message, 001 = 2 word message, etc.). For long addresses, the first message word is located in the word location that immediately follows the associated vector.

b: Word number of message start in the message field (3-87 decimal). For long addresses, the word number indicates the location of the second message word.

x: Unused bits. The value of these bits is not guaranteed.

D.3.2 Short Message / Tone-Only Vector

Refer to Table D-6 for bit assignments.

Table D-6. Short Message / Tone-Only Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN ₆	WN ₅	WN ₄	WN ₃	WN ₂	WN ₁	WN ₀
Byte 2	e	p ₁	p ₀	x	x	V ₂	V ₁	V ₀
Byte 1	x	x	d ₁₁	d ₁₀	d ₉	d ₈	d ₇	d ₆
Byte 0	d ₅	d ₄	d ₃	d ₂	d ₁	d ₀	t ₁	t ₀

V: 010 for a short message/tone-only vector.

WN: Word number of vector (2 - 87 decimal). Describes the location of the vector word in the frame.

e: Set if more than 2 bit errors are detected in the word or, if after error correction, the check character calculation fails.

- p: Phase on which the vector was found (0=a, 1=b, 2=c, 3=d)
- d: Data bits whose definition depend on the value of t in this packet in accordance with Table D-7. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder will send a message packet from the word location immediately following the vector packet. Except for the short message on a non-network address (t=0), all message bits in the message packet are unused and should be ignored.

Table D-7. Data Bits Defined by Value of t

t ₁ t ₀	d ₁₁ d ₁₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	Description
00	c ₃ c ₂ c ₁ c ₀ b ₃ b ₂ b ₁ b ₀ a ₃ a ₂ a ₁ a ₀	Short numeric: 3 numeric chars ¹ when on a messaging address
00	T ₃ T ₂ T ₁ T ₀ M ₂ M ₁ M ₀ A ₄ A ₃ A ₂ A ₁ A ₀	Part of NID when on a network address
01	s ₈ s ₇ s ₆ s ₅ s ₄ s ₃ s ₂ s ₁ s ₀ S ₂ S ₁ S ₀	Tone only: 8 sources (S) and 9 unused bits (s)
10	s ₁ s ₀ R ₀ N ₅ N ₄ N ₃ N ₂ N ₁ N ₀ S ₂ S ₁ S ₀	Tone only: 8 sources (S), message number (N), message retrieval flag (R), and 2 unused bits (s)
11		Spare message type

1. For long addresses, an extra 5 characters are sent in the Message Packet immediately following the Vector Packet.

- t: Message type. These bits define the meaning of the d bits in this packet.
- x: Unused bits. The value of these bits is not guaranteed.

D.3.3 HEX / Binary, Alphanumeric, and Secure Message Vector

Refer to Table D-8 for bit assignments.

Table D-8. HEX / Binary, Alphanumeric, and Secure Message Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN ₆	WN ₅	WN ₄	WN ₃	WN ₂	WN ₁	WN ₀
Byte 2	e	p ₁	p ₀	x	x	V ₂	V ₁	V ₀
Byte 1	x	x	n ₆	n ₅	n ₄	n ₃	n ₂	n ₁
Byte 0	n ₀	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	b ₀

V: Vector type identifier. See Table D-9.

Table D-9. Vector Type Identifiers

$V_2V_1V_0$	Type
000	Secure
101	Alphanumeric
110	Hex / Binary

- WN:** Word number of vector (2 - 87 decimal). Describes the location of the vector word in the frame.
- e:** Set if more than 2 bit errors are detected in the word, if the check character calculation fails after error correction has been performed, or if the vector value is determined to be invalid.
- p:** Phase on which the vector was found (0=a, 1=b, 2=c, 3=d)
- n:** Number of message words in this frame including the first message word that immediately follows a long address vector. Valid values are 1 through 85 decimal.
- b:** Word number of message start in the message field. Valid values are 3 through 87 decimal.
- x:** Unused bits. The value of these bits is not guaranteed.

Note: For long addresses, the first message packet is sent from the word location immediately following the word location of the vector packet. The b bits indicate the second message word in the message field if one exists.

D.3.4 Short Instruction Vector

Refer to Table D-10 for bit assignments.

Table D-10. Short Instruction Vector Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN ₆	WN ₅	WN ₄	WN ₃	WN ₂	WN ₁	WN ₀
Byte 2	e	p ₁	p ₀	x	x	V ₂	V ₁	V ₀
Byte 1	x	x	d ₁₀	d ₉	d ₈	d ₇	d ₆	d ₅
Byte 0	d ₄	d ₃	d ₂	d ₁	d ₀	i ₂	i ₁	i ₀

- V:** 001 for a short instruction vector.
- WN:** Word number of vector (2 - 87 decimal). Describes the location of the vector word in the frame.
- e:** Set if more than 2 bit errors are detected in the word or, if after error correction, the check character calculation fails.
- p:** Phase on which the vector was found (0=a, 1=b, 2=c, 3=d)

- d: Data bits whose definition depend on the i bits in this packet in according with Table D-11. Note that if this vector is received on a long address and the e bit in this packet is not set, the decoder will send a message packet immediately following the vector packet. All message bits in the message packet are unused and should be ignored for all modes except the temporary address assignment with MSN ($i_2i_1i_0=010$).

Table D-11. Data Bits with Definition Dependent on i Bit

$i_2i_1i_0$	$d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$	Description
000	$a_3 a_2 a_1 a_0 f_6 f_5 f_4 f_3 f_2 f_1 f_0$	Temporary address assignment ¹
001	$d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$	11 event flags for system event
010	$a_3 a_2 a_1 a_0 f_6 N_5 N_4 N_3 N_2 N_1 N_0$	Temporary address assignment with MSN ²
011	—	Reserved
100	—	Reserved
101	—	Reserved
110	—	Reserved
111	—	Reserved for test

1. Assigned temporary address (a) and assigned frame (f). See Section E.5, “Operation of a Temporary Address,” for a description of the use of these fields.
2. Assigned temporary address (a), MSb of assigned frame (f_6), and message sequence number (N). The message packet sent with this instruction on long addresses contains extra frame information, see Section E.5, “Operation of a Temporary Address,” for a description and for details on the use of the other fields.

- i: Instruction type. These bits define the meaning of the d bits in this packet.
- x: Unused bits. The value of these bits is not guaranteed.

D.4 Message Packet

The message field follows the vector field in the FLEX protocol. It contains the message data, checksum information, and may contain fragment numbers and message numbers.

If the error bit of a vector word is not set and the vector word indicates that there are message words associated with the page, the message words are sent in message packets. Refer to Table D-12 for bit assignments.

The ID of the message packet is the word number where the message word was received in the frame.

Table D-12. Message Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	WN6	WN5	WN4	WN3	WN2	WN1	WN0
Byte 2	e	p_1	p_0	i_{20}	i_{19}	i_{18}	i_{17}	i_{16}

Table D-12. Message Packet Bit Assignments (Continued)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1	i ₁₅	i ₁₄	i ₁₃	i ₁₂	i ₁₁	i ₁₀	i ₉	i ₈
Byte 0	i ₇	i ₆	i ₅	i ₄	i ₃	i ₂	i ₁	i ₀

WN: Word number of message word (3 - 87 decimal). Describes the location of the message word in the frame.

e: Set if more than two bit errors are detected in the word.

p: Phase on which the message word was found (0=a, 1=b, 2=c, 3=d)

i: These are the information bits of the message word. The definitions of these bits depend on the vector type and which word of the message is being received.

D.5 Roaming Status Packet

The MC68183 will automatically prompt the host to read a roaming status packet if RSR, MS1, MFI, MS2, MBI, MAW, NBU, NDR₁, NDR₀, or SCU is set. Refer to Table D-13 for bit assignments.

Table D-13. Roaming Status Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	0	0	0	0	0
Byte 2	RSR	MS1	MFI	MS2	MBI	MAW	NBU	n
Byte 1	x	x	x	x	x	x	NDR ₁	NDR ₀
Byte 0	x	x	x	x	SCU	RSC ₂	RSC ₁	RSC ₀

RSR: Resynchronization Signal Received. RSR is set when the FLEXchip detected a resynchronization signal and the host configured FLEXchip to ignore it via the IRS bit in the roaming control packet. RSR is cleared when read.

MS1: Missed Synchronization 1. MS1 is set when the FLEXchip failed to detect the first synchronization pattern (A/\bar{A}) of a FLEX frame and FLEXchip was configured to report missed frame information via the MFC bit in the roaming control packet. MS1 is cleared when read.

MFI: Missed Frame Information word. MFI is set when the frame information word is received with an uncorrectable number of errors and FLEXchip was configured to report missed frame information via the MFC bit in the roaming control packet. MFI is cleared when read.

MS2: Missed Synchronization 2. MS2 is set when the FLEXchip failed to detect the second synchronization pattern (C/\bar{C}) of a frame and FLEXchip was configured to report missed frame information via the MFC bit in the roaming control packet. MS2 is cleared when read.

- MBI:** Missed Block Information word 1. MBI is set when at least one of the block information word ones is received with an uncorrectable number of errors and FLEXchip was configured to report missed frame information via the MFC bit in the roaming control packet. MBI is set no more than once per frame regardless of the number of missed block information word 1's in the frame. MBI is cleared when read.
- MAW:** Missed Address Word. MAW is set when any address words in the address field is received with an uncorrectable number of errors and FLEXchip was configured to report missed frame information via the MFC bit in the roaming control packet. This bit is set no more than once per frame, regardless of the number of missed address words in the frame. MAW is cleared when read.
- NBU:** Network Bit Update. NBU is set when the NBC bit in the roaming control packet is set and a frame information word is received with a correctable number of errors. NBU will not be set when the frame information word is not received due to missing the first synchronization pattern (A/A). NBU is cleared when read.
- n:** Network bit value. When NBU is set, this is the value of the n bit in the last received frame information word.
- NDR:** Noise Detect Result. The NDR bits indicate the result of a noise detect. The results of noise-detects initiated by setting the SND bit in the roaming control packet will always be reported. The results of the automatic noise-detects performed in asynchronous mode will only be reported if the RND bit is set in the roaming control packet. When continuous noise-detects during block data are enabled by setting the CND bit in the roaming control packet, only the "No FLEX signal detected" result will be reported. The NDR bits are cleared when read. Refer to Table D-14.

Table D-14. Noise Detect Result

NDR	Noise Detect Result
00	No information
01	Noise detect was abandoned
10	FLEX signal detected
11	FLEX signal not detected

- SCU:** System Collapse Update. SCU is set when the MC68183 is configured for manual collapse mode by setting the MCM bit in the roaming control packet and the system collapse of a frame is received. SCU is set no more than once per frame, regardless of the number of phases in the frame. SCU will not be set in frames in which no block information word ones is received properly. SCU is cleared when read.
- RSC:** Received System Collapse. When SCU is set, this value represents the system collapse value that was received in the frame.

D.6 Receiver Shut-Down Packet

The shutdown packet is sent in both synchronous and asynchronous mode. It is designed to indicate to the host that the receiver is turned off and how much time there is until the FLEXchip will automatically turn it back on. Refer to Table D-15 for bit assignments.

Table D-15. Receiver Shut-Down Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	1	1	1	1	0
Byte 2	FNV	CF ₆	CF ₅	CF ₄	CF ₃	CF ₂	CF ₁	CF ₀
Byte 1	TNF ₇	TNF ₆	TNF ₅	TNF ₄	TNF ₃	TNF ₂	TNF ₁	TNF ₀
Byte 0	FCO	NAF ₆	NAF ₅	NAF ₄	NAF ₃	NAF ₂	NAF ₁	NAF ₀

FNV: Frame Number Valid. This bit is set if the last decoded frame info word was correctable and the frame number was the expected value. When in asynchronous mode, this value will be 0.

CF: Current Frame. When in synchronous mode, CF is the current frame number. This value is latched on the negative edge of the $\overline{\text{READY}}$ line when this packet is sent to the host. The value of this field is valid only if the MC68183 is in synchronous mode and the FIV bit in the status packet is set. When in asynchronous mode, this value will be 0.

TNF: Time to Next Frame. When in synchronous mode, TNF indicates the time there would be to the start of the A-word check if the MC68183 were to warm up for the next frame. When in asynchronous mode, TNF indicates the time to the start of the next automatic noise detect. See Section E.6, “Using the Receiver Shut-Down Packet,” for an explanation of how to use this value. This value is latched on the negative edge of the $\overline{\text{READY}}$ line when this packet is sent to the host.

FCO: Frame Carried On. Set if the MC68183 is decoding the next frame due to the reception of a non-zero carry-on value in the current or a previous frame. When in asynchronous mode, this value will be 0.

NAF: Next Assigned Frame. This is the frame number of the next frame the MC68183 was scheduled to decode when the receiver shut down. The value of this field is valid only if the MC68183 is in synchronous mode and the FIV bit in the status packet is set. When in asynchronous mode, this value will be 0.

D.7 Status Packet

The status packet contains various types of information that the host may require. The status packet will be sent to the host whenever the MC68183 is polled and has no other data to send. The MC68183 can also prompt the host to read the status packet due to events for which the MC68183 was configured to send it. Refer to Table D-16 for bit assignments. (See Section C.3, “Control Packet,” for a detailed description of the bits.) The MC68183 will prompt the host to read a status packet if any of the following holds true.

- SMU bit in the status packet and the SME bit in the configuration packet are set.
- MT bit in the status packet and the MTE bit in the configuration packet are set.
- EOF bit in the status packet is set.
- LBU bit in the status packet is set.
- EA bit in the status packet is set.
- BOE bit in the status packet is set.

- The ID of the status packet is 127 (decimal).

Table D-16. Status Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	0	1	1	1	1	1	1	1
Byte 2	FIV	f ₆	f ₅	f ₄	f ₃	f ₂	f ₁	f ₀
Byte 1	SM	LB	x	x	c ₃	c ₂	c ₁	c ₀
Byte 0	SMU	LBU	x	MT	x	EOF	EA	BOE

FIV: Frame Info Valid. Set when a valid frame info word has been received since becoming synchronous to the system, and the f and c fields contain valid values. If FIV is clear, no valid frame info words have been received since the MC68183 became synchronous to the system.

This value will change from 0 to 1 at the end of block 0 of the frame in which the first frame info word was properly received. It will be cleared when the MC68183 goes into asynchronous mode. FIV is initialized to 0 when the MC68183 is reset and when the MC68183 is turned off by clearing the ON bit in the control packet.

f: Current frame number. This value is updated every frame, regardless of whether the MC68183 needs to decode the frame. This value will change to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SM: Synchronous Mode. SM is set when the MC68183 is synchronous to the system. The MC68183 will set SM when the first synchronization words are received. It will clear SM when the MC68183 has not properly received both synchronization words in any frame for 8, 16, or 32 minutes (depending on the number of assigned frames and the system collapse). SM is initialized to 0 when the MC68183 is reset and when it is turned off by clearing the ON bit in the control packet.

LB: Low Battery. LB is set to the value last read from the LOBAT pin. The host controls when the LOBAT pin is read via the receiver control packets. LB is initialized to 0 at reset. It is also initialized to the inverse of the LBP bit in the configuration packet when the MC68183 is turned on by setting the ON bit in the control packet.

c: Current system cycle number. This value is updated every frame regardless of whether the MC68183 needs to decode the frame. This value will change to its proper value for a frame at the end of block 0 of the frame. The value of these bits is not guaranteed when FIV is 0.

SMU: Synchronous Mode Update. SMU is set if the SM bit has been updated in this packet. When the MC68183 is turned on, SMU will be set when the first synchronization words are found (SM changes to 1) or when the first synchronization search window after the MC68183 is turned on expires (SM stays 0).

The latter condition gives the host the option of assuming the paging device is in range when it is turned on, and displaying out-of-range only after the initial A search window expires. After the initial synchronous mode update, the SMU bit will be set whenever the MC68183 transitions from/to synchronous mode. Cleared when read. Changes in the SM bit due to

turning off the MC68183 will not cause SMU to be set. SMU is initialized to 0 when the MC68183 is reset.

- LBU:** Low Battery Update. LBU is set if the value on two consecutive reads of the LOBAT pin yielded different results and is cleared when read. The host controls when the LOBAT pin is read via the receiver control packets. Changes in the LB bit due to turning on the MC68183 will not cause LBU to be set. LBU is initialized to 0 when the MC68183 is reset.
- MT:** Minute Time-out. MT is set if 1 minute has elapsed and cleared when read. MT is initialized to 0 when the MC68183 is reset.
- EOF:** End Of Frame. EOF is set when the MC68183 is in all frames mode and the end of frame has been reached. The MC68183 is in all frames mode if the all frames mode enable counter is non-zero, if any temporary address enabled counter is non-zero, or if the FAF bit in the all frame mode packet is set. Cleared when read. EOF is initialized to 0 when the MC68183 is reset.
- EA:** End of Addresses. If EAE of the control packet is set and an address is detected in a frame, EA will be set after FLEXchip processes the last address in the frame. Because data packets take priority over the status packet, the status packet with the EA bit set is guaranteed to come after all address packets for the frame. EA is cleared when read. EA is initialized to 0 when the MC68183 is reset.
- BOE:** Buffer Overflow Error. Set when information has been lost due to slow host-response time. When the data packet FIFO transmit buffer on the MC68183 overflows, the MC68183 clears the buffer, turns off decoding by clearing the ON bit in the control packet, and sets this bit. BOE is cleared when read. This bit is initialized to 0 when the MC68183 is reset.
- x:** Unused bits. The value of these bits is not guaranteed.

D.8 Part ID Packet

The part ID packet is sent by the MC68183 whenever the MC68183 is disabled due to the checksum feature. See Section C.1, “Checksum Packet,” for a description of the checksum feature. Since the MC68183 is disabled after reset, the part ID is the first packet the host will receive after reset. The ID of the part ID packet is 255 (decimal). Table D-17 gives bit assignments for the part ID packet.

Table D-17. Part ID Packet Bit Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	1	1	1	1	1	1	1	1
Byte 2	MDL ₁	MDL ₀	CID ₁₃	CID ₁₂	CID ₁₁	CID ₁₀	CID ₉	CID ₈
Byte 1	CID ₇	CID ₆	CID ₅	CID ₄	CID ₃	CID ₂	CID ₁	CID ₀
Byte 0	REV ₇	REV ₆	REV ₅	REV ₄	REV ₃	REV ₂	REV ₁	REV ₀

MDL: Model. MDL identifies the FLEXchip model. Current value is 0.

CID: Compatibility ID. This value describes the FLEXchips to which this part is backwards-compatible. See Table D-18 for meaning and current value.

Table D-18. CID Meaning and Current Value

Bit	Indicates this IC Can Be Used in Place Of	Value for MC68183
CID ₀	FLEXchip ¹	1 (TRUE)
CID ₁	MC68183 ²	1 (TRUE)
CID ₂	Numeric FLEXchip	0 (FALSE)

1. Compatibility to MC68183 is indicated by MDL set to 0, CID₀ set to 1, and REV greater than or equal to 7.

2. Compatibility to MC68183 is indicated by MDL set to 0, CID₁ set to 1, and REV greater than or equal to 8.

REV: Revision. REV identifies the revision and manufacturer of the FLEXchip. Table D-19 lists the currently available part IDs of the FLEXchip family.

Table D-19. FLEXchip Revisions and Manufacturers

Part ID Packet (Hexadecimal)	Revision	Manufacturer
00 01 03	FLEXchip	Texas Instruments
00 01 04	FLEXchip	Motorola Semiconductor Products Sector
00 01 06	FLEXchip	Philips
00 01 07	FLEXchip II	Motorola Semiconductor Products Sector
00 01 08	FLEXchip II	Texas Instruments
00 03 03	Roaming FLEXchip	Motorola Semiconductor Products Sector
00 03 05	Roaming FLEXchip	Texas Instruments
00 03 09	Roaming FLEXchip II	Motorola Semiconductor Products Sector
00 03 0A	Roaming FLEXchip II	Texas Instruments
00 04 01	Numeric FLEXchip	Texas Instruments

Appendix E Application Notes

E.1 Receiver Control

The MC68183 has eight programmable receiver control lines (S0-S7). The host has control of the receiver warm-up and shut-down timing as well as all various settings on the control lines through configuration registers on the MC68183. The configuration registers for most settings allow the host to configure what setting is applied to the control lines, how long to apply the setting, and if the LOBAT input pin is polled before changing from the setting. With this programmability, the FLEXchip II IC should be able to interface with many off-the-shelf receiver ICs.

When using the internal demodulator (i.e., when the IDE bit of the configuration packet is set), the S0 pin becomes the input for the demodulator and the S0 register setting in the receiver control configuration packets controls the tracking mode of the peak and valley detectors for the internal data slicer. When the S0 bit is set in a receiver setting, the internal data slicer will be in fast track mode. When the S0 bit is cleared in a receiver setting, the internal data slicer will be in slow track mode. For details on the configuration of the receiver control settings, see Section C.9, “Receiver Control Configuration Packets.”

E.2 Receiver Settings at Reset

The receiver control ports are three-state outputs which are set to the high-impedance state when the MC68183 is reset and until the corresponding FRS bit in the receiver line control packet is set or until the MC68183 is turned on by setting the ON bit in the control packet. This allows the designer to force the receiver control lines to the receiver off setting with external pull-up or pull-down resistors before the host can configure these settings in the MC68183. When the MC68183 is turned on, the receiver control ports are driven to the settings configured by the Section C.9, “Receiver Control Configuration Packets,” until the MC68183 is reset again.

E.2.1 Automatic Receiver Warm-Up Sequence

The MC68183 allows for up to six steps associated with warming up the receiver. When the MC68183 automatically turns on the receiver, it starts the warm-up sequence 160 ms before it requires valid signals at the EXTS0 and EXTS1 input pins (or the equivalent internal signals when using the internal demodulator/data slicer). The first step of the warm-up sequence involves leaving the receiver control lines in the “off” state for the amount of time programmed for “warm-up off-time.”

At the end of the “warm-up off-time,” the first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting. Each subsequent warm-up setting is applied to the receiver control lines for their corresponding time until a disabled warm-up setting is found.

At the end of the last used warm-up setting, the “1600sps sync setting” or the “3200sps sync setting” is applied to the receiver control lines depending on the current state of the MC68183. The sum total of all of the used warm-up times and the “warm-up off time” must not exceed 160ms. If it exceeds 160ms, the MC68183 will execute the receiver shut-down sequence at the end of the 160ms warm-up period. Figure E-1 shows the receiver warm-up sequence while decoding when all warm-up settings are enabled.

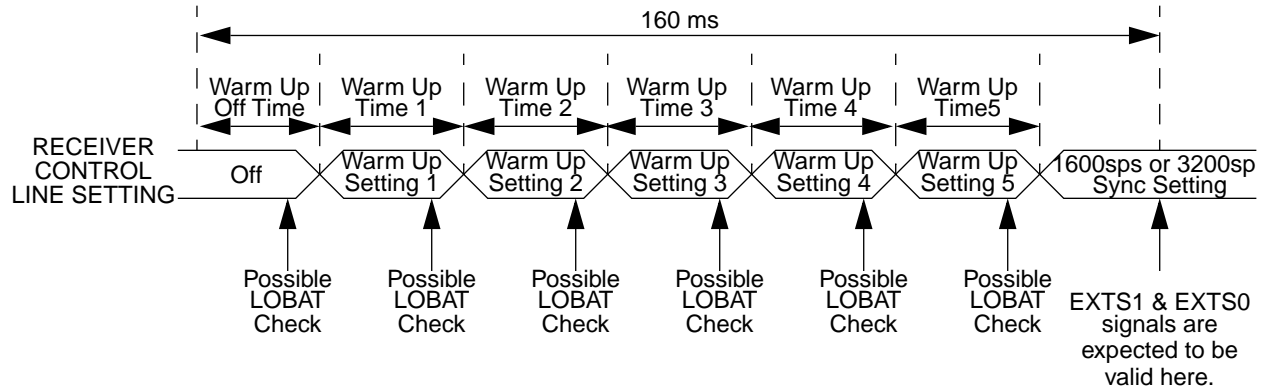


Figure E-1. Automatic Receiver Warm-Up Sequence

E.2.2 Host-Initiated Receiver Warm-Up Sequence

The host can cause the MC68183 to warm up the receiver in three ways: by setting the ON bit in the control packet to turn on the FLEXchip; by requesting a noise-detect by setting the SND bit in the roaming control packet; or by setting the SAS bit in the roaming control packet to requesting an A-word search. When the MC68183 warms up the receiver in response to a host request, the first warm-up setting, if enabled, is applied to the receiver control lines for the amount of time programmed for that setting. Each subsequent warm-up setting is applied to the receiver control lines for the corresponding time until a disabled warm-up setting is found.

Once a disabled warm-up setting is found, the “3200sps sync setting” (for ON and SND warm-ups) or the “1600sps sync setting” (for SAS warm-ups) is applied to the receiver control lines. The decoder does not expect a valid signal until after the “3200sps sync warm-up time” (for ON, SND, and SAS warm ups) has expired. Figure E-2 shows the receiver warm-up sequence when the host initiates a warm-up sequence and when all warm-up settings are enabled.

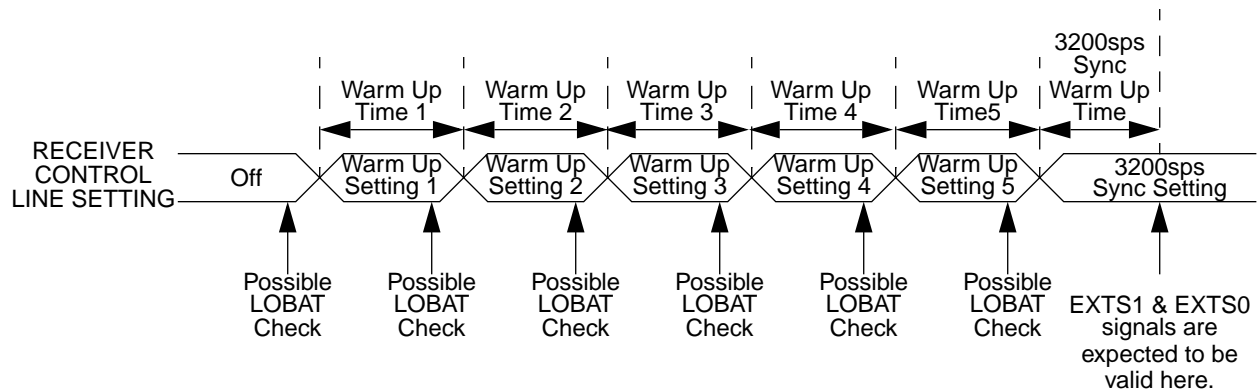


Figure E-2. Host-Initiated Receiver Warm-Up Sequence

E.2.3 Receiver Shut-Down Sequence

The MC68183 allows for up to three steps associated with shutting down the receiver. When the MC68183 decides to turn off the receiver, the first shut-down setting, if enabled, is applied to the receiver control lines for the corresponding shut-down time. At the end of the last used shut-down

time, the “off” setting is applied to the receiver control lines. If the first shut-down setting is not enabled, the MC68183 will transition directly from the current on setting to the “off” setting. The receiver turn-off sequence when all shut-down settings are enabled is shown in Figure E-3.

If the receiver is on or being warmed up when the decoder is turned off (by clearing the ON bit in the control packet), the MC68183 will execute the receiver shut -down sequence. If the MC68183 is executing the shut-down sequence when the MC68183 is turned on (by setting the ON bit in the Control Packet), the MC68183 will complete the shut-down sequence before starting the warm-up sequence.

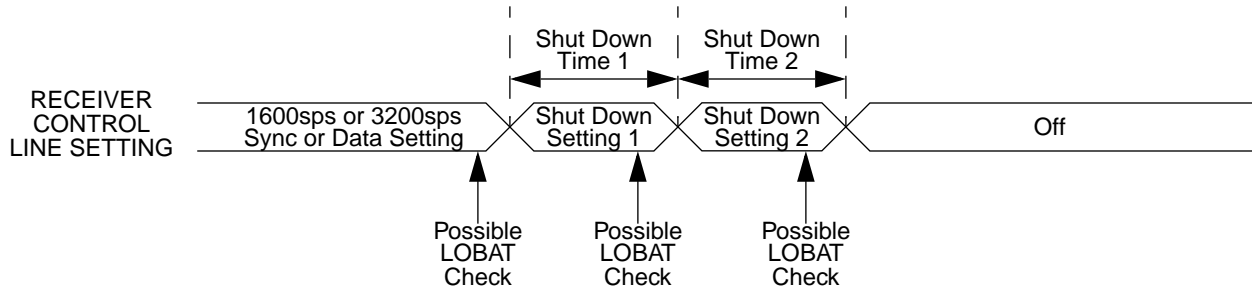


Figure E-3. Receiver Shut-Down Sequence

E.2.4 Miscellaneous Receiver States

In addition to the warm-up and shut-down states, the MC68183 has four other receiver states. When these settings are applied to the receiver control lines, the MC68183 will be decoding the EXT_{S1} and EXT_{S0} input signals (or the equivalent internal signals when using the internal demodulator/data slicer). The timing of these signals and their duration depends on the data the MC68183 decodes. The four settings are as follows:

- 1600sps Sync Setting: applied when the MC68183 is searching for a 1600 symbols per second signal.
- 3200sps Sync Setting: applied when the MC68183 is searching for a 3200 symbols per second signal.
- 1600sps Data Setting: applied after the MC68183 has found the C or \bar{C} sync word in a 1600 symbols per second frame.
- 3200sps Data Setting: applied after the MC68183 has found the C or \bar{C} sync word in a 3200 symbols per second frame.

Some examples of how these settings will be used in the MC68183 are shown in Figure E-4.

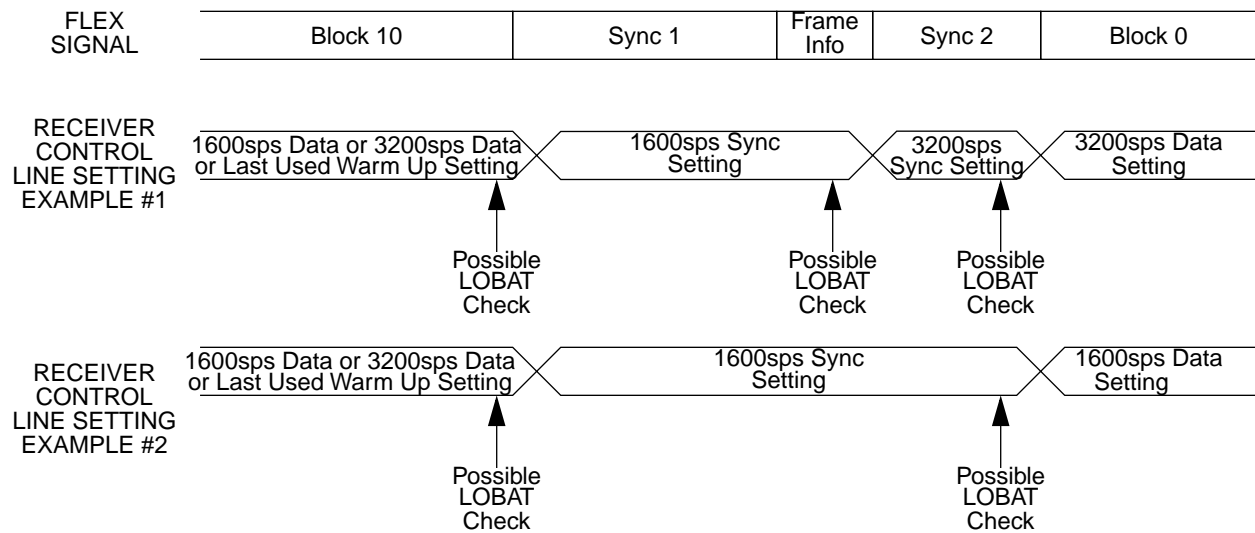


Figure E-4. Examples of Receiver Control Transitions

E.2.5 Low-Battery Detection

The MC68183 can be configured to poll the LOBAT input pin at the end of every receiver control setting. This check can be enabled or disabled for each receiver control setting. If the poll is enabled for a setting, the pin will be read just before the MC68183 changes the receiver control lines from that setting to another setting. The MC68183 will send a status packet whenever the value on two consecutive reads of the LOBAT pin yields different results.

E.3 Message Building

A simple message consists of an address packet followed by a vector packet indicating the word numbers of associated message packets. The tables below show a more complex example of receiving three messages and two block information word packets in the first two blocks of a 2-phase, 3200 bps, FLEX frame. Note that the messages shown may be portions of fragmented or group messages. Note further that in the case of a 6400 bps FLEX signal, there would be four phases: A, B, C and D, and in the case of a 1600 bps signal there would be only a single phase A.

Table E-1 shows the block number, word number (WN), and word content of both phases A and C. Contents of words not meant to be received by the host are left blank. Each phase begins with a block information word (WN 0) which is not sent to the host. The first message is in phase A and has an address (WN 3), vector (WN 7), and three message words (WN 9 - 11). The second message is also in phase A and has an address (WN 4), a vector (WN 8), and four message words (WN 12 - 15). The third message is in phase C and has a two-word-long address (WN 5 - 6) followed by a vector (WN 10) and three message words. Because the third message is sent on a long address, the first message word (WN 11) begins immediately after the vector. The vector indicates the location of the second and third message words (WN 14 - 15). Refer to Table E-1 for more information.

Table E-1. FLEX Signal

BLOCK	Word Number	PHASE A	PHASE C
0	0	BIW1	BIW1
	1		BIW
	3	ADDRESS 1	BIW
	4	ADDRESS 2	
	5		LONG ADDRESS 3 WORD 1
	6		LONG ADDRESS 3 WORD 2
	7	VECTOR 1	
1	8	VECTOR 2	
	9	MESSAGE 1,1	
	10	MESSAGE 1,2	VECTOR 3
	11	MESSAGE 1,3	MESSAGE 3,1
	12	MESSAGE 2,1	
	13	MESSAGE 2,2	
	14	MESSAGE 2,3	MESSAGE 3,2
	15	MESSAGE 2,4	MESSAGE 3,3

Table E-2 shows the sequence of packets received by the host. The FLEXchip processes the FLEX signal one block and phase at a time. Thus, the address and vector information in block 0 phase A is sent to the host in packets 1–3. Then information in block 0 phase C (two block information words and one long address) is sent to the host in packets 4–6. Packets 7–18 correspond to information in block 1 and are processed in phase A first and phase C second.

Table E-2. FLEXchip Packet Sequence

Packet	Packet Type	Phase	Word Number	Comment
1st	ADDRESS	A	N.A. (7)	Address 1 has a vector located at WN 7
2nd	ADDRESS	A	N.A. (8)	Address 2 has a vector located at WN 8
3rd	VECTOR	A	7	Vector for Address 1: Message Words located at WN = 9 to 11, phase A
4th	BIW	C	N.A.	If BIWs enabled, then BIW packet sent
5th	BIW	C	N.A.	If BIWs enabled, then BIW packet sent

Table E-2. FLEXchip Packet Sequence (Continued)

Packet	Packet Type	Phase	Word Number	Comment
6th	LONG ADDRESS	C	N.A. (10)	Long address 3 has a vector beginning in word 10 of phase C
7th	VECTOR	A	8	Vector for address 2: message words located at WN = 12 to 15, phase A
8th	MESSAGE	A	9	Message information for address 1
9th	MESSAGE	A	10	Message information for address 1
10th	MESSAGE	A	11	Message information for address 1
11th	MESSAGE	A	12	Message information for address 2
12th	MESSAGE	A	13	Message information for address 2
13th	MESSAGE	A	14	Message information for address 2
14th	MESSAGE	A	15	Message information for address 2
15th	VECTOR	C	10	Vector for long address 3: message words located at WN = 14 - 15, phase C
16th	MESSAGE	C	11	Second word of long vector is first message information word of address 3
17th	MESSAGE	C	14	Message information for address 3
18th	MESSAGE	C	15	Message information for address 3

The first message is built by relating packets 1, 3, and 8–10. The second message is built by relating packets 2, 7 and 11–14. The third message is built by relating packets 6 and 15–18. Additionally, the host may process block information in packets 4 and 5 for time-setting information.

E.4 Building a Fragmented Message

The longest message that will fit into a frame is 84 code-words total of message data. Three alpha characters per word yields a maximum message of 252 characters in a frame, assuming no other traffic. Messages longer than this value must be sent as several fragments.

Additional fragments can be expected when the “continue bit” in the first message word is set. This causes the pager to examine every following frame for an additional fragment until the last fragment with the continue bit reset is found. The only requirement relating to the placement in time of the remaining fragments is that no more than 32 frames (1 minute) or 128 frames (4 minutes)—as indicated by the service provider—may pass between fragment receptions.

Each fragment contains a check sum character to detect errors in the fragment: a fragment number 0, 1, or 2 to detect missing fragments, a message number to identify which message the fragment is a part, and the continue bit that indicates either that more fragments are in queue or that the last fragment has been received.

The following describes the sequence of events between the host and the MC68183 required to handle a fragmented message. First, the host will receive a vector indicating one of the types shown in Table E-3.

Table E-3. Host Vector Indications

$V_2V_1V_0$	Type
000	Secure
101	Alphanumeric
110	Hex / Binary

- The MC68183 will increment the all frame mode counter inside the MC68183 and begin to decode all of the following frames.
- The host will receive the message packet(s) contained within that frame followed by a status packet. The host must decide based on the message packet to return to normal decoding operation.

If the message is indicated as fragmented by the message continued flag “C” being set in the message packet then the host does not decrement the all frame mode counter at this time. The host decrements the counter if the message continued flag “C” is clear by writing the all frame mode packet to the MC68183 with the “DAF” bit = 1. If no other fragments or temporary addresses are pending and the FAF bit is clear in the all frame mode register, the MC68183 returns to normal operation.

- The MC68183 continues to decode all frames and passes any address information, vector information, and message information to the host, followed by a status packet indicating the end of the frame. If the message is indicated as fragmented by the message continued flag “C” in the message packet, the host remains in the receive mode expecting more information from the MC68183.
- After the host receives the second and subsequent fragment with the message continued flag “C” = 1, it should decrement the all frame mode counter by sending an all frame mode packet to the MC68183 with the “DAF” bit = 1. Alternately, the host may choose to decrement the counter at the end of the entire message by decrementing the counter once for each fragment received.
- When the host receives a message packet with the message continued flag “C” = 0, the host will send two all frame mode packets to the MC68183 with the “DAF” bit = 1. The two packets decrement the count for the first and last fragment. This decrements the all frame counter to zero. If no other fragmented messages or temporary addresses are pending, and if the FAF bit is clear in the all frame mode register, the MC68183 returns to normal operation.
- The above process must be repeated for each occurrence of a fragmented message. The host must keep track of the number of fragmented messages being decoded and insure the all frame mode counter decrements after each fragment or after each fragmented message. Refer to Table E-4 and Table E-5 for more information on fragmented and unfragmented alphanumeric messages.

Table E-4. Alphanumeric Message without Fragmentation

Packet	Packet Type	Phase	All Frame Counter	Comment
1st	ADDRESS 1	A	0	Address 1 is received
2nd	VECTOR 1	A	1	Vector = alphanumeric type
3rd	MESSAGE	A	1	Message word received "C" bit = 0, no more fragments are expected.
4th	Variable ¹		0	Host writes all frame mode packet to the MC68183 with the "DAF" bit = 1

1. Host-initiated packet. The MC68183 returns a packet as described in Appendix D, "Decoder-to-Host Packet Descriptions."

Table E-5. Alphanumeric Message with fragmentation

Packet	Packet Type	Phase	All Frame Counter	Comment
1st	ADDRESS 1	A	0	Address 1 is received
2nd	VECTOR 1	A	1	Vector = alphanumeric type
3rd	MESSAGE	A	1	Message word received "C" bit = 1, message is fragmented, more expected
4th	STATUS		1	End of frame indication (EOF = 1)
5th	ADDRESS 1	B	1	Address 1 is received
6th	VECTOR 1	B	2	Vector = alphanumeric type
7th	MESSAGE	B	2	Message word received "C" bit = 1, message is fragmented, more expected.
8th	Variable ¹		1	Host writes all frame mode packet to the MC68183 with the "DAF" bit = 1
9th	STATUS		1	End of frame indication (EOF = 1)
10th	ADDRESS 1	A	1	Address 1 is received
11th	VECTOR 1	A	2	Vector = alphanumeric type
12th	MESSAGE	A	2	Message word received "C" bit = 0, no more fragments are expected.
13th	Variable ¹		1	Host writes all frame mode packet to the MC68183 with the "DAF" bit = 1.
14th	Variable ¹		0	Host writes all frame mode packet to the MC68183 with the "DAF" bit = 1.

1. Host-initiated packet. The MC68183 returns a packet according to Appendix C, "Host-to-Decoder Packet Descriptions."

E.5 Operation of a Temporary Address

E.5.1 Group Messaging

The FLEX protocol allows for a dynamic group call for the purpose of sending a common message to a group of paging devices. The dynamic group call approach assigns a “Temporary Address” using the personal address and the short instruction vector.

The FLEX protocol specifies 16 addresses for the dynamic group call that may be temporarily activated in a future frame. (If the frame or one of the frames designated is equal to the present frame the host is to interpret this as the next occurrence of this frame 4 minutes in the future.) The temporary address is valid for one message that starts in the specified frame(s) and remains valid throughout the following frames to the completion of the message. If the message is not found in the specified frame(s), the host must disable the assigned temporary address.

The following describes the sequence of events between the host and the MC68183 required to handle a temporary address:

- Following an address packet, the host will receive a vector packet with $V_2V_1V_0 = 001$ and $i_2i_1i_0 = 000$ or 010 (a short instruction vector indicating a temporary address has been assigned to this pager). The system may send either $i_2i_1i_0 = 000$ or $i_2i_1i_0 = 010$ or both when assigning a temporary address.

The vector packet with $i_2i_1i_0 = 000$ will indicate which temporary address is assigned and the frame in which the temporary address is expected. The vector packet with $i_2i_1i_0 = 010$ will indicate which temporary address is assigned, the MSB of the expected frame (essentially indicating 64 frames in which to look for the temporary address), and a message sequence number. When the vector packet with $i_2i_1i_0 = 010$ is received on a long address, the specific assigned frame is included in the message word sent after the vector.

- The MC68183 will increment the corresponding temporary address counter for each temporary address assignment vector received and begin to decode all of the following frames. Note that this implies a single dynamic group assignment that is implemented by sending two short instructions (one for each temporary address assignment mode of the short instruction vector) will cause the corresponding temporary address counter to increment twice.
- The MC68183 continues to decode all of the frames and passes any address information, vector information and message information to the host followed by a status packet indicating the end of each frame and the current frame number.
- There are several scenarios which may occur with temporary addresses.
 - The temporary address is not found in any of the assigned frames and therefore the host must terminate the temporary address mode by sending an all frame mode packet to the MC68183 with the “DTA” bit of the particular temporary address set (if both temporary address assignment packets were used to assign the temporary address, the “DTA” bit must be set twice to disable the temporary address).
 - The temporary address is found in the frame it was assigned and was not a fragmented message. Again, the host must terminate the temporary address mode by sending an all frame mode packet to the MC68183 with the “DTA” bit of the particular temporary address set. (If both temporary address assignment packets were used to assign the temporary address, the “DTA” bit must be set twice to disable the temporary address.)
 - The temporary address is found in the assigned frame, and it is a fragmented message. The host must follow the rules for operation of a fragmented message and determine the proper time to stop the all frame mode operation. In this case, the host must write to the “DAF”

bit with a “1” and the appropriate “DTA” bit with a “1” in the all frame mode register in order to terminate both the fragmented message and the temporary address. (If both temporary address assignment packets were used to assign the temporary address, the “DTA” bit must be set twice to disable the temporary address).

- The above operation is repeated for every temporary address.

E.6 Using the Receiver Shut-Down Packet

E.6.1 Calculating Time Left

The receiver shut-down packet gives timing information to the host. Two times are of particular interest when implementing a roaming algorithm.

- **TimeToWarmUpStart.** Defined as the amount of time there is before the receiver will start to warm up (i.e. transition from the off state to the first warm-up state).
- **TimeToTasksDisabled.** Defined as the amount of time the host has to complete any host initiated tasks (e.g. by setting SND or SAS in the roaming control packet).

The formulas for calculating these times depend on whether the FLEXchip is in synchronous mode or asynchronous mode.

Synchronous Mode:

$$\text{TimeToWarmUpStart} \geq (\text{TNF} \cdot 80\text{ms}) + (\text{SkippedFrames} \cdot 1874.375\text{ms}) + \text{ReceiverOffTime} - 167.5\text{ms}$$

$$\text{TimeToTasksDisabled} \geq (\text{TNF} \cdot 80\text{ms}) + (\text{SkippedFrames} \cdot 1874.375\text{ms}) - 247.5\text{ms}$$

Asynchronous Mode:

$$\text{TimeToWarmUpStart} \geq ((\text{TNF} - 2) \cdot 80\text{ms}) + \text{ReceiverOffTime}$$

$$\text{TimeToTasksDisabled} \geq ((\text{TNF} - 3) \cdot 80\text{ms})$$

Where

TNF is the Time to Next Frame. Value received from the receiver shut-down packet.

SkippedFrames is the number of frames that will not be decoded. This can be calculated from the current frame (CF) and next needed frame (NAF) fields in the receiver shut-down packet. (For example, if CF is 10 and NAF is 12, SkippedFrames is 1.)

ReceiverOffTime is the time programmed in the receiver off setting packet.

E.6.2 Calculating How Long Tasks Take

Because the **TimeToTaskDisabled** discussed in the previous section limits how much the host can do while the MC68183 is battery-saving, it is necessary for the host to know how long it can take the MC68183 to perform a task.

The formulas below calculate how long the two types of host initiated tasks take to complete as measured from the last SPI clock of the packet that initiates the task to the time the receiver shut-down sequence starts. Note that the receiver shut-down sequence must start before tasks are disabled.

The following formula calculates how long it will take to complete a noise-detect started by setting the SND bit in the roaming control packet. This formula assumes either that the noise detect was performed while in synchronous mode, the noise-detect was performed in asynchronous mode and did not find FLEX signal, or that the noise detect found FLEX signal but the DAS bit of the roaming control packet was set.

$$\text{TimeToPerformNoiseDetect} \leq \text{TotalWarmUpTime} + 82\text{ms}$$

Where

TotalWarmUpTime: The sum of the times programmed for the used warm-up steps, plus the time programmed for the 3200sps sync setting in the receiver control-configuration packets.

The following formula calculates how long it will take to complete an A-word search initiated by setting the SAS bit in the roaming control packet. This formula assumes that the A-word search failed to find roaming FLEX channel.

$$\text{TimeToPerformAwordSearch} \leq \text{TotalWarmUpTime} + \text{AST} + 47\text{ms}$$

Where

TotalWarmUpTime: The sum of the times programmed for the used warm up steps plus the time programmed for the 3200sps Sync Setting in the receiver control configuration packets.

AST: The value configured using the timing control packet.

The following formula calculates how long it will take to complete a noise detect/A-word search combination. This can occur when the noise-detect is performed while in asynchronous mode, the noise detect finds FLEX signal, and the DAS bit of the roaming control packet is not set.


$$\text{TimeToPerformBoth} \leq \text{TotalWarmUpTime} + \text{AST} + 127\text{ms}$$

Where

TotalWarmUpTime: The sum of the times programmed for the used warm-up steps plus the time programmed for the 3200sps sync setting in the receiver control configuration packets.

AST: The value configured using the timing control packet.

OnCE and Mfax are registered trademarks of Motorola, Inc.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/Europe/Locations Not Listed:

Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
1 (800) 441-2447
1 (303) 675-2140

Motorola Fax Back System (Mfax™):

TOUCHTONE (602) 244-6609
1 (800) 774-1848
RMFAX0@email.sps.mot.com

Asia/Pacific:

Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-26629298

Technical Resource Center:

1 (800) 521-6274

DSP Helpline

dsphelp@dsp.sps.mot.com

Japan:

Nippon Motorola Ltd
SPD, Strategic Planning Office141
4-32-1, Nishi-Gotanda
Shinagawa-ku, Japan
81-3-5487-8488

Internet:

<http://www.motorola-dsp.com/>



MOTOROLA
