MIC8010

Liquid Crystal Display Driver

General Description

The MIC8010 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8010 is available in die form; contact the factory concerning dice and custom packaging requirements

Ordering Information

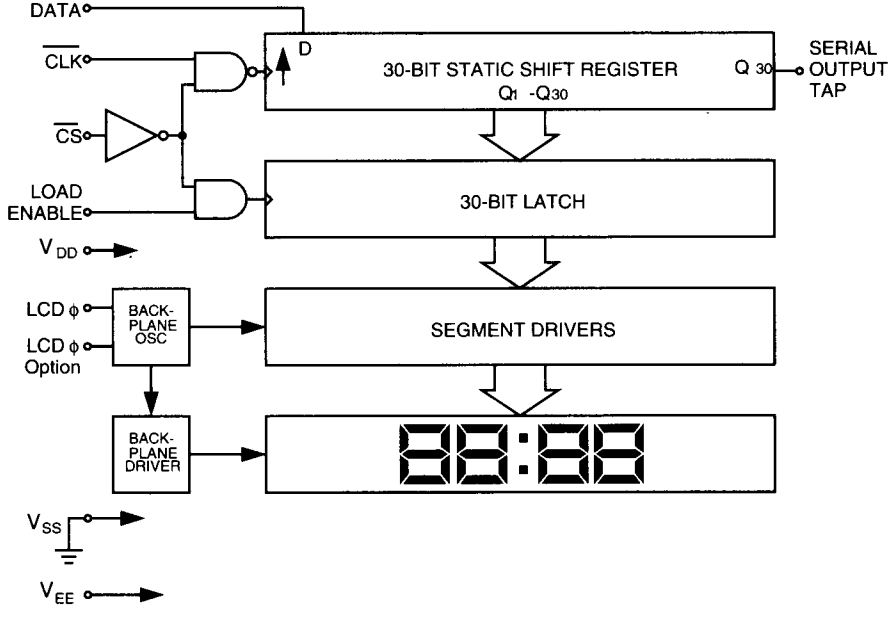
Part Number	Temperature Range	Package
MIC8010-01BN	–40°C to +85°C	40-pin Plastic DIP
MIC8010-02BN	–40°C to +85°C	40-pin Ceramic DIP
MIC8010-01AL	–55°C to +125°C	40-pin Ceramic LCC
MIC8010-02AL	–55°C to +125°C	40-pin Ceramic LCC

Features

- Pin-for-pin compatible with Holt HI8010
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Drives 30 segments
- Compatible with dichroic, midchroic, VF or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec or extended temperature range part available; contact factory for details
- Cascadable serial interface
- 60V extended output swing available; contact factory for details

4

Block Diagram



Note: The MIC8010 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Supply Voltage:
- V_{DD} –0.3V to +18V
- V_{EE} V_{DD} – 35V to +0.3V

Input Voltage (except LCDϕ) –0.3V to V_{DD} + 0.3V
LCDϕ Input Voltage V_{DD} – 35V to V_{DD} + 0.3V
DC Current Drain per input pin 10 mA

Operating Temperature Range:
- MIC8010-01BN, -02BN –40°C to +85°C
- MIC8010-01AL, -02AL –55°C to +125°C

Storage Temperature Range –65°C to +150°C
Power Dissipation 250 mW

DC Electrical Characteristics (Notes 3 and 4) V_{DD} = 5V, V_{EE} = –25V, V_{SS} = 0V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Operating Voltage	V_{DD}		3		18	V
Supply Current	I_{DD}	no load			200	µA
	I_{EE}	no load, f_{BP} = 100Hz			150	µA
Input Low Voltage	V_{IL}		0		1.3	V
(excluding LCDϕ)		–55°C to +125°C, V_{DD} = 4V to 16V			$0.2V_{DD}$	V
Input High Voltage	V_{IH}		2		V_{DD}	V
(excluding LCDϕ)		–55°C to +125°C, V_{DD} = 4V to 16V	$0.5V_{DD}$			V
Input Low Voltage (LCDϕ)	V_{ILX}		V_{EE}		2	V
		–55°C to +125°C, V_{DD} = 4V to 16V			$0.1V_{DD}$	V
Input High Voltage (LCDϕ)	V_{IHX}		2.5		V_{DD}	V
		–55°C to +125°C, V_{DD} = 4V to 16V	$0.9V_{DD}$			V
Input Current	I_{IN}	V_{DD} = 0 to 5V			1	µA
Input Capacitance	C_I	Note 5			5	pF
Segment Output Impedance	R_{SEG}	I_L = 10µA			10	kΩ
Backplane Output Impedance	R_{BP}	I_L = 10µA			450	Ω
Data Out Current	I_{DOT}	Source Current, V_{OH} = 4.5V			0.6	mA
	I_{DOL}	Sink Current, V_{OL} = 0.5V	–0.6			mA

AC Electrical Characteristics (Note 3) V_{EE} = –25V, V_{SS} = 0V, T_A = 25°C, no load, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Clock Period	t_{CL}	V_{DD} = 5V	1000			ns
		V_{DD} = 10V	500			ns
Clock Pulse Width	t_{CW}	V_{DD} = 5V	450			ns
		V_{DD} = 10V	220			ns
Data-In Setup	t_{DS}	V_{DD} = 5V	300			ns
		V_{DD} = 10V	150			ns
Data-In Hold	t_{DH}	V_{DD} = 5V	10			ns
		V_{DD} = 10V	10			ns
Chip Select Setup to Clock	t_{CSS}	V_{DD} = 5V	200			ns
		V_{DD} = 10V	100			ns
Chip Select Hold to Clock	t_{CSH}	V_{DD} = 5V	450			ns
		V_{DD} = 10V	220			ns
Load Setup to Clock	t_{LS}	V_{DD} = 5V	500			ns
		V_{DD} = 10V	280			ns

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Chip Select Setup to Load	t_{CSL}		0			ns
Load Pulse Width	t_{LW}	V_{DD} = 5V	500			ns
		V_{DD} = 10	300			ns
Chip Select Hold to Load	t_{LCS}		0			ns
Data Out Valid from Clock	t_{CDO}	V_{DD} = 5V			600	ns
		V_{DD} = 10V			300	ns

Note 1 **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2 All voltages are referred to V_{SS} = 0V.

Note 3 **Minimum** and **Maximum** values are 100% tested. **Typical** values represent the most likely parametric norm.

Note 4 $V_{DD} - 32V < V_{EE} - 5V$ is required for proper device operation.

Note 5 Guaranteed by design.

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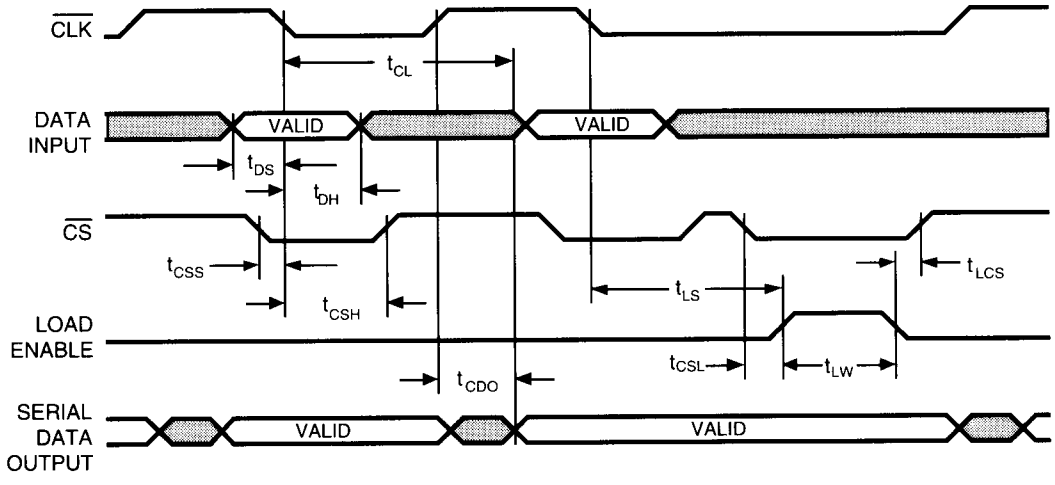
Timing Diagram



Applications Information

The MIC8010 utilizes a serial data interface as a means of programming the LCD segment outputs. The interface protocol is compatible with software written for the Holt HI-8010.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of $\overline{CLOCK}$, and the contents of the shift register exit at SERIAL DATA OUTPUT on the rising edges of $\overline{CLOCK}$. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

If data is shifted into the internal register but not immediately loaded into the latch, $\overline{CLOCK}$ should remain low. The driver may then be deselected without disturbing the contents of the shift register. If $\overline{CLOCK}$ is held high while $\overline{CHIP\ SELECT}$ is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting SERIAL DATA OUTPUT from one chip to DATA INPUT of the next. LOAD, $\overline{CLOCK}$, and $\overline{CHIP\ SELECT}$ are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line.

Power Supplies

The MIC8010 can operate from a single supply of V_{DD} = 4 to 18V, with V_{EE} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{EE} for segment/backplane voltage. V_{EE} is then negative with respect to V_{SS}, and the potential across V_{DD} and V_{EE} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{EE} to V_{DD}. For higher output voltage swing see the MIC8030 series devices.

Internal Oscillator

The on-chip oscillator (Figure 1) is available in two configurations. Devices with the "-01" suffix feature a 1-pin oscillator (LCDϕ and LCDϕ Option tied together). An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC} \div 256$. With R_{OSC} = 150kΩ and C_{OSC} = 470pF, f_{OSC} = 25.6kHz and f_{BP} = 100Hz.

Devices with a "-02" suffix bring out only LCDϕ, leaving LCDϕ Option disconnected. In this case LCDϕ is driven with an external clock; in a typically application several MIC8010-02 drivers would be slaved to a master MIC8010-01 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, dc manner. The feature is used in driving displays other than LCD displays, such as VF or LED. LCDϕ is connected to V_{DD} for this mode.

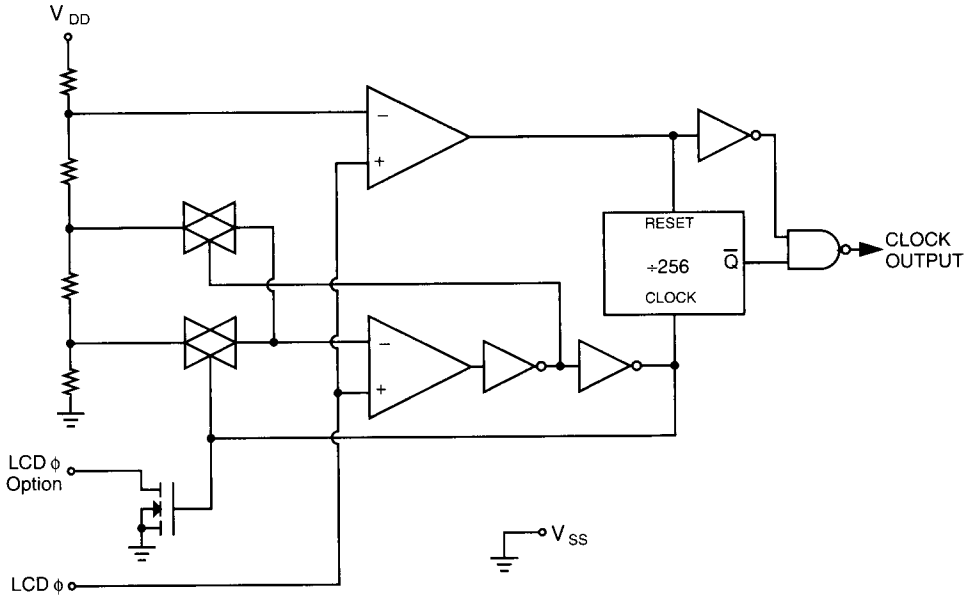


Figure 1. Internal Oscillator Circuit

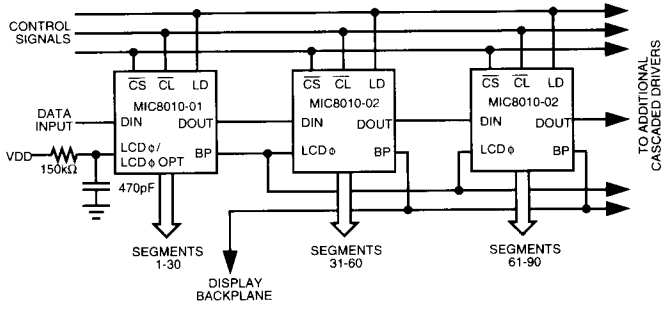


Figure 2. Cascading with Internal Clock Oscillator - 01 Configuration

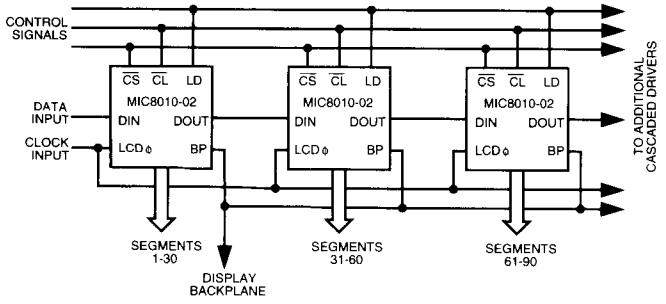


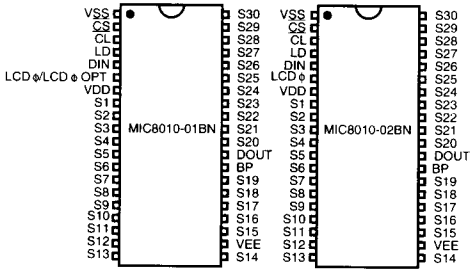
Figure 3. Cascading with External Clocking Source - 02 Configuration

Pin Assignments

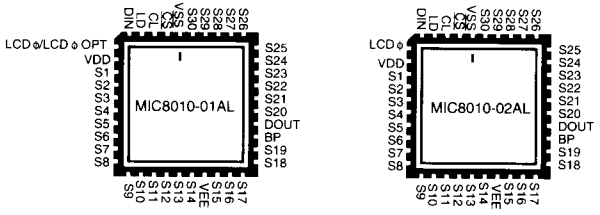
Function	Device Suffix -01	-02
Vss (Ground)	1	1
Chip Select	2	2
Clock	3	3
Load	4	4
Data Input	5	5
LCDφ	6	6
LCDφ Option	6	NC
VDD	7	7
Segment 1	8	8
Segment 2	9	9
Segment 3	10	10
Segment 4	11	11
Segment 5	12	12
Segment 6	13	13
Segment 7	14	14
Segment 8	15	15
Segment 9	16	16
Segment 10	17	17
Segment 11	18	18
Segment 12	19	19
Segment 13	20	20

Function	Device Suffix -01	-02
Segment 14	21	21
V_{EE}	22	22
Segment 15	23	23
Segment 16	24	24
Segment 17	25	25
Segment 18	26	26
Segment 19	27	27
Backplane	28	28
Data Output	29	29
Segment 20	30	30
Segment 21	31	31
Segment 22	32	32
Segment 23	33	33
Segment 24	34	34
Segment 25	35	35
Segment 26	36	36
Segment 27	37	37
Segment 28	38	38
Segment 29	39	39
Segment 30	40	40

Connection Diagrams



40-Pin Plastic DIP



40-Pin Ceramic Chip Carrier