Bt604

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

125 MHz
10KH ECL Compatible
Dynamically Programmed
Timing Edge Vernier

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Distinguishing Features

- 125 MHz Maximum Trigger Rate
- Less than ±1 LSB Timing Accuracy
- 15 ps Delay Resolution (4 ns Span)
- Extendable Delay Span to 40 ns
- Differential Trigger Inputs
- 10KH ECL Compatible
- Monolithic Construction
- 28-pin Plastic J-Lead (PLCC) Package

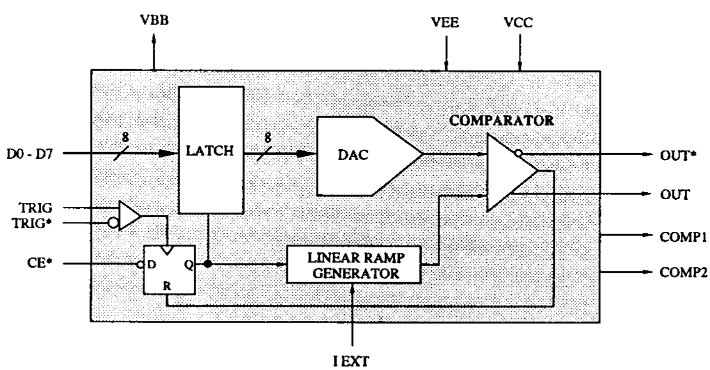
Applications

- Automatic Test Equipment
- Precision Timing Verniers
- Arbitrary Waveform Generators
- Multiple Phase Clock Generators
- Computer Backplane Timing

Related Products

- Bt605
- Bt110

Functional Block Diagram



Product Description

The Bt604 is a Dynamically Programmed Timing Edge Vernier, whose time delay is dynamically loaded upon each trigger of the circuit. In response to a trigger pulse, the Bt604 outputs a pulse of fixed width a programmable delay time later.

With the delay span set to 4 ns, the Bt604 features 15 ps of resolution (255 steps). The delay span is externally adjusted and is set in the range of 4 ns to 40 ns by IEXT.

The device is 10KH ECL compatible with ECL inputs and has a differential ECL input trigger and output pulse.

In applications for Automatic Test Equipment (ATE), the Bt604 forms the critical component in providing precise timing edges having fine resolution and excellent edge placement accuracy, and is suitable for use in testers featuring timing changes "on-the-fly."

The Bt604 also meets the need for programmable time delays in numerous electronic instruments that perform signal modulation, processing, and generation.

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Brooktree®

Circuit Description

As illustrated in the block diagram, the Bt604 contains an 8-bit D/A converter, a linear ramp generator, and a comparator.

Functional Operation

Referring to Figures 1 and 2, if CE* is a logical zero, the differential input trigger (TRIG, TRIG*) initiates a linear ramp on the rising edge of TRIG and latches the D0–D7 input data which sets the DAC output voltage.

The comparator detects when the ramp reaches the DAC's programmed value, whereupon it initiates an output pulse of fixed width and resets the ramp. Upon resetting the ramp, the input data latch is made transparent, enabling D0–D7 to reprogram the DAC and permitting another trigger of the Bt604.

Delay Calculations

Referring to Figure 2, the output pulse delay consists of a minimum output delay (Tmin) and a programmable output delay (Tprog). For D0–D7 equal to $00 the output delay will be Tmin and for $FF the output delay will be Tmax.

The span of the delay range is:

Tspan = Tmax – Tmin

The output pulse delays are adjustable and are set by IEXT current flow through pin 12. Figure 3 shows the relationships Tspan vs. IEXT and Tspan vs. Tmin. The following equations apply to Figure 3:

Tmin (max) = Tspan * 0.217 + 2.7
Tmin (min) = Tspan * 0.187 + 1.6
Tmin (max) – Tmin (min) = Tspan * 0.03 + 1.1

Referring to Figure 4:

IEXT = (VEXT + 1.25 V) / (REXT + 26 Ω)

Output Pulse Spacing

Consecutive output pulses must be spaced no less than 8 ns apart.

Conditions for Optimum Performance

The timing vernier is a mixed signal device and to obtain the maximum accuracy and stability over frequency there are specific conditions required. The following recommendations are for maintaining the lowest linearity errors and minimizing the absolute timing variations over frequency.

This product requires special attention to proper layout techniques to achieve correct operations. Before beginning PCB layout, please reference the information contained in Bt604 and Bt605 Evaluation Modules Operation and Measurements (AN-30), and follow proper high-speed ECL layout techniques.

Do not expect optimum performance when operating the device in a socket. Lead inductance, transmission line discontinuities and restricted air flow attributable to the use of a socket will degrade performance.

A transverse air flow of 400 linear feet per minute is very important when considering error sources in the magnitude of tens of picoseconds.

The ferrite chip bead selected for use with this device is critical. Use only the bead recommended. It is very important that this bead be mounted as close as possible to the VEE(1) power pins connecting the device to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE (1) pins will result in unstable operation.

Note that all components must be placed as close to the pins as possible, and that all VCC pins must be connected together.

The data set-up time for trigger of the device should be extended to 5 ns for on-the-fly applications. This will ensure the best dynamic performance when making full-scale transitions from code $FF to $00, which is when the worst case settling time conditions occur.

A constant trigger pulse width should be maintained to achieve the best absolute time performance over frequency. A trigger pulse width of Tmin – 500 ps is required to keep the falling edge of the trigger pulse width from occurring during the ramp.

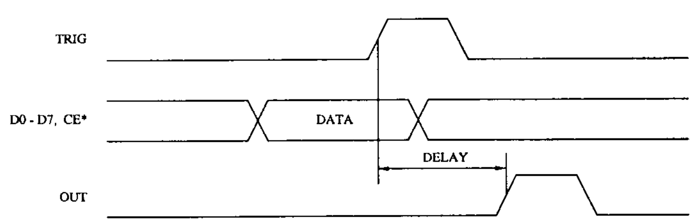


Figure 1. Input/Output Timing.

Circuit Description *(continued)*

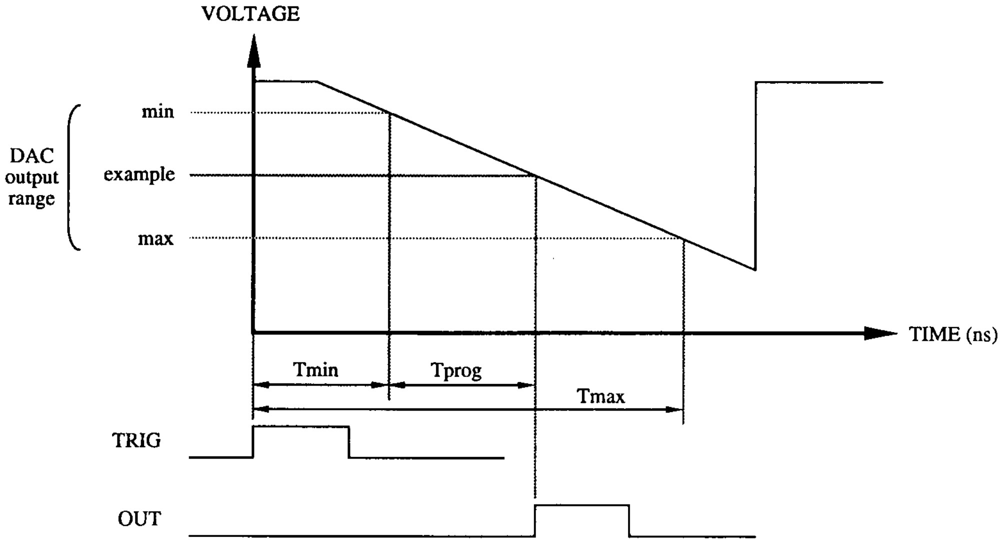


Figure 2. Linear Ramp and Output Pulse Timing.

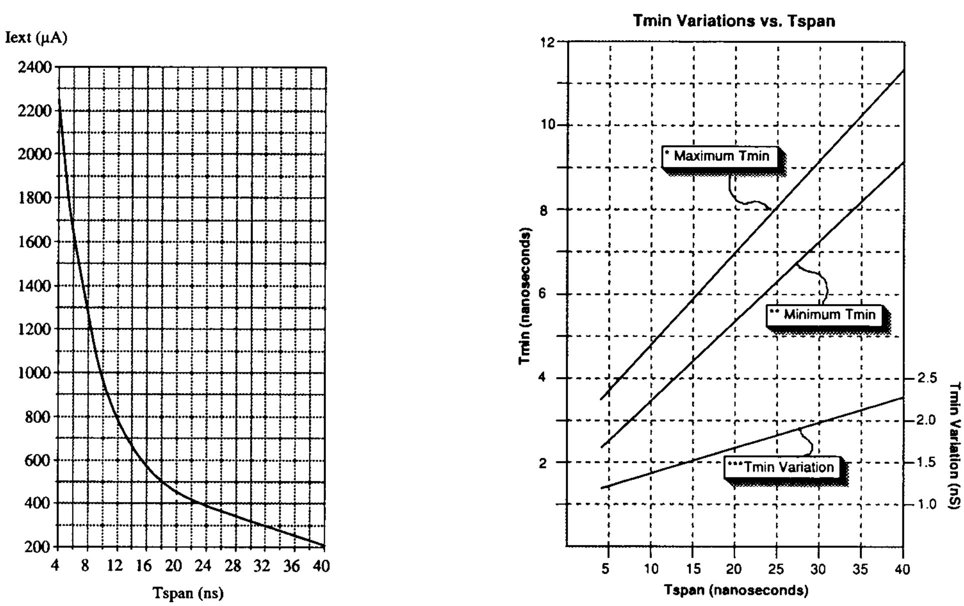
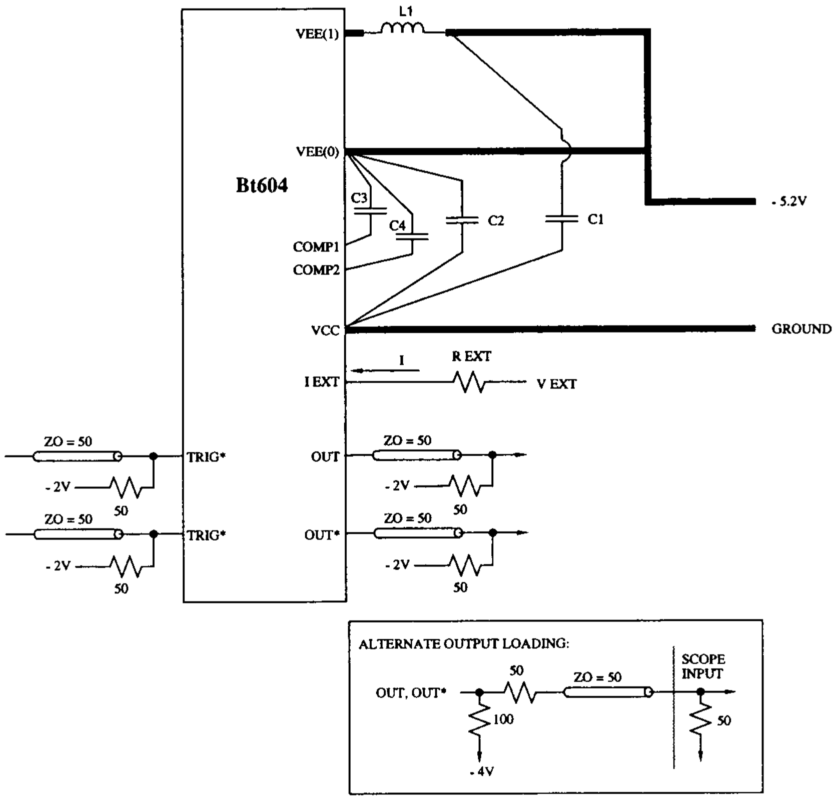


Figure 3. Typical Output Delays.

Circuit Description *(continued)*



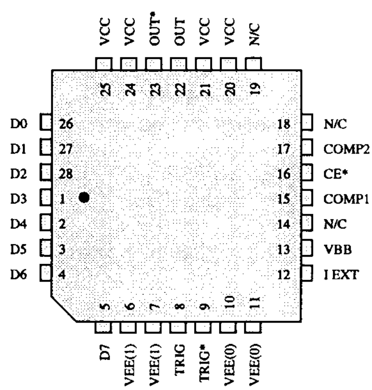
Location	Description	Vendor Part Number
C1–C4 L1 REXT	0.1 µF ceramic capacitor ferrite chip bead 1% metal film resistor (selected for proper Tspan)	Erie RPE112Z5U104M50V TDK HF70ACB322513 or TDK CB301210 Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt604. All devices should be as close as possible to the Bt604.

Figure 4. Typical Connection Diagram and Parts List.

Pin Descriptions

Pin Name	Description
D0–D7	Data input pins (ECL compatible). On the rising edge of TRIG, a ramp is initiated whereupon D0–D7 are latched into the device. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse. See Figure 1.
CE*	Chip enable input (ECL compatible). CE* must be a logical zero on the rising edge of the TRIG to enable the device to respond to the trigger. If CE* is floating, the trigger will always be enabled. See Figure 1.
TRIG, TRIG*	Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if CE* is a logical zero. If CE* is a logical one, no operation occurs. It is recommended that triggering be performed using differential inputs.
OUT, OUT*	Differential outputs (ECL compatible).
IEXT	Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically –1.25 V.
COMP1, COMP2	Compensation pins. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE(0) and also COMP2 and VEE(0). See Figure 4.
VEE	Device power. All VEE pins must be connected. **Warning: It is important that a ferrite chip bead be used to connect the VEE(1) power pins to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.**
VCC	Device ground. All VCC pins must be connected together.
VBB	–1.36 V (typical) output.



Note: N/C pins may be left floating without affecting the performance of the Bt604.

Application Information

Introduction

The Bt604 Timing Edge Vernier uses an external current source to set and calibrate the time delay span, Tspan. This section describes how Tspan may be set using external resistors and how an external diode may be used to improve, by a factor of approximately 3:1, the effects of temperature variations.

In applications where the output time delay may be measured, Tspan may be automatically calibrated using an external programmable current source. Also described is how this can be achieved in a cost effective manner using Brooktree's Bt110 CMOS Octal 8-bit DAC.

Tspan Temperature Compensation

The Bt604 exhibits small changes in Tspan with changes in temperature caused by temperature coefficient differences between the minimum time delay (Tmin) and the maximum time delay (Tmax), where:

$$\text{Tspan} = \text{Tmax} - \text{Tmin}$$

Tspan is set with an external current source (usually a resistor to a voltage VEXT) as shown in Figure 4. The Tspan positive temperature coefficient can be partially compensated with an external network exhibiting a negative temperature coefficient consisting of two resistors and an inexpensive 1N4148 diode (see Figure 5). Resistors R1 and R2 are selected from Table 1 according to the Tspan desired. R1 and R2 are metal film resistors. R2 is selected or trimmed to obtain the desired Tspan.

The 2 mV/°C decrease in the forward voltage drop across the diode provides the necessary small changes in current. This network is most effective over a temperature range of 40 to 60 °C. Also shown in Table 1 are the temperature coefficients that can be expected over this temperature range for a 10° change in temperature. This is not a linear function in all cases. For example, with a 5 ns Tspan, Tmin may decrease from 40 to 50 °C, and then increase from 50 to 60 °C. As a result, values shown are absolute values.

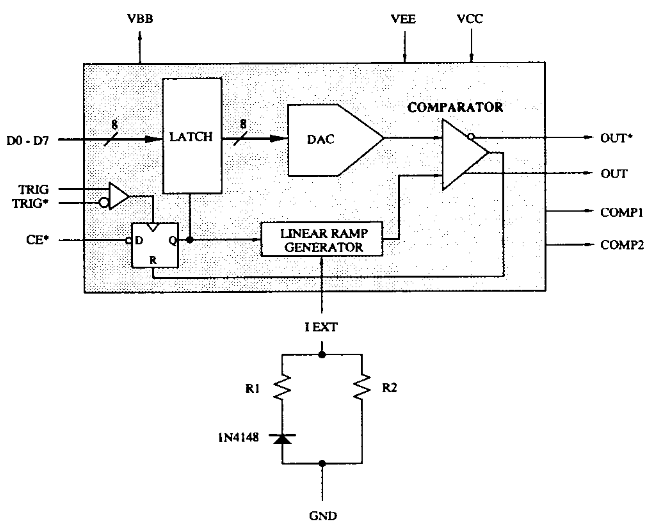


Figure 5. Typical Temperature Compensation Circuit.

Application Information *(continued)*

Tspan Calibration Using the Bt110

The accuracy and stability of the circuit providing the reference current (IEXT) directly affects the timing span accuracy. Computing values for R1 and R2 in Figure 5 results in a Tspan accuracy of better than ±20%. This may require the adjustment or trimming of R2 to set Tspan to the precision required by the application. Using the Bt110 CMOS Octal 8-bit DAC can eliminate the need to trim resistors and provides a cost-effective, low-power solution to Tspan calibration. The block diagram of the Bt110 is shown in Figure 6.

For example, the Bt604 requires a nominal external current of 1850 µA for a Tspan of 5 ns. When the span is set to 5 ns, the Tspan/IEXT ratio is typically 2.80 ps/µA. Setting Tspan with resistor values as per Table 1 could result in a Tspan error of ±20%, or ±1 ns. To correct for this error would require an adjustment of IEXT of ±1 ns divided by 0.0028 ns/µA or ±357 µA. If this IEXT adjustment is to be supplied by a DAC, then the full-scale range would need to be 2 x 357 = 714 µA. An 8-bit DAC with this range would have a calibration resolution of 714 µA divided by 255 or 2.8 µA per bit. This represents a calibration resolution of 2.8 µA times 2.8 ps/µA or 7.84 ps.

This can be stated more simply as:

- Setting Tspan with resistors results in an error of ±x%
- The Bt604 has 8 bits of resolution
- Calibrating with an 8-bit DAC results in a calibration resolution of 2x% of 1 LSB of the Bt604
- For Tspan = 5 ns
  1 LSB = 5 ns/255 = 19.6 ns
  Calibration resolution for ±x = ±20% is
  0.4 x 19.6 = 7.84 ps

The circuit shown in Figure 7 implements this using the Brooktree Bt110 CMOS Octal 8-bit DAC.

The output range of the Bt110 is set by R5:

Range (µA) = 1000*VREF (V) / R5 (Ω)

where VREF into the Bt110 may be set by the internal 1.2v reference of the Bt110. Using this internal reference, the full-scale gain error of the Bt110 is ±10%. Table 2 shows resistor values for the circuit in Figure 7.

As the Bt110 has eight 8-bit DACs, it is capable of calibrating up to eight Bt604s.

Tspan (ns)	R1 (Ω)	R2 (Ω)	Tmin Tempco (ps/°C)	Tmax Tempco (ps/°C)	Tspan Tempco (ps/°C)
5	1000	914	2.5	2.5	1.0
10	2000	2411	2.5	2.5	1.0
15	3300	3569	2.5	2.5	2.0
20	4700	4590	4.0	4.0	2.0

Table 1. Component Values for Figure 5.

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Application Information *(continued)*

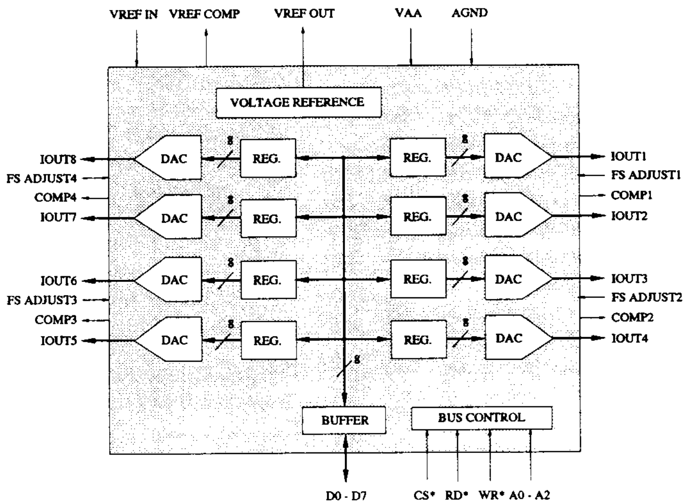

Figure 6. Block Diagram of the Bt110 Octal 8-Bit DAC.

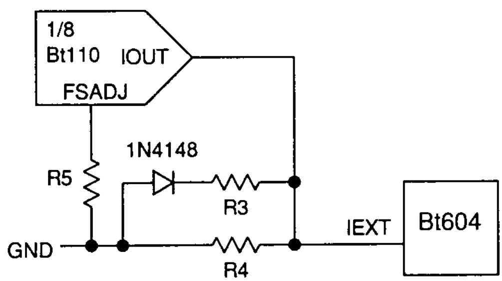

Figure 7. Tspan Calibration Using the Bt110.

Tspan (ns)	R3 (Ω)	R4 (Ω)	R5 (Ω)	Nominal Range of Bt110 DAC (μA)
5	1000	1456	1200	1000
10	2000	2700	2660	450
15	3300	3900	4800	250
20	4700	4700	10000	120

Table 2. Component Values for Figure 7.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	VCC	0	0	0	V
Power Supply	VEE	–4.9	–5.2	–5.5	V
Reference Current	IEXT	150		2500	μA
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to VCC)				–8.0	V
Voltage on Any Digital Pin		0		VEE	V
Output Current				–30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	–1170 –1130 –1070		–840 –810 –735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	–1950 –1950 –1950		–1480 –1480 –1450	mV mV mV
Output High Voltage	VOH	0 +25 +70	–1020 –980 –920		–840 –810 –735	mV mV mV
Output Low Voltage	VOL	0 +25 +70	–1950 –1950 –1950		–1630 –1630 –1600	mV mV mV
Input High Current (Vin = VIH max) TRIG, TRIG*	IIH IIH	FULL FULL			20 30	µA µA
Input Low Current (Vin = VIL min) TRIG, TRIG*	IIL IIL	FULL FULL			20 25	µA µA
Output Delay Spans Differential Linearity Error** Integral Linearity Error**	 DL IL	 FULL +25°–70° 0°			 ±0.9 ±1.0 ±1.25	 LSB LSB LSB
VBB Output Voltage	VBB	FULL	–1.44		–1.30	V
IEXT for Tspans Tspan = 4 ns Tspan = 5 ns Tspan = 10 ns Tspan = 15 ns Tspan = 20 ns Tspan = 30 ns	 IEXT	 FULL	 2.1 1.6 0.80 0.53 0.39 0.25	 2.375 1.85 0.925 0.615 0.455 0.295	 2.65 2.1 1.05 0.70 0.52 0.34	 mA mA mA mA mA mA
Tspan with IEXT = 1.7 mA (Tspan = Tmax – Tmin)		FULL	4.9		6.2	ns
Minimum Delay Time* Data = 00, Tspan = 5 ns Tspan = 10 ns	 Tmin	 FULL	 2.5 3.5		 3.8 4.9	 ns ns
VEE Supply Current	IEE	70° 0°, 25°		 145	200 210	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." OUT and OUT* loading with 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal supply, i.e., –5.2 V.

Note: The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

*For other minimum time delay values, refer to delay calculation equations in the Circuit Description section.
**Tested at 10 MHz trigger rate with span at 5 ns.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Trigger Rate (Note 1)	Fmax			125	MHz
Trigger Width High	TWI	2			ns
Output Pulse Width High Time	TWO	2.5		4.5	ns
Output Pulse Rise/Fall Time (20/80%)			550	750	ps
Output Pulse Spacing	TS	8			ns
Minimum Delay Time vs. Tspan					
ΔT00 / ns (Tspan = 5 ns to 10 ns)		180		220	ps / ns
Output Delay					
Tspan (Tspan = Tmax – Tmin)		4		40	ns
Resolution (Tspan / 255)		15.7		157	ps
Tempco (5 ns Span)					
ΔTspan / °C			6		ps / °C
ΔTmin / °C			4		ps / °C
Power Supply Rejection			100		ps / V
(Data = 0-FF HEX, Tspan = 5 ns)					
CE* Setup Time	TSU	2.0			ns
CE* Hold Time	TH	1.5			ns
D0–D7 Setup Time	TDSU	1			ns
D0–D7 Hold Time	TDH	1.5			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions." ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. OUT and OUT* loading with 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal supply, i.e., –5.2 V.

Note 1: Maximum Tspan and Trigger Rates:

Maximum Tspan (ns) Maintaining Linearity		Maximum Trigger Rate (MHz)	Minimum Trigger Period (ns)
of ±2 LSB	of ±1 LSB		
4.0	—	125	8
5.1	4.6	100	10
5.8	5.5	90	11.1
6.75	6.3	80	12.5
8.1	7.7	70	14.3
9.9	8.7	60	16.6
12.0	10.5	50	20.0
15.5	14.1	40	25.0
22.0	20.5	30	33.3

The information in this table is guaranteed but not 100% production tested. See Figures 8 and 9 for a graphic representation.

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AC Characteristics *(continued)*

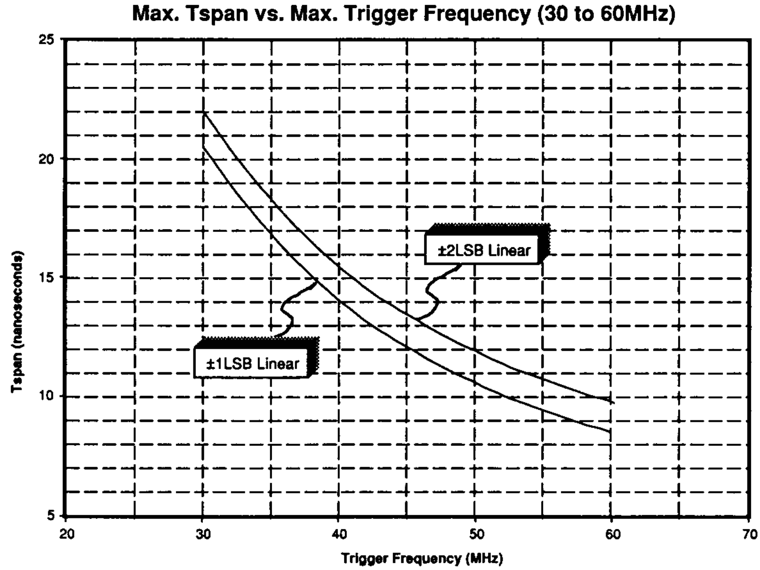

Figure 8. Bt604 Tspan vs. Frequency (30–60 MHz).

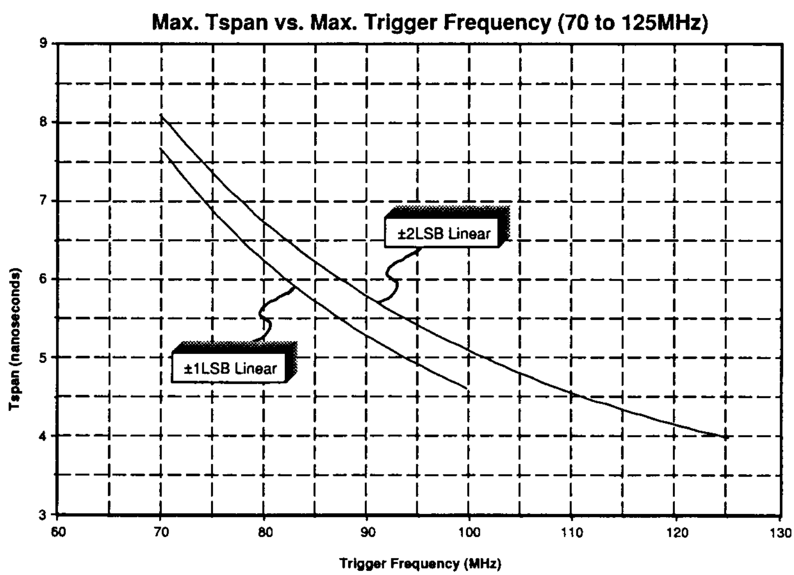

Figure 9. Bt604 Tspan vs. Frequency (70–125 MHz).

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt604KPJ	28-pin Plastic J-Lead	0° to +70° C

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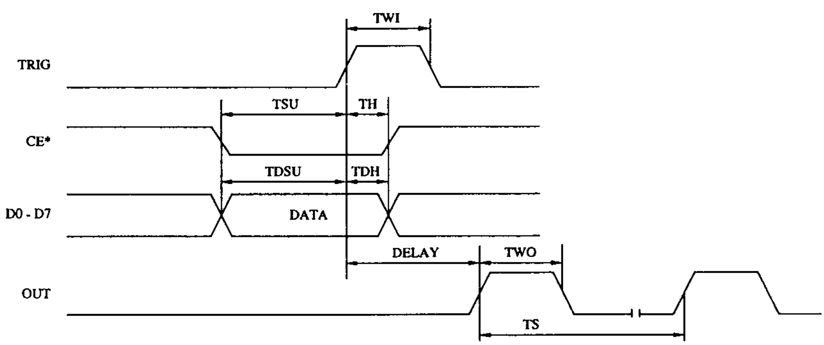
Timing Waveforms



Input/Output Timing.