

DM7220/DM8220 9-Bit Parity Generators/Checkers

General Description

These circuits can be used both to check for parity and to generate a parity bit. When the generation of a parity bit is desired, the eight data inputs are connected to the transmission lines. If a low logic level is then connected to the parity input, the circuit will generate odd parity. The succeeding parity checker will acknowledge an odd number of "1's" (odd parity) with a low logic level on its output. If a high logic level is connected to the parity input of the first parity generator, the parity checker will acknowledge even parity with a high logic level on its output, although the output of the parity generator will be low.

Features

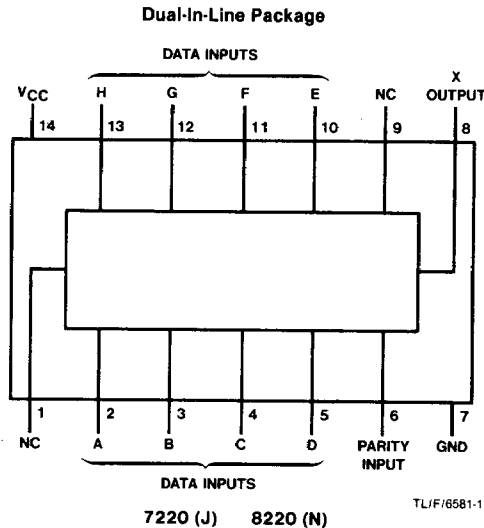
- Typical propagation delay 34 ns
- Typical power dissipation 130 mW

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	- 65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram



Recommended Operating Conditions

Symbol	Parameter	DM7220			DM8220			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			16			16	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -12 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	2.4			V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max			0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.4V			40	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-1.6	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM72	-20	-55	mA
			DM82	-18	-55	
I _{CC}	Supply Current	V _{CC} = Max		26	35	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R _L = 400Ω C _L = 15 pF			Units
		Min	Typ	Max	
t _{PLH} Propagation Delay Time Low to High Level Output	Data to Output		36	58	ns
t _{PHL} Propagation Delay Time High to Low Level Output	Data to Output		32	52	ns
t _{PLH} Propagation Delay Time Low to High Level Output	Parity to Output		21	35	ns
t _{PHL} Propagation Delay Time High to Low Level Output	Parity to Output		14	25	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Function Table

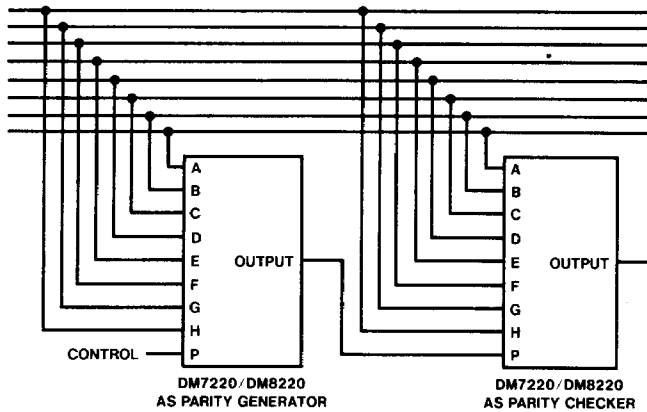
Parity Input	Output*	Inputs A Thru H
H	L	Even number of inputs are High
L	L	Odd number of inputs are High

*Single device

Typical Application

If the control line is a logical "0" the parity generator will generate odd parity. The parity checker will acknowledge the presence of an odd number of "1's" (odd parity) with a logical "0" on its output.

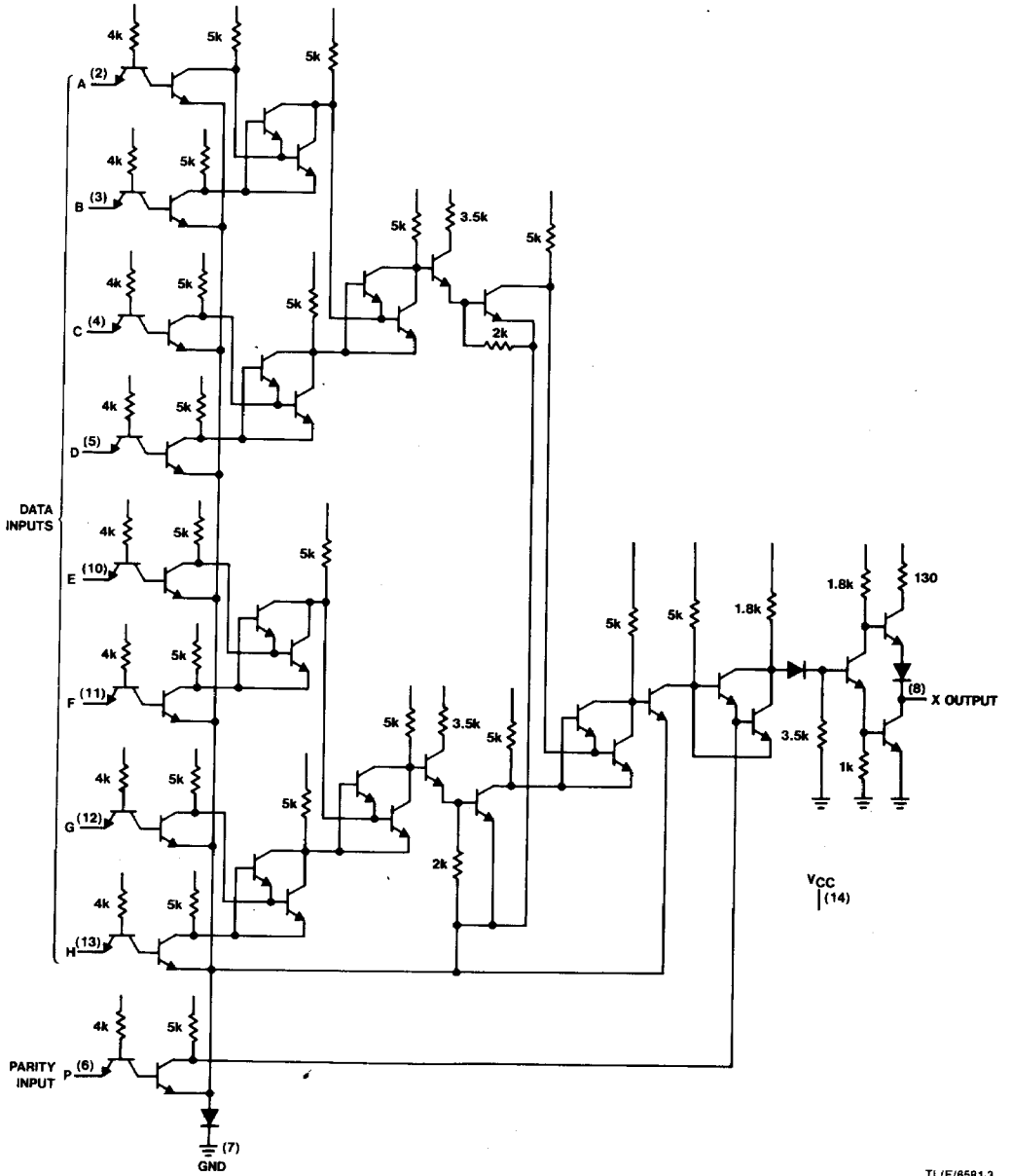
If the control line is a logical "1" the parity generator will generate even parity. The parity checker will acknowledge the presence of an even number of "1's" (even parity) with a logical "1" on its output.



TL/F/6581-2

Schematic Diagram

72/8220



TL/F/6581-3