



MICRO NETWORKS

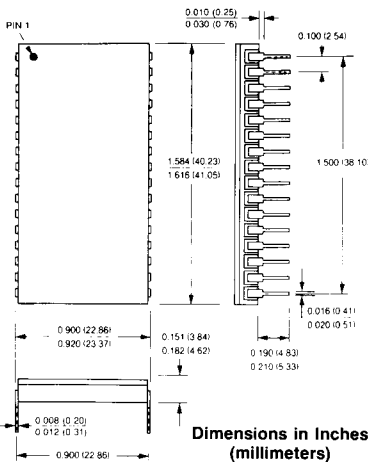
MN6295 MN6296

LOW-DISTORTION, 50kHz
16-Bit, SAMPLING
A/D CONVERTERS

FEATURES

- 50kHz Sampling Rate With Internal T/H Amplifier
- 25kHz Full-Power Input Bandwidth
- 84dB Signal-to-Noise Ratio Over Full Bandwidth
- -88dB Harmonics Over Full Bandwidth
- FFT Testing
- Serial and Parallel Outputs
- 1.3 Watts Power Consumption
- 32-Pin Side-Brazed DIP
- Fully Specified 0°C to +70°C (J and K Models) or -55°C to +125°C (S and T Models)
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

32 PIN SIDE-BRAZED DIP



DESCRIPTION

The MN6295/6296 Family of 50kHz, 16-bit, sampling A/D converters offers an outstanding combination of resolving power, sampling rate, low noise and low harmonic distortion. These SA type A/D's are packaged in small, side-brazed, 32-pin, triple-wide DIP's and have internal track-hold (T/H) amplifiers that enable them to accurately sample and digitize 25kHz full-scale input signals at rates up to 50kHz. The package, including the internal T/H, is smaller than that of most stand-alone 16-bit A/D's. Each device is fully FFT (Fast Fourier Transform) tested using contemporary DSP technology and guarantees up to 84dB signal-to-noise ratio (SNR, rms-to-rms) and up to -88dB harmonics and spurious noise.

MN6295 (10V input span) and MN6296 (20V input span) are configured in a manner that makes their internal T/H completely user transparent. A 2.5kΩ input resistor isolates the T/H from its signal source, and the T/H's operational mode is internally controlled by the A/D's status line. Users need only supply start-convert pulses at the desired sampling rate. Each device is fully tested both statically, in the traditional manner, and dynamically with a series of 512-point FFT's. This type of configuration and testing eliminates the need for potentially confusing and misleading T/H specifications like aperture delay, aperture jitter, charge injection, etc., and also eliminates frustrating attempts to translate data-converter time-domain specifications into frequency-domain performance.

The MN6295/6296 Family offers 4 electrical performance grades (J,K,S and T part-number suffixes) and 2 operating temperature ranges (0°C to +70°C and -55°C to +125°C).

MN6295/96



MICRO NETWORKS

324 Clark St., Worcester, MA 01606 (508) 852-5400

April 1990

MN6295 MN6296 50kHz SAMPLING 16-Bit A/D CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	-55°C to +125°C
Specified Temperature Range:	
MN6295J, K; MN6296J, K	0°C to +70°C
MN6295S, S/B, T, T/B	-55°C to +125°C
MN6296S, S/B, T, T/B	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Positive Supply (+Vcc, Pin 28)	0 to +16.5 Volts
Negative Supply (-Vcc, Pin 21)	0 to -16.5 Volts
Logic Supply (+Vdd, Pin 30)	0 to +7 Volts
Digital Inputs (Pins 31, 32)	0 to +5.5 Volts
Analog Inputs (Pins 24, 25)	±15 Volts
Analog Ground (Pin 22)	
to Digital Ground (Pin 19)	±1 Volt
Ref. Out (Pin 23) Short Circuit Duration	Continuous to Ground

ORDERING INFORMATION

PART NUMBER _____ **MN6295T/B CH**

Select MN6295 or MN6296. _____

Select suffix J, K, S or T for _____

desired performance and specified _____

temperature range. _____

Add "/B" to "S" or "T" models for _____

Environmental Stress Screening. _____

Add "CH" to "S/B" or "T/B" models _____

for 100% screening according to _____

MIL-H-38534. _____

Contact factory for availability of "CH" _____

device types.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, ±Vcc = ±15V, +Vdd = +5V unless otherwise indicated) (Note 1)

	MIN.	TYP.	MAX.	UNITS
ANALOG INPUTS				
Input Voltage Ranges: MN6295 MN6296		0 to +10, ±5 ±10		Volts Volts
Input Impedance (Note 17): Resistance Capacitance		2.5 50		kΩ pF
DIGITAL INPUTS (Start, Short Cycle)				
Logic Levels: Logic "1" Logic "0"	+2.0		+0.8	Volts Volts
Logic Currents: Logic "1" (V _{IH} = +2.4V) Logic "0" (V _{IL} = +0.4V)			+40 -1.6	μA mA
DIGITAL OUTPUTS (Serial, Parallel, Status, Clock)				
Output Coding (Note 2): Unipolar Ranges Bipolar Ranges		CSB COB		
Logic Levels: Logic "1" (I _{source} ≤ 320μA) Logic "0" (I _{sink} ≤ 3.2mA)	+2.4		+0.4	Volts Volts
INTERNAL REFERENCE				
Reference Output (Pin 23): Voltage Drift Output Current (Notes 3, 17)	+9.9	+10 ±15	+10.1 1	Volts ppm/°C mA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: ±Vcc Supply +Vdd Supply	±14.5 +4.5	±15 +5	±15.5 +5.5	Volts Volts
Power Supply Rejection (Note 14): +Vcc Supply -Vcc Supply +Vdd Supply		±0.003 ±0.003 ±0.001	±0.02 ±0.02 ±0.01	%FSR/%Supply %FSR/%Supply %FSR/%Supply
Current Drains: +Vcc Supply -Vcc Supply +Vdd Supply		+42 -30 +48	+55 -40 +60	mA mA mA
Power Consumption		1320	1725	mW

PERFORMANCE SPECIFICATIONS (Typical T_A = +25°C, ±V_{cc} = ±15V, +V_{dd} = +5V unless otherwise indicated)

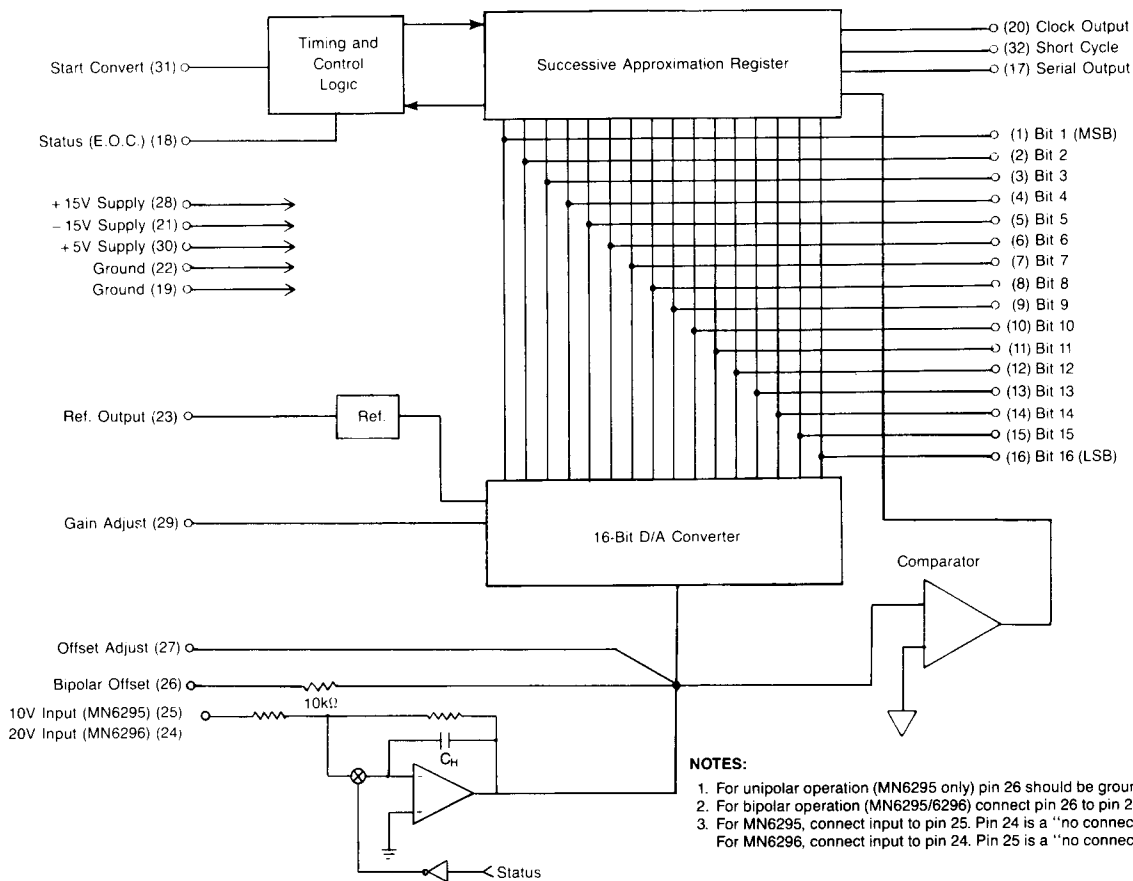
DYNAMIC CHARACTERISTICS	MN6295J MN6296J	MN6295K MN6296K	MN6295S MN6296S	MN6295T MN6296T	UNITS
Minimum Guaranteed Sampling Rate (Note 4)	50	50	50	50	kHz
Maximum A/D Conversion Time (Note 5)	16	16	16	16	μsec
Signal-to-Noise Ratio (SNR, Note 6):					
Initial (+25°C) (Minimum)	80	84	80	84	dB
T _{min} to T _{max} (Minimum, Note 7)	78	82	78	82	dB
Harmonics and Spurious Noise (Note 8):					
Initial (+25°C) (Minimum)	-85	-88	-85	-88	dB
T _{min} to T _{max} (Minimum, Note 7)	-82	-85	-82	-85	dB
Input Signal Full-Scale Bandwidth (Minimum, Note 9)	25	25	25	25	kHz
STATIC CHARACTERISTICS					
Integral Linearity Error: Initial (+25°C) (Max. Note 16)	± 0.006	± 0.003	± 0.006	± 0.003	%FSR
T _{min} to T _{max} (Maximum, Note 7)	± 0.012	± 0.006	± 0.012	± 0.006	%FSR
Resolution for Which No Missing Codes is Guaranteed: Initial (+25°C)	13	14	13	14	Bits
T _{min} to T _{max} (Note 7)	13	14	13	14	Bits
Unipolar Offset Error (Notes 10, 11):					
Initial (+25°C) (Maximum)	± 0.05	± 0.05	± 0.05	± 0.05	%FSR
Drift (Maximum)	± 15	± 7.5	± 15	± 7.5	ppm of FSR/°C
Max Error T _{min} to T _{max} (Note 7, 15)	± 0.12	± 0.084	± 0.2	± 0.125	%FSR
Bipolar Zero Error (Notes 10, 12):					
Initial (+25°C) (Maximum)	± 0.075	± 0.05	± 0.075	± 0.05	%FSR
Drift (Maximum)	± 15	± 10	± 15	± 10	ppm of FSR/°C
Max Error T _{min} to T _{max} (Note 7, 15)	± 0.15	± 0.1	± 0.225	± 0.15	%FSR
Full Scale Accuracy Error (Notes 10, 13):					
Initial (+25°C) (Maximum)	± 0.2	± 0.1	± 0.2	± 0.1	%FSR
Drift (Maximum)	± 30	± 20	± 30	± 20	ppm of FSR/°C
Max Error T _{min} to T _{max} (Note 7, 15)	± 0.35	± 0.2	± 0.5	± 0.3	%FSR

SPECIFICATION NOTES:

- Detailed timing specifications appear in the Timing sections of this data sheet.
- CSB=complementary straight binary.
COB=complementary offset binary.
See table of transition voltages in section labeled Digital Output Coding.
- In addition to supplying 1mA of current for bipolar offsetting purposes (pin 23 connected to pin 26), the internal reference is capable of driving up to 1mA into an external load. If the internal reference is used to drive an external load, the load should not change during a conversion.
- Minimum guaranteed sampling rate refers to the fact that these devices guarantee all other performance specs while sampling and digitizing at a 50kHz rate. Obviously, devices may be operated at lower sampling frequencies if desired and typically will meet all performance specs while sampling at rates of 55kHz or higher.
- Whenever Status (pin 18) is low (logic "0"), the internal T/H is in the track mode, and the A/D converter is not converting. When Status is high (the definition of A/D conversion time), the T/H is in the hold mode, and the A/D is performing a conversion.
- This parameter represents the rms-signal-to-rms-noise ratio in the output spectrum (excluding harmonics) with a full-scale input sine wave (0dB) at any frequency up to 25kHz.
- MN6295J, K and MN6296J, K are fully specified for 0°C to +70°C operation. MN6295S, S/B, T, T/B and MN6296S, S/B, T, T/B are fully specified for -55°C to +125°C operation.
- This parameter represents the peak signal to peak non-fundamental component (harmonic or spurious, inband or out of band) in the output spectrum.
- This is the highest-frequency, full-scale, input signal for which the SNR and harmonic figures are guaranteed when sampling at a 50kHz rate.
- Adjustable to zero with external potentiometer.
- Unipolar offset error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 0000 0000 0000 0000 to 0000 0000 0000 0001 when operating the MN6295 on its unipolar range. The ideal value at which this transition should occur is -½LSB. See Digital Output Coding.
- Bipolar zero error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1000 0000 0000 0000 to 0111 1111 1111 1111 when operating the MN6295/6296 on a bipolar range. The ideal value at which this transition should occur is +½LSB. See Digital Output Coding.
- Full scale accuracy specifications apply at negative full scale for unipolar input ranges and at both positive and negative full scale for bipolar input ranges. Full scale accuracy error is defined as the difference between the ideal and the actual input voltage at which the digital output just changes from 1111 1111 1111 1110 to 1111 1111 1111 1111 for unipolar and bipolar input ranges. Additionally, it describes the accuracy of the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition for bipolar input ranges.
- Power supply rejection is defined as the change in the analog input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 or 0000 0000 0000 0000 to 0000 0000 0000 0001 output transitions occur versus a change in power-supply voltage.
- Listed maximum error-over-temperature specifications for unipolar offset, bipolar zero and full scale accuracy correspond to the combination of maximum room-temperature errors and worst case drift conditions to describe the worst case error that might be encountered over the entire specified temperature range.
- ±0.006%FSR is equivalent to ±½LSB for 13 bits and is equal to ±0.6mV for a device with a 10V full scale range (0 to -10V or ±5V input range). ±0.003%FSR is equivalent to ±¼LSB for 14 bits and is equal to ±0.3mV for a device with a 10V full scale range.
- These parameters are listed for reference only and are not tested.

Specifications subject to change without notice as Micro Networks reserves the right to make improvements and changes in its products.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — MN6295 and MN6296 are 16-bit, sampling, A/D converters. Each contains a 16-bit successive-approximation type A/D and a companion track-hold (T/H) amplifier. The T/H's enable MN6295 and MN6296 to accurately and repetitively sample and digitize dynamically changing input signals in both traditional data-acquisition and contemporary DSP-type applications.

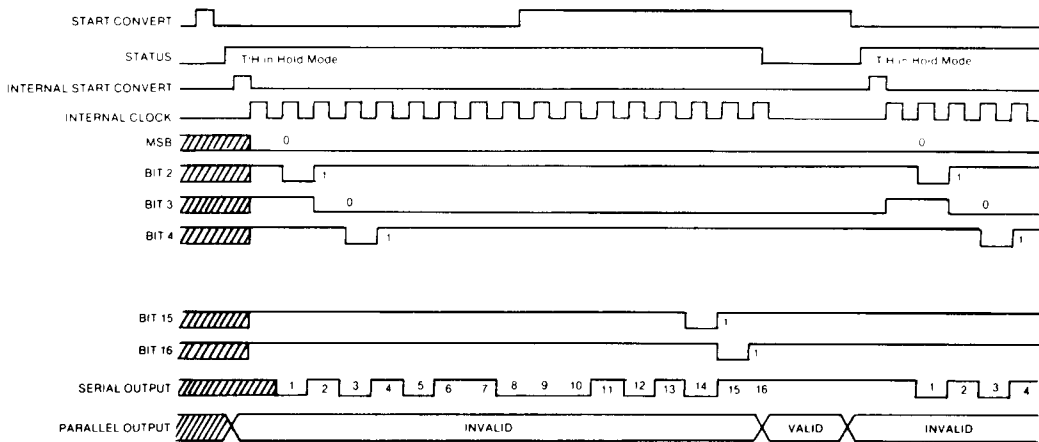
Successive approximation (SA) type A/D converters, when operated without the aid of T/H amplifiers, are severely limited in their ability to accurately convert changing analog input signals. The traditional rule of thumb for gauging such performance is that the A/D's are incapable of accurately converting signals that are slewing faster than $(\pm 1/2 \text{ LSB})/(\text{conversion time})$. For a 14-bit A/D with an input range of $\pm 10\text{V}$ and a conversion time of $16\mu\text{sec}$, this corresponds to an input slew-rate limit of $\pm 38\mu\text{V}/\mu\text{sec}$. If one wishes to express the slew-rate limit as a bandwidth for a full-scale input sinusoid, it corresponds to 0.61Hz.

The proliferating use of A/D converters in DSP applications has resulted in significantly greater demands on A/D's to be able to convert dynamic signals, particularly sinusoids. More and more frequently, T/H amplifiers are used with A/D's to enable them to accomplish this task.

MN6295/6296 are extremely user friendly. They have been configured in a manner that virtually eliminates all of the problems encountered when mating T/H's and successive approximation A/D's and driving the pair from real-world signal sources. The T/H is truly transparent. A $2.5\text{k}\Omega$ input resistor isolates it from the external signal source, and its output is internally connected directly to the input of the A/D converter. The output current, impedance and transient-response characteristics of the T/H have been optimized for driving the 16-bit SA A/D. More importantly, the critical dynamic characteristics of the T/H (aperture delay, aperture jitter, small and large signal bandwidths, droop rate, etc.) have been similarly optimized. Most importantly, the critical inter-device timing relationships (T/H mode control, transient decay time, etc.) are internally controlled by MN6295/6296's timing and control circuitry. All that users need to provide externally is the start convert pulse.

The falling edge of the start convert pulse activates MN6295/6296's internal timing circuitry. Immediately, the T/H (which has been in the track or signal-acquisition mode up until this time) is driven into the hold mode, instantaneously "freezing" the value of the analog input signal. Simultaneously, MN6295/6296's status output (also called "End of Conversion" or E.O.C.) is set to a logic "1", indicating that the T/H is now in hold; that an A/D conversion is now in progress;

TIMING DIAGRAM



SPECIFICATIONS ($T_A = +25^\circ\text{C}$, $\pm V_{CC} = \pm 15\text{V}$, $+V_{DD} = +5\text{V}$ unless otherwise indicated)

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Conversion Time (16 Bits) (Note 6)		15	16	μsec
Internal Clock Frequency (Notes 4, 8)	110	1.07	1.19	MHz
Start Convert Pulse Width (Notes 2, 7)	40			nsec
Delay Falling Edge of Start to (Note 8): Status = "1" Clock Output = "1"		30 350		nsec nsec
Delay Rising Clock Edge to Output Data Valid (Parallel, Serial, Status) (Note 8)	20		50	nsec
Delay LSB Valid to Falling Edge of Status (Notes 3, 8)	20	40		nsec

TIMING DIAGRAM NOTES:

- Operation shown is for the digital word 0101 0110 0010 1011.
- The Start Convert command can be either a positive or negative pulse at least 40nsec wide. Conversions are initiated on the falling edge of the Start Convert command.
- Data will be valid 20nsec prior to the falling edge of Status (E.O.C.).
- The internal clock is enabled and the conversion commences following an internal delay which allows for T/H switching and settling.
- When the converter is initially "powered up" it may come on at any point in the conversion cycle.
- Conversion time is defined as the width of the Status (E.O.C.) pulse.
- The minimum time between falling edges of the Start Convert command is 20 μsec .
- These parameters are listed for reference only and are not tested.

and that the parallel output data (from the previous conversion) is no longer valid. MN6295/6296's internal timing logic now provides approximately 350nsec of delay to permit the track-to-hold switching transient at the output of the T/H to decay. Subsequently, the internal clock is started, and the 16-bit A/D conversion of the held signal proceeds.

The value of the hold capacitor used in MN6295/6296's internal T/H has been selected so that T/H output droop, even over temperature, is not significant (greater than $\pm 1/2$ LSB) during the A/D's conversion time. Similarly, the offset and pedestal voltages, as well as the gain error, of the T/H do not contribute to the overall accuracy of the sampling A/D because they are effectively nulled out during our active laser trimming of the A/D converter.

At the completion of the A/D conversion, MN6295/6296's internal control logic turns off the internal clock; drops the status output back to a logic "0"; and commands the T/H back into the track mode to acquire a new input signal. Status going low signifies that the conversion is complete and that the parallel output data is valid. A 20nsec delay has been added between the finalization of the LSB and the falling edge of status. This ensures that all output bits are valid when status falls and permits the use of this trailing edge to clock data into output latches. Output data remains valid until the falling edge of the next start convert pulse.

LAYOUT CONSIDERATIONS — Proper attention to layout and decoupling is necessary to obtain specified accuracies from MN6295/6296. The unit's two ground pins (pin 19 and 22) are not connected to each other internally. They must be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane beneath the package. If the grounds must be run separately, a non-polarized 0.01 μF ceramic bypass capacitor should be connected between the analog ground (pin 22) and digital ground (pin 19) as close to the unit as possible. Wide conductor runs should be employed.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Bipolar Offset (pin 26), Analog Input (pins 24,25), Offset Adjust (pin 27) and Gain Adjust (pin 29) are particularly noise susceptible. Care should be taken to avoid long runs or runs close to digital lines when utilizing these inputs. Input signal lines should be as short as possible. In bipolar operation, where Bipolar Offset (pin 26) is connected to Reference Output (pin 23), a short jumper should be used. For unipolar operation (MN6295 only) pin 26 should be grounded. For external gain or offset adjustment, the series resistor(s) should be located as close to Offset Adjust (pin 27) or Gain Adjust (pin 29) as possible. A 0.01 μF capacitor should be connected between Gain Adjust (pin 29) and Analog Ground as close to the package as possible.

Power supplies should be decoupled with tantalum and ceramic capacitors located close to the MN6295/6296. For optimum performance and noise rejection, 1 μ F tantalum capacitors paralleled with 0.01 μ F ceramic capacitors should be used.

If short-cycling is not used, the Short-Cycle pin (pin 32) must be connected to +5V (pin 30).

THE INTERNAL T/H AMPLIFIER

As stated in the Description of Operation, MN6295/6296's internal T/H amplifier is transparent to the user. The T/H's output is connected directly to the A/D's input and its operational mode is controlled by the Timing and Control Logic (see Block Diagram). The user is not required to supply additional support timing circuits sometimes necessary when mating an A/D with its companion T/H. Additionally, MN6295/6296 users need not concern themselves with oftentimes confusing T/H specifications like acquisition time, aperture-delay time, aperture jitter, droop rate, etc.. These parameters are not specified for MN6295/6296 and are, in fact, impossible to directly test because the T/H's output and control lines are not accessible at the device pins. Frequency-domain specifications like input bandwidth, sampling rate, signal-to-noise ratio, harmonic distortion, etc. obviates the need for knowing the specific T/H time-domain specifications, however, the following table does supply typical values for those critical T/H performance specifications.

Note that the static errors (gain error, track-mode offset error and pedestal) of the T/H function add directly to the corresponding errors of the A/D converter but that both are effectively nulled with the functional laser trimming of the A/D. T/H offset error and pedestal, for example, add directly to A/D converter offset error. However, when the A/D offset is functionally laser trimmed, it is done with the whole device sampling at a 50kHz rate and the T/H is in the hold mode whenever trimming is actually performed. Consequently, all error sources are compensated for. All static errors on MN6295/6296 (accuracy error, unipolar offset error, bipolar zero error, etc.) are tested and specified as full input-output transfer specifications and include both the T/H and A/D.

Typical T/H Performance Specifications	
Gain Error	$\pm 0.01\%$
Gain Linearity Error	$\pm 0.001\%$ FSR
Track Mode Output Offset Error	$\pm 0.5\text{mV}$
Pedestal	$\pm 0.5\text{mV}$
Acquisition Time: 10V step to $\pm 0.003\%$	2.5 μsec
20V step to $\pm 0.003\%$	3 μsec
Track-Hold Transient Settling (to $\pm 1\text{mV}$)	250nsec
Slew Rate	$\pm 30\text{V}/\mu\text{sec}$
Full Power Bandwidth	500kHz
Effective Aperture Delay Time	-25nsec
Aperture Jitter	0.4nsec
Droop Rate	$\pm 0.05\mu\text{V}/\mu\text{sec}$
Hold-Mode Feedthrough Attenuation	-86dB

PARALLEL OUTPUTS—During the successive approximation process the weight of each bit is compared to the value of the analog input voltage. The converter is reset to MSB-0111 1111 1111-LSB by the rising edge of the first clock pulse. Subsequent rising clock edges set the bit previously tested to its final state and brings the next bit to be tested to a logic "0". This process continues until all bits have been tested and Status returns to a logic "0". Valid parallel output data can only be latched at the end of the sample/conversion cycle.

The LSB bit is valid 20nsec prior to the falling edge of Status (E.O.C.), therefore, this edge may be used to latch parallel output data. While

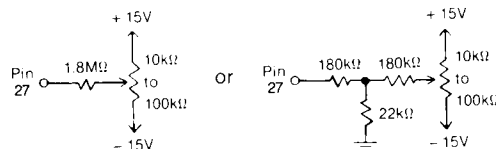
the converter is idling (Status is "0"), the parallel output data from the most recent conversion remains valid until the start of the next conversion cycle.

SERIAL OUTPUT—Serial output data is provided only during the conversion process and is in a NRZ (non-return-to-zero) format. The data is coded the same as parallel output data and is synchronous with the internal clock. Each serial output bit is valid 20nsec after the rising clock edge (serial output data lags parallel output by one clock cycle, see timing diagram) and can be strobed into a shift register by rising edges of the internal clock.

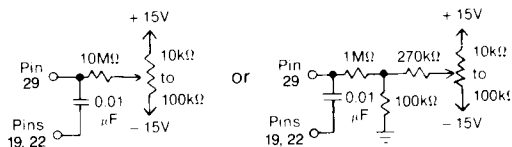
OPTIONAL EXTERNAL ZERO AND GAIN ADJUSTMENTS—Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the following diagrams. Adjustments should be made following warmup, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be $\pm 20\%$ carbon composition or better. Multiturn potentiometers with TCR's of 100ppm/ $^{\circ}\text{C}$ or less are recommended to minimize drift with temperature. If these adjustments are not used, Offset Adjust (pin 27) should be left open and a 0.01 μ F capacitor should be connected from Gain Adjust (pin 29) to Ground.

ZERO ADJUSTMENT—Connect the zero adjust potentiometer as shown below. For unipolar (MN6295 only), apply the input voltage at which the 0000 0000 0000 0000 to 0000 0000 0000 0001 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "0" and the LSB "flickers" on and off.

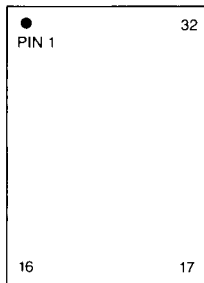
For bipolar ranges (MN6295 and MN6296), apply the input voltage at which the 0111 1111 1111 1111 to 1000 0000 0000 0000 transition is ideally supposed to occur. While continuously converting, adjust the zero potentiometer until all bits are "flickering."



GAIN ADJUSTMENT—Connect the gain potentiometer as shown below and apply the input voltage at which the 1111 1111 1111 1110 to 1111 1111 1111 1111 transition is ideally supposed to occur. While continuously converting, adjust the gain potentiometer until all the output bits are "1" and the LSB "flickers" on and off. A 0.01 μ F capacitor should be connected from Gain Adjust (pin 29) to Ground.



PIN DESIGNATIONS



- | | | | |
|----|--------------|----|---------------------------------|
| 1 | Bit 1 (MSB) | 32 | Short Cycle |
| 2 | Bit 2 | 31 | Start Convert |
| 3 | Bit 3 | 30 | +5V Supply (+Vdd) |
| 4 | Bit 4 | 29 | Gain Adjust |
| 5 | Bit 5 | 28 | +15V Supply (+Vcc) |
| 6 | Bit 6 | 27 | Offset Adjust |
| 7 | Bit 7 | 26 | Bipolar Offset |
| 8 | Bit 8 | 25 | 10V Input (MN6295; N.C. MN6296) |
| 9 | Bit 9 | 24 | 20V Input (MN6296; N.C. MN6295) |
| 10 | Bit 10 | 23 | Reference Output (+10V) |
| 11 | Bit 11 | 22 | Ground |
| 12 | Bit 12 | 21 | -15V Supply (-Vcc) |
| 13 | Bit 13 | 20 | Clock Output |
| 14 | Bit 14 | 19 | Ground |
| 15 | Bit 15 | 18 | Status |
| 16 | Bit 16 (LSB) | 17 | Serial Output |

DIGITAL OUTPUT CODING

Analog Input		Digital Output	
0 to -10V	±5V	±10V	
		MSB	LSB
0	+F.S.	0000 0000 0000 0000	
-1/2LSB	+F.S. - 1/2LSB	0000 0000 0000 0000 [†]	
-1/2 F.S. + 3/2LSB	+3/2LSB	0111 1111 1111 1111 [†]	
-1/2 F.S. + 1/2LSB	+1/2LSB	$\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi\phi$	
-1/2 F.S. - 1/2LSB	-1/2LSB	1000 0000 0000 0000 [†]	
-1/2 F.S. + 3/2LSB	-F.S. + 3/2LSB	1111 1111 1111 1111 [†]	
-F.S.	-F.S.	1111 1111 1111 1111	

CODING NOTES:

- For 10 Volts FSR, 1LSB for 16 Bits=152.6 μ V. 1LSB for 14 Bits=610.4 μ V.
- For 20 Volts FSR, 1LSB for 16 Bits=305.2 μ V. 1LSB for 14 Bits=1.22mV.
- For unipolar ranges, the coding is straight binary.
- For bipolar ranges, the coding is offset binary.

*Analog voltages listed are the theoretical values for the transitions indicated. Ideally, with the MN6295/MN6296 continuously converting, the output bits indicated as ϕ will change from a "1" to a "0" or vice versa as the input voltage passes through the level indicated.

INPUT RANGE SELECTION

Part Number	Range	Connect Pin 26 to Pin
6295	0 to -10V	Ground
6295	±5V	23
6296	±10V	23

EXAMPLE: For the ±10V range, the transition from output code 0000 0000 0000 0000 to output code 0000 0000 0000 0001 (or vice versa) will ideally occur at an input of +9.999847V (+F.S. - 1/2LSB). Subsequently, any voltage greater than +9.999847V will give a digital output of all "0's." The transition from digital output 0111 1111 1111 1111 to 1000 0000 0000 0000 (or vice versa) will ideally occur at an input of +0.000153 volts. The 1111 1111 1111 1110 to 1111 1111 1111 1111 transition will occur at -9.999542V. An input more negative than this level will give all "1's."

ORDERING INFORMATION

Part Number	Input Voltage Range		Specified Temperature Range	No Missing Codes	Integral Linearity (3)	Minimum Sampling Rate	Minimum Input Bandwidth	SNR	Harmonics
	Unipolar	Bipolar							
MN6295J	0 to -10V	±5V	0°C to +70°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	-85dB
MN6295K	0 to -10V	±5V	0°C to +70°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	-88dB
MN6295S	0 to -10V	±5V	-55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	-85dB
MN6295S/B (1)	0 to -10V	±5V	-55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	-85dB
MN6295S/B CH(2)	0 to -10V	±5V	-55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	-85dB
MN6295T	0 to -10V	±5V	-55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	-88dB
MN6295T/B (1)	0 to -10V	±5V	-55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	-88dB
MN6295T/B CH(2)	0 to -10V	±5V	-55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	-88dB
MN6296J	N.A.	±10V	0°C to +70°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	-85dB
MN6296K	N.A.	±10V	0°C to +70°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	-88dB
MN6296S	N.A.	±10V	-55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	-85dB
MN6296S/B (1)	N.A.	±10V	-55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	-85dB
MN6296S/B CH(2)	N.A.	±10V	-55°C to +125°C	13 Bits	±0.006%FSR	50kHz	25kHz	80dB	-85dB
MN6296T	N.A.	±10V	-55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	-88dB
MN6296T/B (1)	N.A.	±10V	-55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	-88dB
MN6296T/B CH(2)	N.A.	±10V	-55°C to +125°C	14 Bits	±0.003%FSR	50kHz	25kHz	84dB	-88dB

Notes:

- Includes Environmental Stress Screening.
- Contact factory for availability of CH device types.
- ±0.006%FSR is equivalent to ±1/2LSB for 13 bits.
±0.003%FSR is equivalent to ±1/2LSB for 14 bits.

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