NWK938

155 Mb/s ATM TWISTED PAIR PHY/PMD TRANSCEIVER DEVICE WITH CLOCK RECOVERY

The NWK938 is a Physical Medium Dependent device designed to operate at 155 Mb/s over category 5 unshielded or shielded twisted pair cable using the ATM Forum specification for 155.52Mb/s SONET/SDH communication. The chip interfaces to a Transmission Convergence (TC) sublayer chip via a serial link.

FEATURES

- Complies with ATM Forum specification for 155Mb/s over Twisted Pair Cable
- Serial Interface to Transmission Convergence Sublayer
- Operates over 100 Meters of Category 5 UTP or STP Cable
- Quantized Feedback Circuit to Overcome 'Baseline Wander'
- Adaptive Equalization
- Clock Multiplier to 155.52MHz from 19.44MHz reference
- 155.52MHz Receive Clock Recovery PLL
- Clock Recovery PLL also suitable for Optical Module
- Programmable TX output current
- Single +5 V Supply
- 44 Lead Plastic Thin Quad Flat Pack

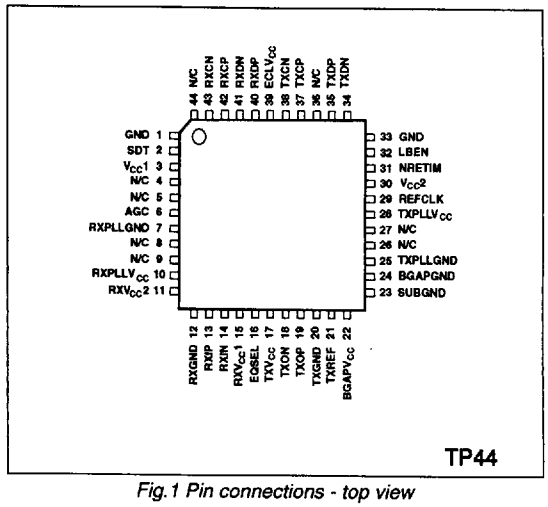


Fig.1 Pin connections - top view

ORDERING INFORMATION

NWK938/CG/TP1N

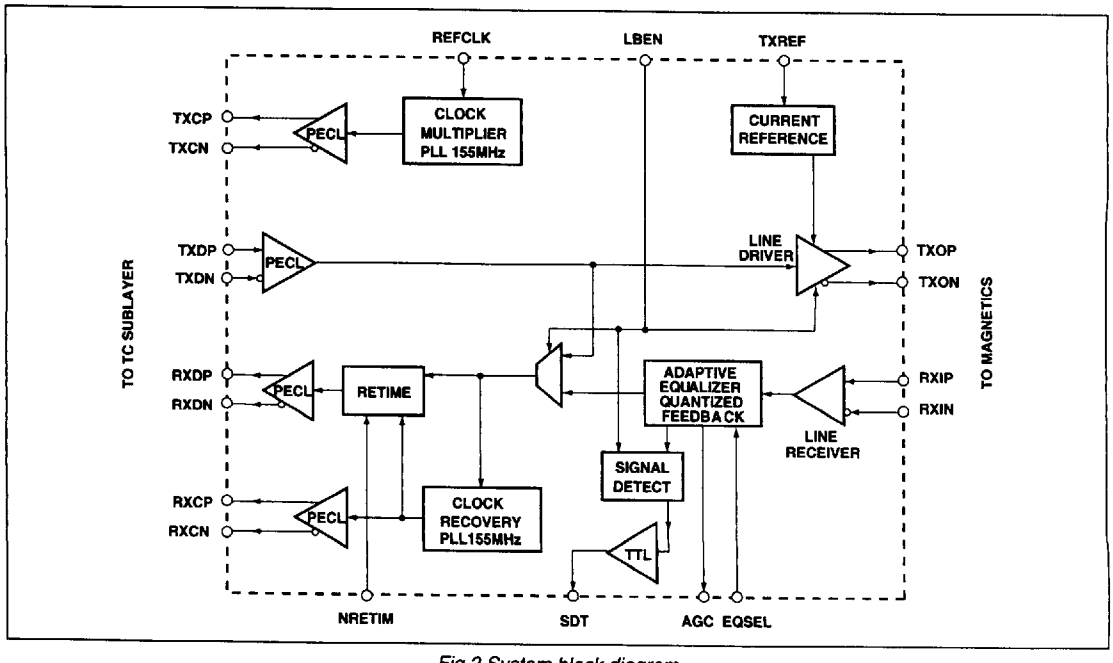


Fig.2 System block diagram

ABSOLUTE MAXIMUM RATINGS

Operation at absolute max. ratings is not implied. Exposure to stresses outside those listed could cause permanent damage to the device.

DC Supply voltage (V_{CC})	–0.5 to +7V
Storage temperature (tst)	–65 to +150°C
ESD	2kV HBM

RECOMMENDED OPERATING CONDITIONS

DC supply voltages (V_{CC})	+5V ±5%
Operating temperature (T_A)	0°C to +70°C (+25°C typ.)
Power dissipation (P_D)	700mW (typ.)

ELECTRICAL CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
DC characteristics						
Total V_{CC} supply current	I_{CC}	-	100	-	mA	no PECL loads
TTL high level I/P voltage	V_{IH}	2	-	-	V	
TTL low level I/P voltage	V_{IL}	-	-	0.8	V	
TTL high level I/P current	I_{IH}	-	-	20	µA	$V_{IH} = V_{CC}$
TTL low level I/P current	I_{IL}	-	-	–400	µA	$V_{IL} = 0.4V$
EQSEL high level I/P voltage	V_{IH}	4.2	-	-	V	
EQSEL low level I/P voltage	V_{IL}	-	-	0.8	V	
EQSEL floating level I/P	V_{IZ}	-	$V_{CC}/2$	-	V	
EQSEL high level I/P current	I_{IH}	-	-	1400	µA	V_{IH}
EQSEL low level I/P current	I_{IL}	-	-	–1400	µA	$V_{IL} = 0V$
PECL high level I/P voltage		3.8	-	V_{CC}-0.5	V	
PECL low level I/P voltage		-	-	3.6	V	
PECL high level input current	I_{IH}	-	-	20	µA	$V_{IH} = V_{CC}–0.5V$
PECL low level input current	I_{IL}	-	-	20	µA	$V_{IL} = V_{CC}–1.4V$
PECL high level O/P voltage		-	$V_{CC}–0.9$	-	V	50Ω load to V_{CC} –2V
PECL low level O/P voltage		-	$V_{CC}–1.75$	3.5	V	50Ω load to V_{CC} –2V
TTL high level O/P voltage	V_{OH}	2.4	-	-	V	$I_{OH} = –200µA$
TTL low level O/P voltage	V_{OL}	-	-	0.5	V	$I_{OL} = 4mA$
TTL high level O/P current	I_{OH}	-	-	–200	µA	
TTL low level O/P current	I_{OL}	-	-	4	mA	
Transmit O/P current pins TXOP, TXON		-	20	-	mA	$R_{REF} = 1.3k\Omega$
Differential RX I/P signal voltage		-	0.7	-	Vp-p	measured on device pins 155Mb/s data, 0mCable
RX I/P common mode voltage		-	$V_{CC}/2$	-	V	RX I/Ps floating
RX I/P impedance		-	24	-	kΩ	
Signal detect threshold	V_{TH}	-	50	-	%	wrt normalized output of equalizer
Low voltage shutdown		-	3.8	-	V	
AC characteristics						
155Mb/s TX driver outputs rise/fall times pins TXOP, TXON		-	2.5	-	ns	50Ω load
PLL characteristics						
3dB bandwidth		-	50	-	kHz	
Damping factor		-	2	-		
Peaking		-	-	.005	dB	
Overshoot		-	-	5	%	
Static error		-	±0.5	-	ns	
Jitter		-	-	0.5	ns	
VCO characteristics						
Centre frequency		-	155	-	MHz	
Deviation		-	±40	-	MHz	
Gain @155MHz		-	70	-	MHz/V	

FUNCTIONAL DESCRIPTION

The NWK938 shall, in conjunction with a Transmission Convergence sublayer chip and suitable magnetics, provide the PHY layer for 155Mb/s ATM. The NWK938 provides the necessary interfacing, transmit clock multiplier, transmit driver, line receiver, equalization, quantized feedback circuit and clock recovery.

The functional blocks within the device are shown in Fig. 2. These are described below:-

Transmit Section

Times Eight Clock Multiplier 19.44MHz to 155MHz

This circuit consists of a phase lock loop (PLL) that is operating at 155MHz, centre frequency. The 155MHz is divided by 8 to produce a 19.44MHz clock which is phase compared with a 19.44MHz crystal clock reference frequency which is input on pin REFCLK. On chip components set the VCO characteristics of loop damping factor (ξ), 3db bandwidth and centre frequency (ωn).

A control current is derived from the clock multiplier and is used by the receive clock recovery circuit to centre the PLL when no input data is present.

Transmit Line Driver

Serial data is input in NRZ format on pins TXDP and TXDN and output on the line driver pins TXOP and TXON. The driver consists of differential current source outputs with programmable sink capability, designed to drive a nominal output impedance of 50Ω.

Output current is set by the value of an external resistor (R_{REF}) between pin TXREF and TXGND.

This resistor defines an internal reference current derived from an on-chip bandgap reference.

Final output current at the TXO outputs is a multiple of this current and is defined as:-

$$I_{TXO}(mA) = 26/R_{REF}(k\Omega)$$

Transition times of the TXO outputs are matched and internally limited to approx. 2.5ns to reduce EMI emissions.

Equalizer

The equalizer circuit is necessary to compensate for signal degradation due to cable losses, however over-equalization must be avoided to prevent excessive overshoots resulting in errors during the reception of data. Three operating modes are therefore provided.

These three operating modes are controlled by the state of tristate input EQSEL and are described below:-

1) Auto Equalization (EQSEL floating)

Fully automatic equalization is achieved through the use of a feedback loop driven by a control signal derived from the signal amplitude. This provides adaptive control and prevents over-modulation of the signal when short cable lengths are used.

2) Full Equalization (EQSEL low)

In this mode, full equalization is applied to the input signal irrespective of amplitude.

3) No Equalization (EQSEL high)

The equalization circuit is disabled completely during this mode.

Quantized Feedback

The low frequency components present in the transmitted waveform are attenuated by the transformers which are present at the transmitter and receiver. This can result in "Baseline Wander" which reduces the noise immunity and increases the error rate.

The NWK938 restores those low frequency components to the received signal using a Quantized Feedback circuit.

Signal Detector

A signal detect circuit is provided which continuously monitors the amplitude of the input signal being received on pins RXIP and RXIN. After the input signal reaches a level which the equalizer can correctly equalize, SDT is asserted high. Conversely if the signal level falls below a limit for reliable operation then SDT will go low.

PLL Clock Recovery

This function consists of a 155MHz PLL that is locked to the incoming data stream. The PLL is first centred to the transmit clock multiplier using an internal analog reference signal. Once an input signal is present the loop will lock to, and thus extract the clock from, the incoming data stream. On chip components set the VCO characteristics of loop damping factor (ξ), 3db bandwidth and centre frequency (ωn)

Receive Data Retiming

Pin NRETIM controls the timing of the received data. A high level on this pin allows the received data to pass directly to the RXDP and RXDN pins. A low level retimes the data using the recovered clock RXC.

Loopback Logic and Optical Receive Clock Recovery

Pin LBEN controls loopback operation. A low level on this pin defines normal operation, a high level defines loopback mode. In loopback mode, the transmit data is internally routed to the receive circuitry, SDT is forced high and the TXOP and TXON outputs are disabled.

In this mode received data from an optical module can be presented to pins TXDP and TXDN and the clock recovery PLL will recover the clock.

AC CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Waveform Timing	Value Min.	Value Typ.	Value Max.	Units	Conditions
AC characteristics						
155Mb/s TX driver outputs rise/fall times pins TXOP, TXON		-	2.5	-	ns	100Ω differential load measured at RJ45
REFCLK frequency	1	-	19.44	-	MHz	
REFCLK tolerance	2	-	100	-	ppm	
REFCLK M/S ratio	3	40:60	-	60:40	%	
RXD valid to RXC +Ve edge	4	3	-	-	ns	
RXC to RXD invalid	5	1	-	-	ns	
REFCLK to SDT transition	-	3	-	10	ns	

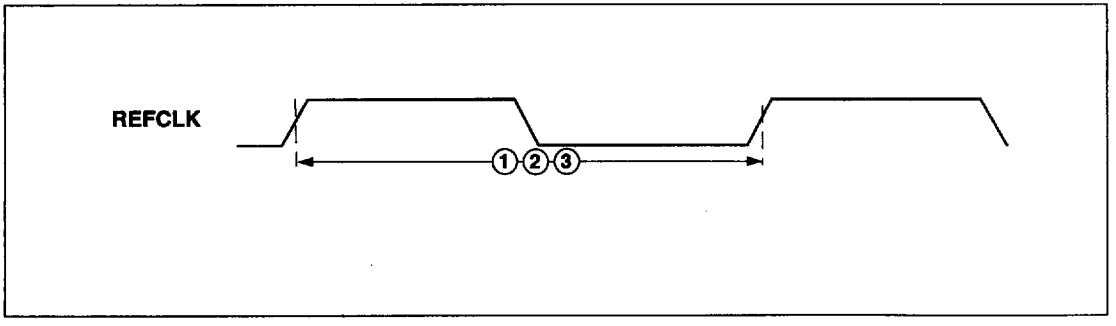


Fig.3 Transmit timing waveform

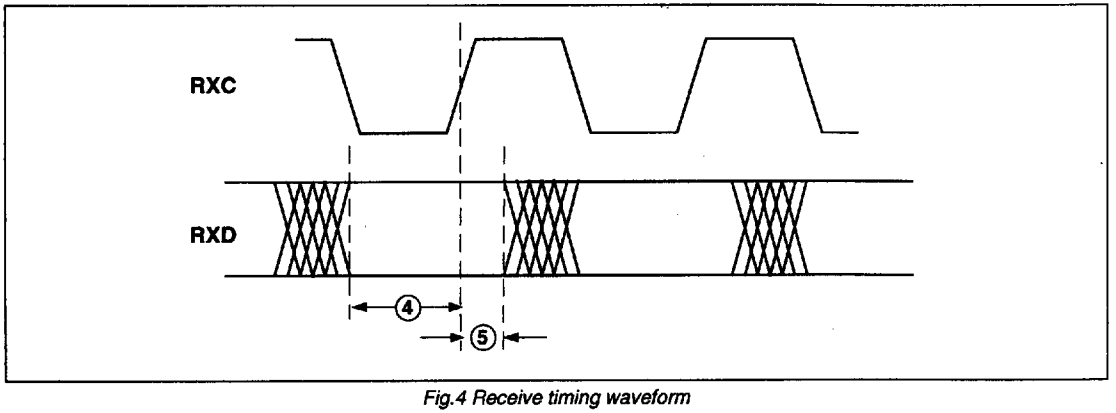


Fig.4 Receive timing waveform

GLOSSARY OF TERMS AND ABREVIATIONS

UTP	Unshielded Twisted Pair
STP	Shielded Twisted Pair
NRZ	Non Return To Zero
PHY	PHYsical Layer
PECL	Pseudo ECL
PMD	Physical Media Dependent

PIN DESCRIPTIONS

Pin	Pin Name	Pin Type	Description
1	GND	power	0V supply to TTL and PECL I/O
2	SDT	TTLOP	Signal detect output. This output is high when an input signal of sufficient amplitude is available on the RXIP and RXIN inputs.
3	$V_{CC}1$	power	+5V supply receive logic
6	AGC	analog	Receiver AGC output (test purposes only)
7	RXPLLGND	power	0V supply to receive PLL
10	$RXPLLV_{CC}$	power	+5V supply to receive PLL
11	$RXV_{CC}2$	power	+5V supply to adaptive equalizer and QFB circuits
12	RXGND	power	0V supply to adaptive equalizer and QFB circuits
13	RXIP	analog	Differential receive signal input from magnetics
14	RXIN	analog	
15	$RXV_{CC}1$	power	+5V supply to slicer
16	EQSEL	3 level IP	Mode select input for equalizer, high = min, open circuit = auto, low = full
17	TXV_{CC}	power	+5V supply to transmit line driver circuits
18	TXON	analog outputs	Differential line driver outputs to drive magnetics
19	TXOP		
20	TXGND	power	0V supply to transmit line driver circuits
21	TXREF	analog	Line driver current reference set-up pin. The current is set by connecting a resistor to the TXGND pin.
22	$BGAPV_{CC}$	power	+5V supply to on-chip bandgap reference
23	SUBGND	power	Chip substrate GND connection
24	BGAPGND	power	0V to on-chip bandgap reference
25	TXPLLGND	power	0V to transmit clock multplier PLL
28	$TXPLLV_{CC}$	power	+5V supply to transmit clock multplier PLL
29	REFCLK	TTLIP	19.44MHz reference clock to PLL's
30	$V_{CC}2$	power	+5V supply to transmit logic
31	NRETIM	TTLIP	Receive data retiming control. A low on this pin selects retimed mode, a high selects non-retimed.
32	LBEN	TTLIP	Loopback enable input. A high on this pin selects loopback mode and a low selects normal operation.
33	GND	power	0V to TTL and PECL I/O
34	TXDN	PECLIP	Differential serial data inputs to transmit channel
35	TXDP	PECLIP	
37	TXCP	PECLOP	Differential 155MHz transmitter clock
38	TXCN	PECLOP	
39	$ECLV_{CC}$	power	+5V supply to PECL I/O
40	RXDP	PECLOP	Differential 155Mb/s serial received data
41	RXDN	PECLOP	
42	RXCP	PECLOP	Differential 155MHz recovered clock aligned to the RXDP & RXDN data outputs
43	RXCN	PECLOP	
4,5,8, 9,26,27, 36,44	N/C	-	No connect. No external connection should be made to these pins.

Table 1: Pin descriptions

EXTERNAL REQUIREMENTS

The NWK938 requires a number of external components for the device to function correctly and these are shown in the simplified system block diagram, Fig.5.

Careful attention should be paid to the layout of the high speed PECL interface to the TC sublayer, with the lines short, matched, ideally with the correct impedance and suitably terminated. Similar attention should be paid to the connections to the magnetics and from there to the RJ45. The transmit and receive paths should be kept seperate to minimise coupling, with the receiver path having precedence in the case of a trade-off. The receiver padder network -R7,R8,R9 should be placed as close to the NWK938 pins as possible.

POWER SUPPLY CONNECTIONS

When connecting the various power supplies to the NWK938 it is important to reduce noise coupling between circuits. Fig.6 shows the way in which the individual pins are recommended to be decoupled and interconnected.

An example layout is shown in Fig.7, which uses a solid ground plane and a V_{CC} plane divided into digital, transmit and receive portions. The close connection of decoupling components to device pins is demonstrated.

It is also recommended that the ground plane be split to provide a chassis ground with the RJ45 connector isolated from the main board ground. There should also be a void underneath the magnetics. A simple example is shown in Fig.8.

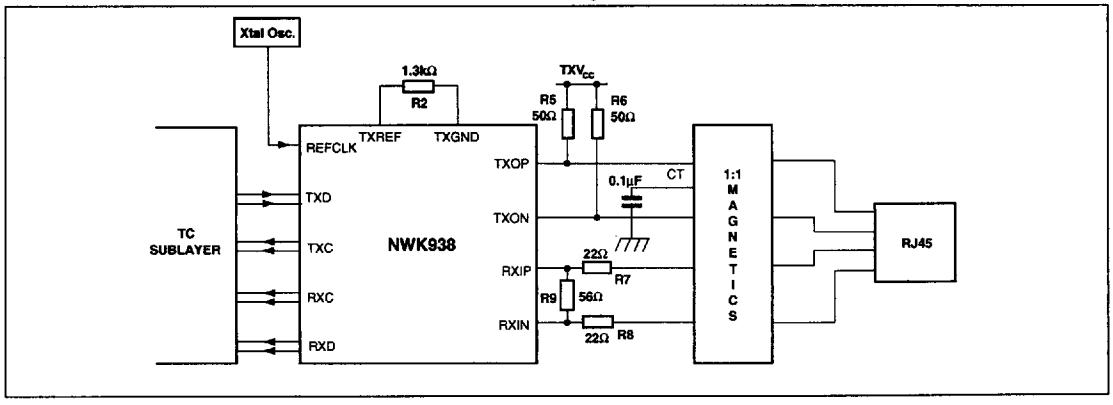


Fig.5 Simplified system block diagram showing NWK938 external components

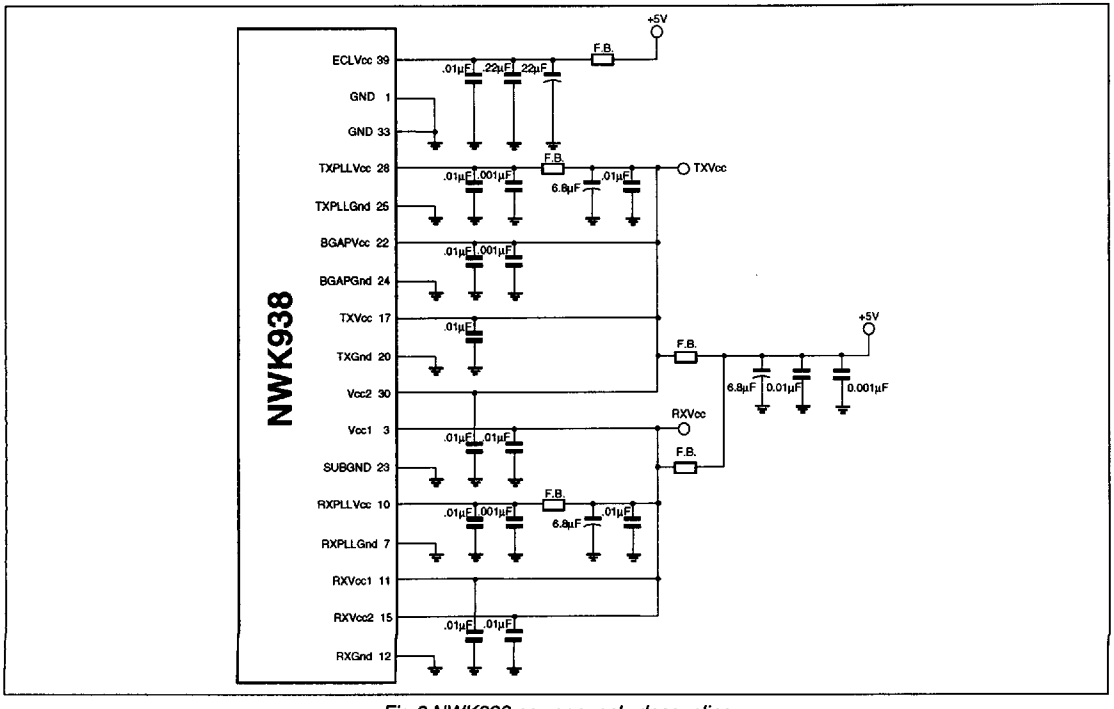


Fig.6 NWK938 power supply decoupling

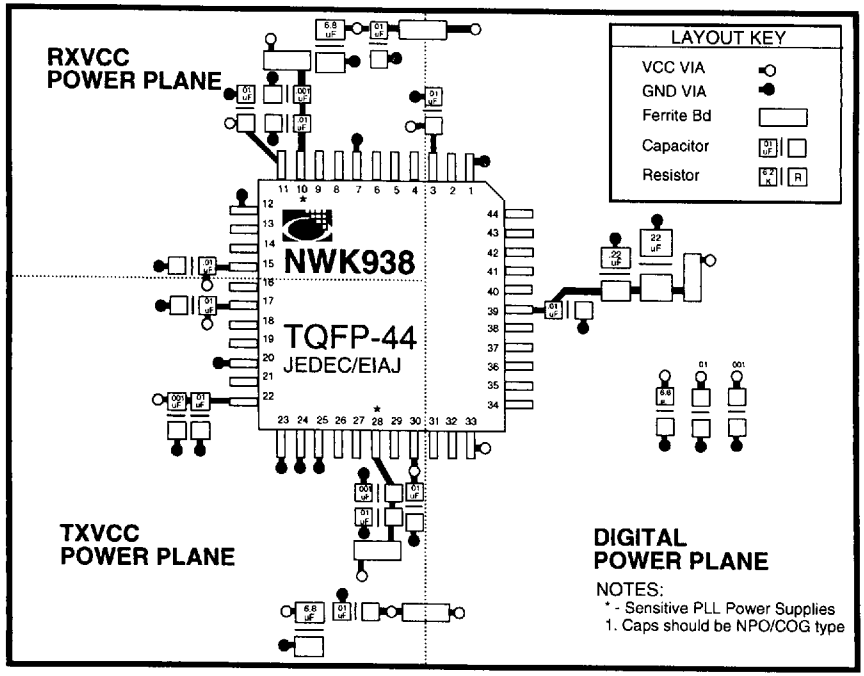


Fig.7 Power plane arrangement and supply decoupling

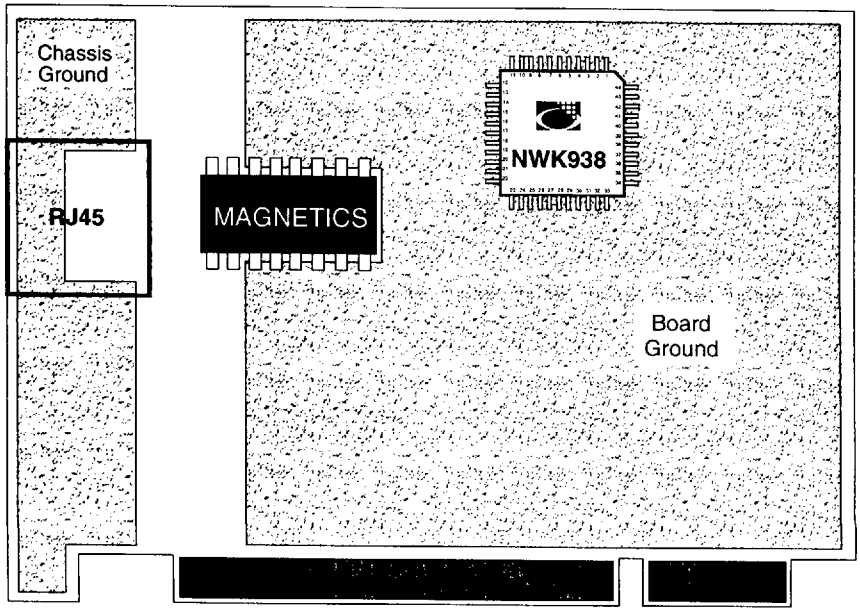
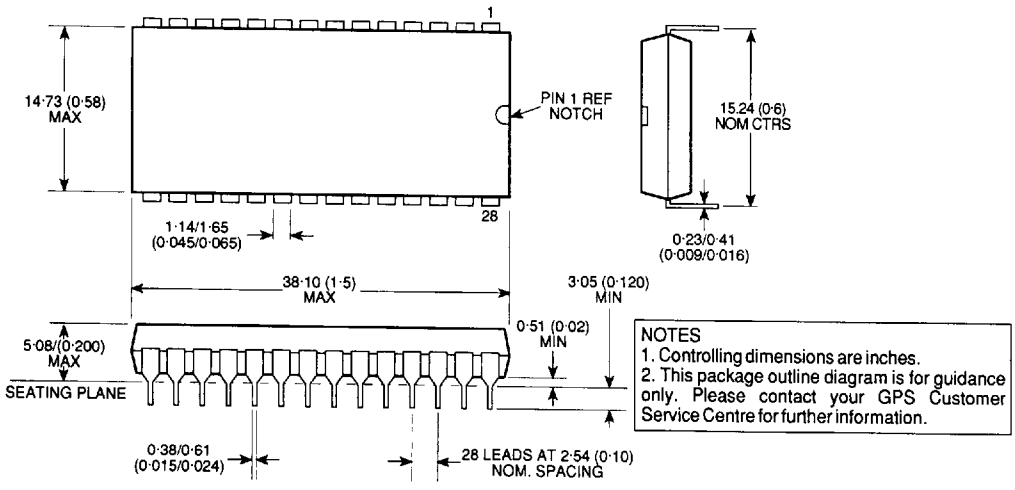
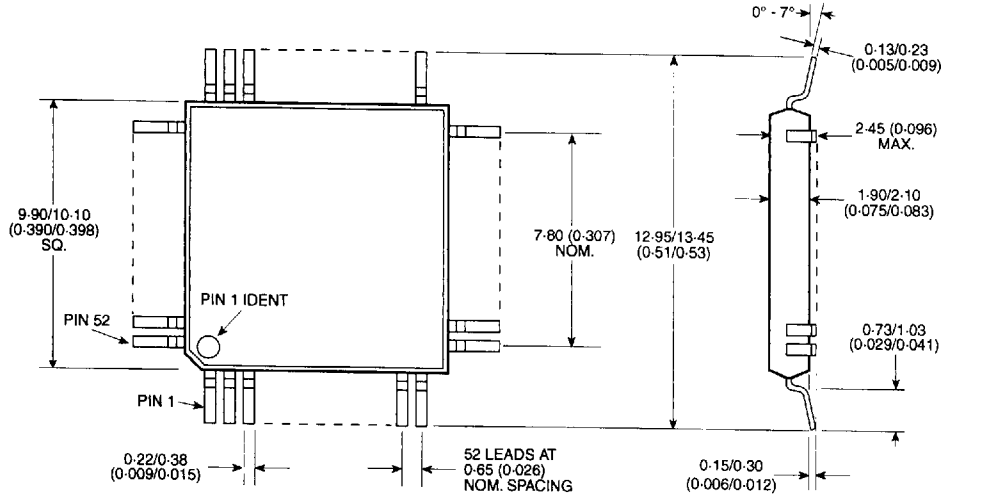


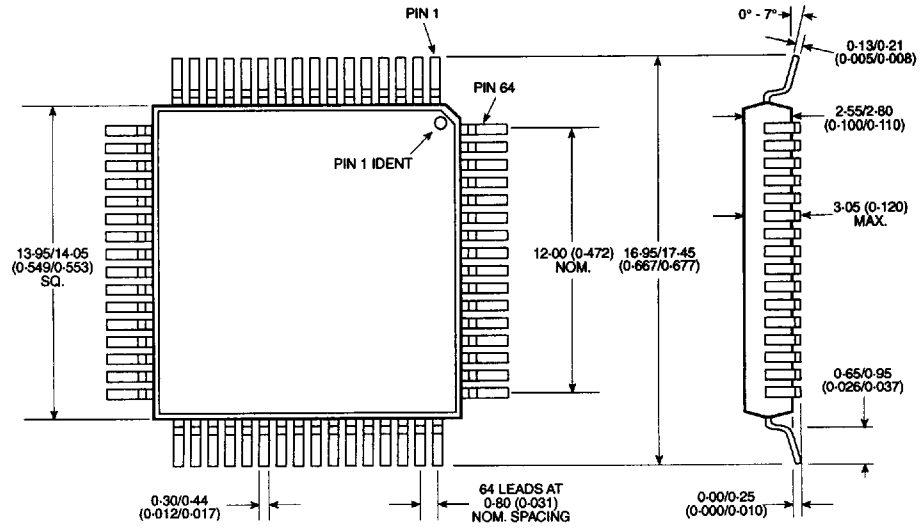
Fig.8 Ground plane management



28-LEAD PLASTIC DIL – DP28

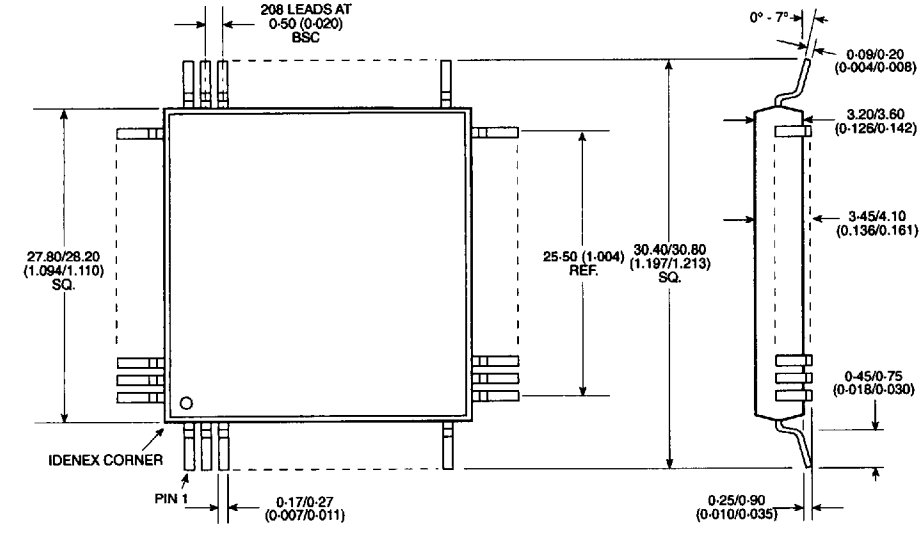


52-LEAD QUAD FLATPACK – GP52



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

64-LEAD PLASTIC QUAD FLATPACK – GP64



NOTES
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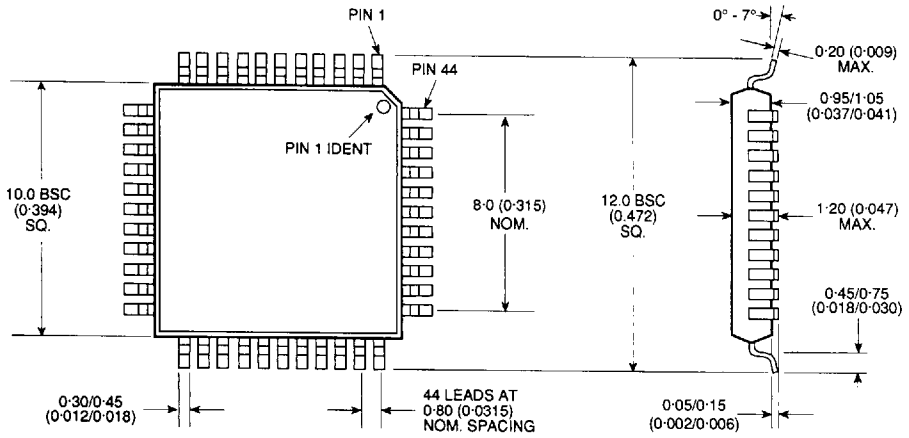
208-LEAD PLASTIC QUAD FLATPACK – GP208



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

44-LEAD THIN PLASTIC QUAD FLATPACK – TP44