Micro Linear

ML2341, ML2351

Single Supply Programmable 8-Bit D/A Converters

GENERAL DESCRIPTION

The ML2341 and ML2351 are CMOS voltage output, 8 bit D/A converters with an internal voltage reference and a µP interface. These devices are designed to be powered by a single supply, but they can also be powered from dual supplies. The output voltage swings above zero scale (V_{ZS}) in the unipolar mode or around zero scale in the bipolar mode, in both cases with programmable gain. V_{ZS} can be set to any voltage from AGND to 2.25V below V_{CC}. The digital and analog grounds, DGND and AGND, are totally independent of each other. DGND can be set to any voltage from AGND to 4.5V below V_{CC} for easy interfacing to standard TTL and CMOS logic families.

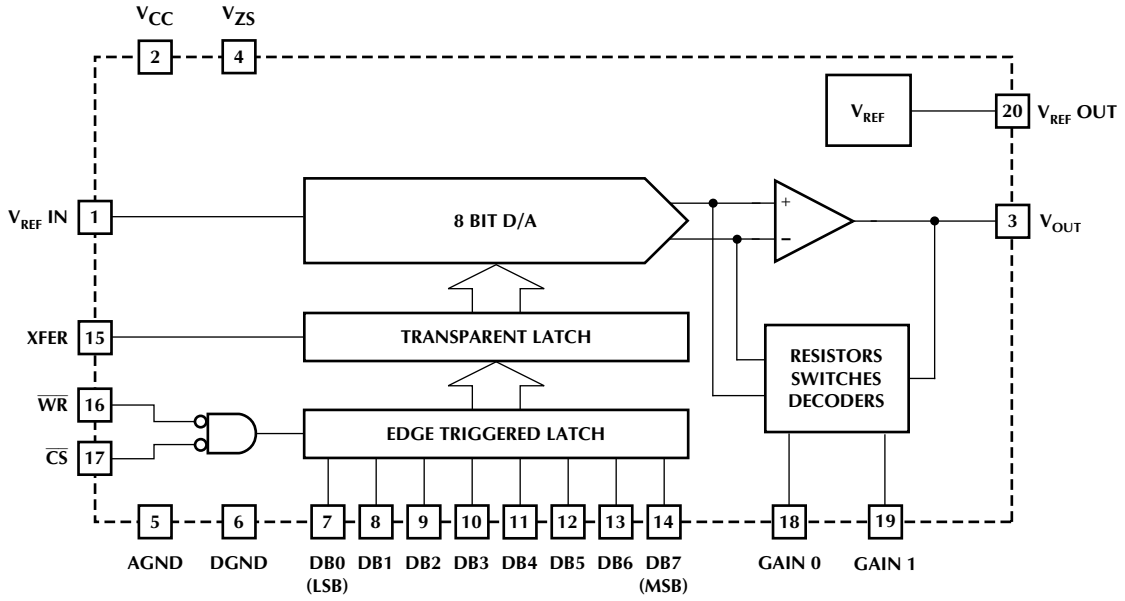
The high level of integration and versatility of the ML2341 and ML2351 makes them ideal for a wide range of applications in hard disk drives, automotive, telecom, and a variety of general purpose industrial uses.

The ML2341 provides a 2.25V or 4.5V reference output for use with A/D converters that use a single 5V ±10% power supply, while the ML2351 provides a 2.5V or 5V reference output.

FEATURES

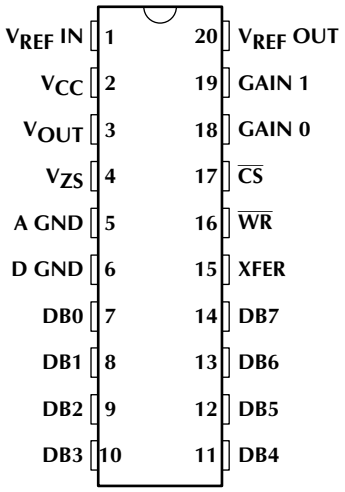
- Programmable output voltage gain settings of 2, 1, 1/2, 1/4, provide 8, 9, 10, or 11 bit effective resolution around zero
- AGND to V_{CC} output voltage swing
- Bipolar or unipolar output voltage
- 4.5V to 13.2V single or ±2.25V to ±6.5V dual supply operation
- Single- and double-buffered, edge-triggered interface with 30ns write time, 0ns hold time
- Voltage reference output (ML2341 - 2.25V or 4.5V, (ML2351 - 2.5V or 5V)
- Nonlinearity ±1/4LSB or ±1/2LSB
- Output voltage settling time guaranteed over temperature and supply voltage tolerance (within 1V of V_{CC} and AGND - 2.5µs max., within 100mV of V_{CC} and AGND - 5µs max.)
- TTL and CMOS compatible digital inputs
- Low supply current ($V_{REF} \leq 2.5V$ - 5mA max.)

BLOCK DIAGRAM



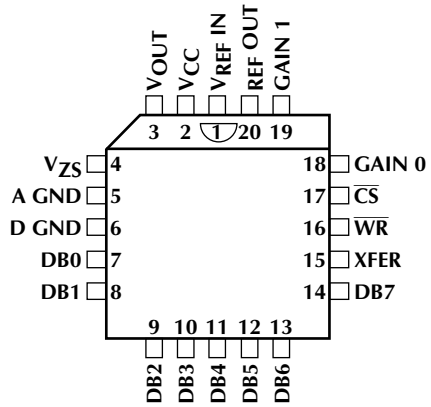
PIN CONFIGURATION

ML2341
ML2351
20-Pin PDIP (P20)
20-Pin SOIC (S20)



TOP VIEW

ML2341
ML2351
20-Pin PLCC (Q20)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{REF} IN	Voltage reference input. V_{REF} IN IS referenced to AGND.
2	V_{CC}	Positive supply.
3	V_{OUT}	Voltage output of the D/A converter. V_{OUT} is referenced to V_{ZS}.
4	V_{ZS}	Zero Scale Voltage. V_{OUT} is referenced to V_{ZS}. V_{ZS}s is normally tied to A GND in the unipolar mode or to mid-supply in the bipolar mode.
5	A GND	Analog ground.
6	D GND	Digital ground. This is the ground reference level for all digital inputs. D GND is normally tied to system ground, but can range from A GND τo (V_{CC} - 4.5V).
7	DB0	Data input — Bit 0 (LSB).
8	DB1	Data input — Bit 1.
9	DB2	Data input — Bit 2.
10	DB3	Data input — Bit 3.
11	DB4	Data input — Bit 4.
12	DB5	Data input — Bit 5.
13	DB6	Data input — Bit 6.
14	DB7	Data input — Bit 7 (MSB).
15	XFER	Transfer enable input. In the double buffered mode of operation, the data in the input latch is transferred to the D/A converter during the high level of XFER.
16	$\overline{WR}$	Write enable input. While $\overline{CS}$ is low data inputs are latched into the input latch on the rising edge of $\overline{WR}$.
17	$\overline{CS}$	Chip select input. Active low input which enables the data to be latched on the rising edge of $\overline{WR}$.
18	GAIN 0	Digital gain setting input 0.
19	GAIN 1	Digital gain setting input 1.
20	V_{REF} OUT	Voltage reference output. V_{REF} OUT is referenced to A GND. V_{REF} OUT is set to 2.25V during low-voltage operation and 4.5V during high-voltage operation for the ML2341. The voltage settings are 2.5V and 5V for the ML2351.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} with respect to A GND 14.2V
D GND ..... A GND - 0.3V to V_{CC} + 0.3V
V_{ZS}, V_{REF} IN ..... A GND - 0.3V to V_{CC} + 0.3V
Logic Inputs ..... A GND - 0.3V to V_{CC} + 0.3V
Input Current, per Pin ..... ±25mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Thermal Resistance (θ_{JA})
20-Pin PDIP ..... 67°C/W
20-Pin PLCC ..... 78°C/W
20-Pin SOIC ..... 95°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
V_{CC} Supply Range
-5 Suffix ..... 4.5V to 5.5V
-12 Suffix ..... 10.8V to 13.2V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} - A GND = 5V ± 10% (-5 Suffix) or 12V ± 10% (-12 Suffix), V_{REF} IN = 2.25V or 4.5V (ML2341) or V_{REF} IN = 2.5V or 5V (ML2351), R_L = R(V_{REF} OUT) = 1kΩ, C_L = C(V_{REF} OUT) = 100pF, $t_R = t_F \leq 20$ns, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CONVERTER AND PROGRAMMABLE GAIN AMPLIFIER							
	Resolution			8			bits
	Integral Linearity Error		B Suffix			±1/4	LSB
			C Suffix			±1/2	LSB
	Differential Linearity Error		B Suffix			±1/2	LSB
			C Suffix			±1/4	LSB
	V_{ZS} Unipolar Mode Threshold			0		1	V
	V_{ZS} Bipolar Mode Threshold			1.5		V_{CC} - 2.25	V
	Unipolar Mode Offset Error	See Figure 1	Gain = 1/4, 1/2, 1			10	mV
			Gain = 2			20	mV
	Bipolar Mode Offset Error	See Figure 1				±10 + 21/2 LSB	mV
	Unipolar Mode Gain Error	See Figure 1			±0.5	±2	%FS
	Bipolar Mode Gain Error	See Figure 1			±0.5	±2	%FS
REFERENCE							
V_{REF} OUT	Reference Output Voltage	ML2341BCX-5, V_{CC} = 5V	T_A = 25°C	2.23	2.25	2.27	V
			T_A = 0°C to 70°C	2.22	2.25	2.28	V
		ML2341CCX-5, V_{CC} = 5V	T_A = 25°C	2.22	2.25	2.28	V
			T_A = 0°C to 70°C	2.20	2.25	2.30	V
		ML2341BCX-12, V_{CC} = 12V	T_A = 25°C	4.48	4.50	4.52	V
			T_A = 0°C to 70°C	4.46	4.50	4.54	V
		ML2341CCX-12, V_{CC} = 12V	T_A = 25°C	4.45	4.50	4.55	V
			T_A = 0°C to 70°C	4.40	4.50	4.60	V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE (Continued)							
V_{REF} OUT	Reference Output Voltage	ML2351BCX-5,	T_A = 25°C	2.48	2.50	2.52	V
		V_{CC} = 5V	T_A = 0°C to 70°C	2.47	2.50	2.53	V
		ML2351CCX-5,	T_A = 25°C	2.45	2.50	2.55	V
		V_{CC} = 5V	T_A = 0°C to 70°C	2.44	2.50	2.58	V
		ML2351BCX-12,	T_A = 25°C	4.98	5.00	5.02	V
		V_{CC} = 12V	T_A = 0°C to 70°C	4.96	5.00	5.04	V
		ML2351CCX-12,	T_A = 25°C	4.95	5.00	5.05	V
		V_{CC} = 12V	T_A = 0°C to 70°C	4.90	5.00	5.10	V
	Temperature Coefficient				50		ppm/°C
	Output Current			0.75		5	mA
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$, 1kHz sine wave on V_{CC}		-40	-60		dB
V_{REF} IN AND V_{ZS}							
V_{REF} IN	Reference Input Voltage Range	$V_{CC} \leq 8.75V$		2		V_{CC}-1.75	V
		$V_{CC} \geq 8.75V$		2		7	V
	DC Input Resistance			10			MΩ
V_{ZS}	V_{ZS} Input Voltage Range	$V_{CC} \leq 7V$		0		V_{CC} - 2.25	V
		$V_{CC} \geq 8V$		0		V_{CC} - 3	V
LOGIC							
V_{INL}	Input Low Voltage					0.8	V
V_{INH}	Input High Voltage			2.0			V
I_{INL}	Input Low Current	V_{IN} = D GND				-1	µA
I_{INH}	Input High Current	$V_{IN} = V_{CC}$				1	µA
OUTPUT							
V_{OUT}	Output Voltage Swing	Unipolar Mode	R_L = 100kΩ	0.01		V_{CC} - 0.05	V
		(Note 2)	R_L = 1kΩ	1.0		V_{CC} - 1.0	V
		Bipolar Mode	R_L = 100kΩ	0.1		V_{CC} - 0.1	V
			R_L = 1kΩ	1.0		V_{CC} - 1.0	V
	Output Current	A GND + 1V < V_{OUT} < V_{CC} - 1V		-10		10	mA
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$, 1kHz sine wave on V_{CC}			-60		dB
AC PERFORMANCE							
t_{S1}	Settling Time 1	A GND + 1V → V_{CC} - 1V			1.2	2.5	µs
t_{S2}	Settling Time 2	A GND + 100mV → V_{CC} - 100mV, R_L = 100kΩ			2.5	5	µs
t_{S3}	Settling Time 3	Output Step of ±1 LSB				1	µs
t_{S4}	Settling Time, Change of any Gain Setting				1.1	2.5	µs
$t_{\overline{WR}}$	$\overline{WR}$ Pulse Width	See Figure 3		40			ns
t_{XFER}	XFER Pulse Width	See Figure 3		60			ns

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC PERFORMANCE (Continued)							
t_{XW}	Rising Edge of $\overline{WR}$ to Falling Edge of XFER	See Figure 3		30			ns
t_{DS}	Data Set-up Time, DB0 - DB7	See Figure 3		40			ns
t_{DH}	Data Hold Time, DB0 - DB7	See Figure 3		0			ns
$t_{\overline{CSS}}$	$\overline{CS}$ Set-up Time	See Figure 3		50			ns
$t_{\overline{CSH}}$	$\overline{CS}$ Hold Time	See Figure 3		0			ns
t_{RESET}	Power-on Reset Time					16	µs
SUPPLY							
I_{CC}	V_{CC} Supply Current (Note 3)	-5 Suffix	Unipolar Mode			6.0	mA
			Bipolar Mode			5.3	mA
		-12 Suffix	Unipolar Mode			11.0	mA
			Bipolar Mode			9.3	mA
$I_{A\ GND}$	Analog Ground Current (Note 3)	-5 Suffix	Unipolar Mode			-4.3	mA
			Bipolar Mode			-5.0	mA
		-12 Suffix	Unipolar Mode			-7.3	mA
			Bipolar Mode			-9.0	mA
$I(V_{ZS})$	V_{ZS} Current	-5 Suffix	Unipolar Mode			-1.7	mA
			Bipolar Mode		-90	-300	µA
		-12 Suffix	Unipolar Mode			-3.7	mA
			Bipolar Mode		-90	-300	µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: In unipolar operation with V_{ZS} and A GND tied together, digital codes that represent an analog value of less than 100mV from A GND should be avoided.

Note 3: Supply current and A GND Current are specified with the digital inputs stable and no load on V_{OUT}.

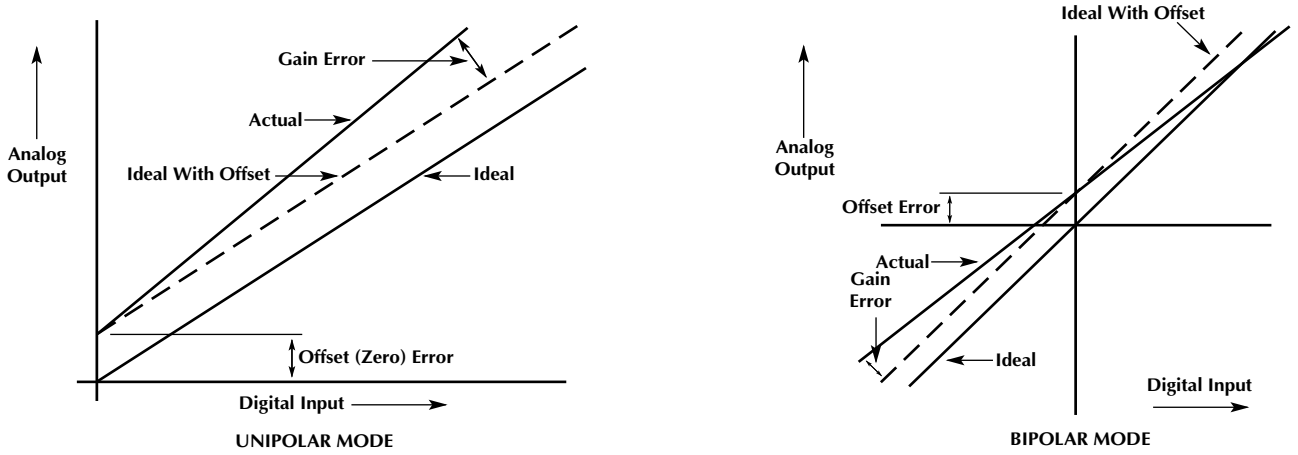


Figure 1. Gain and Offset Error

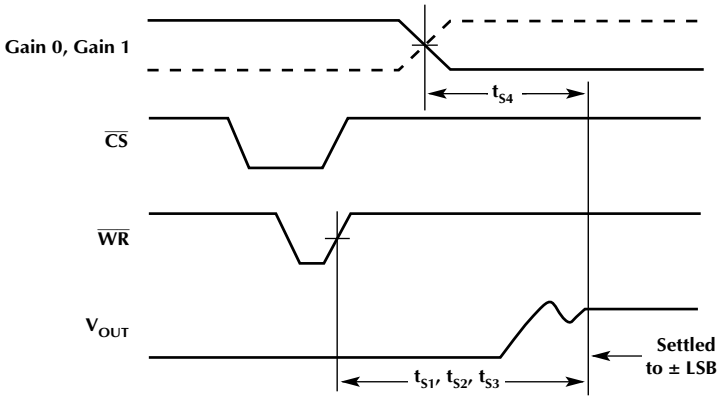


Figure 2. Settling Time

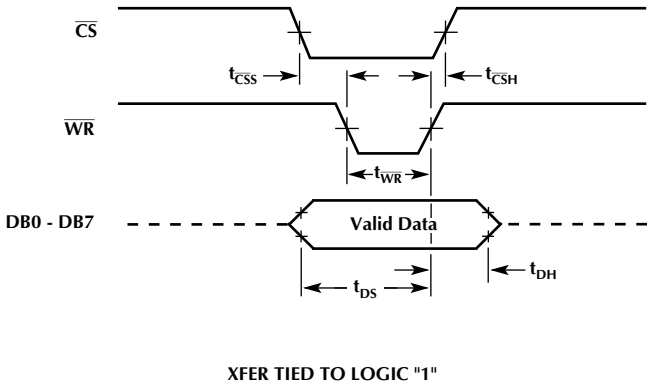


Figure 3a. Timing Diagram, Single Buffered Mode

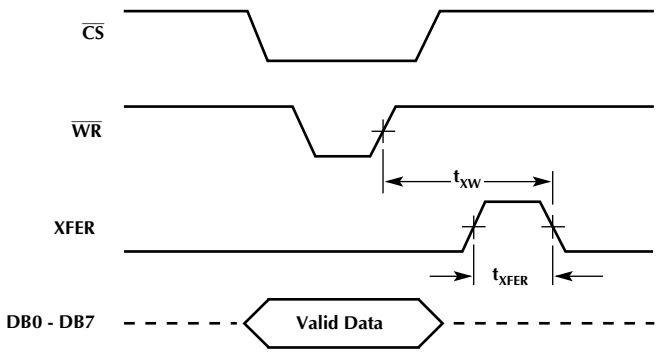


Figure 3b. Timing Diagram, Double Buffered Mode

FUNCTIONAL DESCRIPTION

D/A CONVERTER

The D/A converter is implemented using an array of equal current sources that are decoded semi-linearly for the four most significant bits to improve differential linearity and to reduce output glitch around major carries. A simplified block diagram is shown in Figure 4.

The input voltage reference of the D/A converter is the difference between $V_{REF\ IN}$ and A GND. This difference voltage is converted to a reference current using an internal resistor to set up the appropriate current level in the D/A converter. The D/A converter output current is then converted to a voltage output by an output buffer and a resistive network. The matching among the on-chip resistors preserves the gain accuracy between these conversions.

The D/A converter can be used in a multiplying mode by modulating the reference input within the specified V_{REF} IN range.

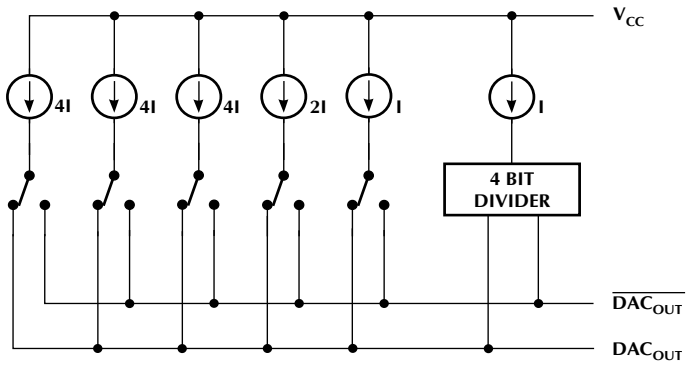


Figure 4. D/A Converter Implementation

SINGLE-SUPPLY vs. DUAL-SUPPLY OPERATION

Either the ML2341 or the ML2351 can be powered from a single supply with an output ranging from 4.5V to 13.2V, or dual supplies ranging from ±2.25V to ±6.6V.

The internal digital and analog circuitry is powered between V_{CC} and A GND. The range of D GND is AGND ≤ D GND ≤ (V_{CC} - 4.5V), with the logic thresholds set between 0.8V and 2.0V above D GND (standard TTL logic). The range of V_{ZS} is the same as that of D GND.

UNIPOLAR AND BIPOLAR OUTPUT VOLTAGE SWING

The ML2341 and ML2351 can operate in either unipolar or bipolar output voltage mode. Mode selection is determined by comparing the zero scale voltage (V_{ZS}) of these devices to a precise internal reference that is referred to A GND. V_{ZS} is ideally the voltage that will be produced at the DAC voltage output when the digital input data is set to all "0s". Unipolar mode is selected when V_{ZS} < 1V, and bipolar mode is selected when V_{ZS} > 1.5V.

Unipolar Output Mode

In the Unipolar mode, V_{OUT} swings above V_{ZS}. Ideally the 00000000 code results in an output voltage of V_{ZS}, and the 11111111 code results in an output voltage of $V_{FS} \leftrightarrow {}^{255}/_{256}$, where V_{FS} is the full-scale voltage determined by V_{REF} IN and the gain setting.

Bipolar Output Mode

In the Bipolar mode, V_{OUT} swings around V_{ZS}. The input data is in two's-complement binary format. Ideally, the 00000000 code results in an output voltage of V_{ZS}; the 10000000 code results in an output voltage of $V_{ZS} - V_{FS}$; and the 01111111 code results in an output voltage of $V_{ZS} + (V_{FS} \leftrightarrow {}^{127}/_{128}$, where V_{FS} is the full scale output voltage determined by V_{REF} IN and the gain setting.

OUTPUT BUFFER AND GAIN SETTING

The output buffer converts the D/A output current to a voltage output using a resistive network with its gain setting determined by the GAIN 0 and GAIN 1 inputs. There are four gain settings for unipolar output voltage mode and bipolar output voltage mode (see Table 1).

The output buffer can source or sink as much as 10mA of current with an output voltage of at least 1V from either V_{CC} or A GND. As the output voltage approaches V_{CC} or A GND, the current sourcing/sinking capability of the output buffer is reduced. In unipolar operation, the output buffer can still swing down to within 10mV of A GND and up to within 40mV of V_{CC} with a 100kΩ load from V_{OUT} to A GND. In bipolar operation, the output buffer swing is limited to about 100mV from either rail.

Gain 1	Gain 0	Gain	Voltage Output Swing Relative to V_{ZS}
0	0	1/4	$V_{REF\ IN} \leftrightarrow 1/4$
0	1	1/2	$V_{REF\ IN} \leftrightarrow 1/2$
1	0	1	$V_{REF\ IN} \leftrightarrow 1$
1	1	2	$V_{REF\ IN} \leftrightarrow 2$

Table 1. Unipolar Output Voltage Mode

Gain 1	Gain 0	Gain	Voltage Output$_{P-P}$
0	0	1/4	$\pm V_{REF\ IN} \leftrightarrow 1/8$
0	1	1/2	$\pm V_{REF\ IN} \leftrightarrow 1/4$
1	0	1	$\pm V_{REF\ IN} \leftrightarrow 1/2$
1	1	2	$\pm V_{REF\ IN} \leftrightarrow 1$

Table 2. Bipolar Output Voltage Mode

FUNCTIONAL DESCRIPTION (Continued)

VOLTAGE REFERENCE

A bandgap voltage reference is incorporated on the ML2341 and ML2351. Two reference voltages can be produced by each device. An internal comparator monitors the power supply voltage to determine the selection of the reference voltage. A reference voltage of 2.25V on the ML2341, and 2.50V on the ML2351, is selected when the supply voltage is less than approximately 7.5V. Otherwise, a reference voltage of 4.50V, and 5.00V, respectively, is selected. To prevent the comparator from oscillating between the two selections avoid operation with a power supply in the range from 7.0V to 8.0V.

The bandgap reference is trimmed for zero Temperature Coefficient (TC) at 35°C to minimize output voltage drift over the operating temperature range.

The internal reference is buffered for use by the DAC and external circuits. The reference buffer will source more than 5mA of current and sink more than 1mA of current. The output voltage ranges of the ML2341 and ML2351 with V_{REF} IN connected to V_{REF} OUT are shown in Tables 3 and 4.

An external reference can alternatively be used on V_{REF} IN to set the desired full scale voltage. However, the linearity of the D/A converter depends upon the reference used. To ensure integral linearity at an 8 bit level a reference voltage >2V and <7V (2.75V for operation with a low voltage power supply) should be used.

DIGITAL INTERFACE

The digital interface of the device consists of a chip select input, $\overline{CS}$, a write input, $\overline{WR}$, a transfer input, XFER and eight data inputs, DB0 through DB7. The digital interface operates in one of the two modes — single- or double-buffered.

Single-Buffered Mode

To use the ML2341 and ML2351 in the single-buffered mode, tie XFER to logic "1" This will put the D/A latch in the transparent mode and the rising edge of $\overline{WR}$ at low level of $\overline{CS}$ will latch the data on DB0 - DB7 into the input latch as well as update the D/A output voltage.

Double-Buffered Mode

To use the devices in the double-buffered mode timing information is applied to both the $\overline{WR}$ and XFER inputs. The rising edge of $\overline{WR}$, when $\overline{CS}$ is at a low level, will latch the data on DB0 - DB7 into the input latch. The D/A output voltage will not be updated, however, until XFER is brought to a high level, which transfers the data from input latch to D/A latch. Note that the D/A latch is a transparent latch controlled by the level, not the edge, of the XFER input. Any write operation to the input latch while XFER is still at a high level results in the immediate update of the D/A output voltage.

POWER-ON RESET

The ML2341 and ML2351 have an internal power-on reset circuit to initialize the device when power is first applied to the device. The power-on reset interval of 8µs (typical) begins when V_{CC} reaches approximately 2.0V. During the power-on reset interval both the input and data latch are reset to all "0's"

Gain Setting	V_{REF} = 2.25V with $V_{CC} \leq$ 7.0V		V_{REF} = 4.50V with $V_{CC} \geq$ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
1/4	0 to 0.562V	–0.281V to 0.281V	0 to 1.125V	–0.562V to 0.562V
1/2	0 to 1.125V	–0.562V to 0.562V	0 to 2.25V	–1.125V to 1.125V
1	0 to 2.25V	–1.125V to 1.125V	0 to 4.50V	–2.25V to 2.25V
2	0 to 4.5V	–2.25V to to 2.25V	0 to 9.00V	–4.5V to 4.5V

Table 3. ML2341 DAC Output

Gain Setting	V_{REF} = 2.50V with $V_{CC} \leq$ 7.0V		V_{REF} = 5.00V with $V_{CC} \geq$ 8.0V	
	Unipolar	Bipolar	Unipolar	Bipolar
1/4	0 to 0.625V	–0.3125V to 0.3125V	0 to 1.25V	–0.625V to 0.625V
1/2	0 to 1.25V	–0.625V to 0.625V	0 to 2.50V	–1.25V to 1.25V
1	0 to 2.50V	–1.25V to 1.25V	0 to 5.00V	–2.50V to 2.50V
2	0 to 5.00V	–2.50V to 2.50V	0 to 10.0V	–5.00V to 5.00V

Table 4. ML2351 DAC Output

TYPICAL APPLICATIONS

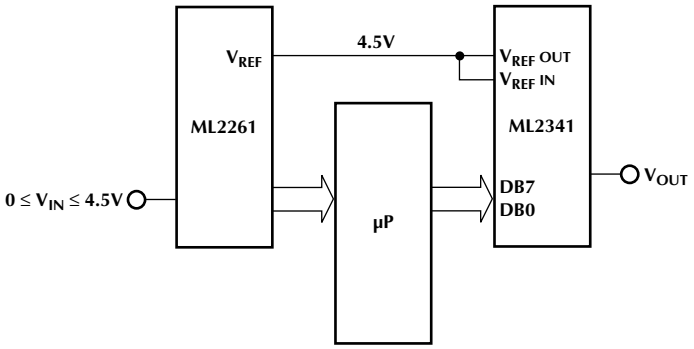


Figure 5. Sharing the 4.5V D/A Reference with an A/D (Single 5V V_{CC})

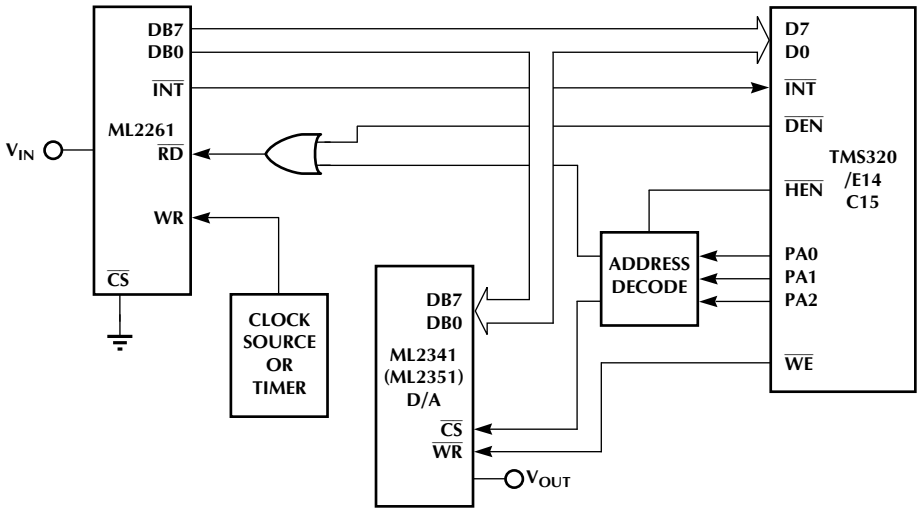


Figure 6. TMS320 Interface with D/A Output

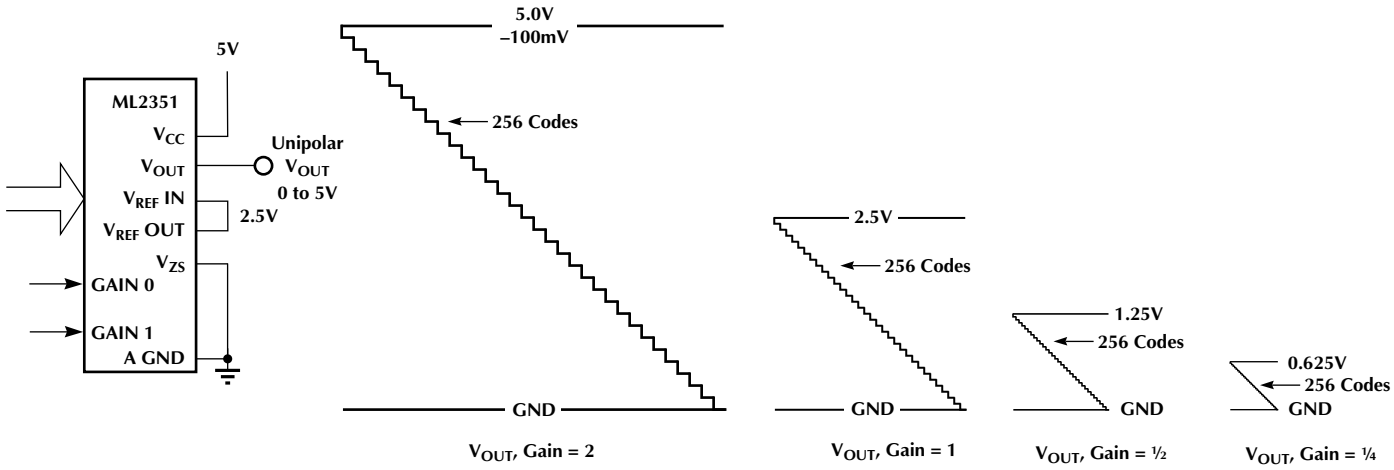


Figure 7. Single 5V Supply Unipolar V_{OUT}

TYPICAL APPLICATIONS (Continued)

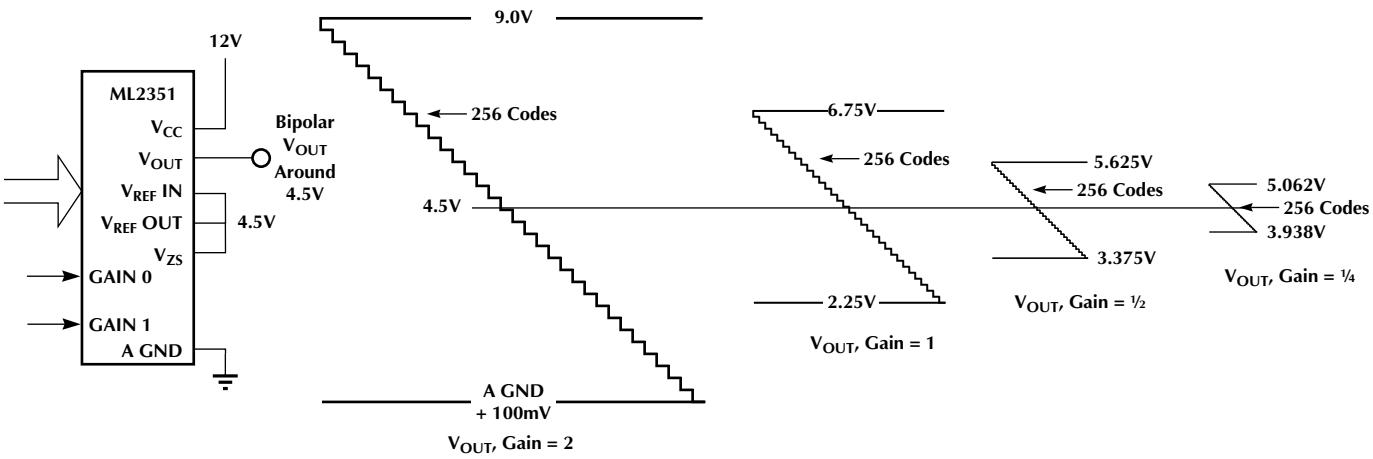


Figure 8. Single 12V Supply Bipolar V_{OUT} with 11 Bits of Resolution Around 4.5V

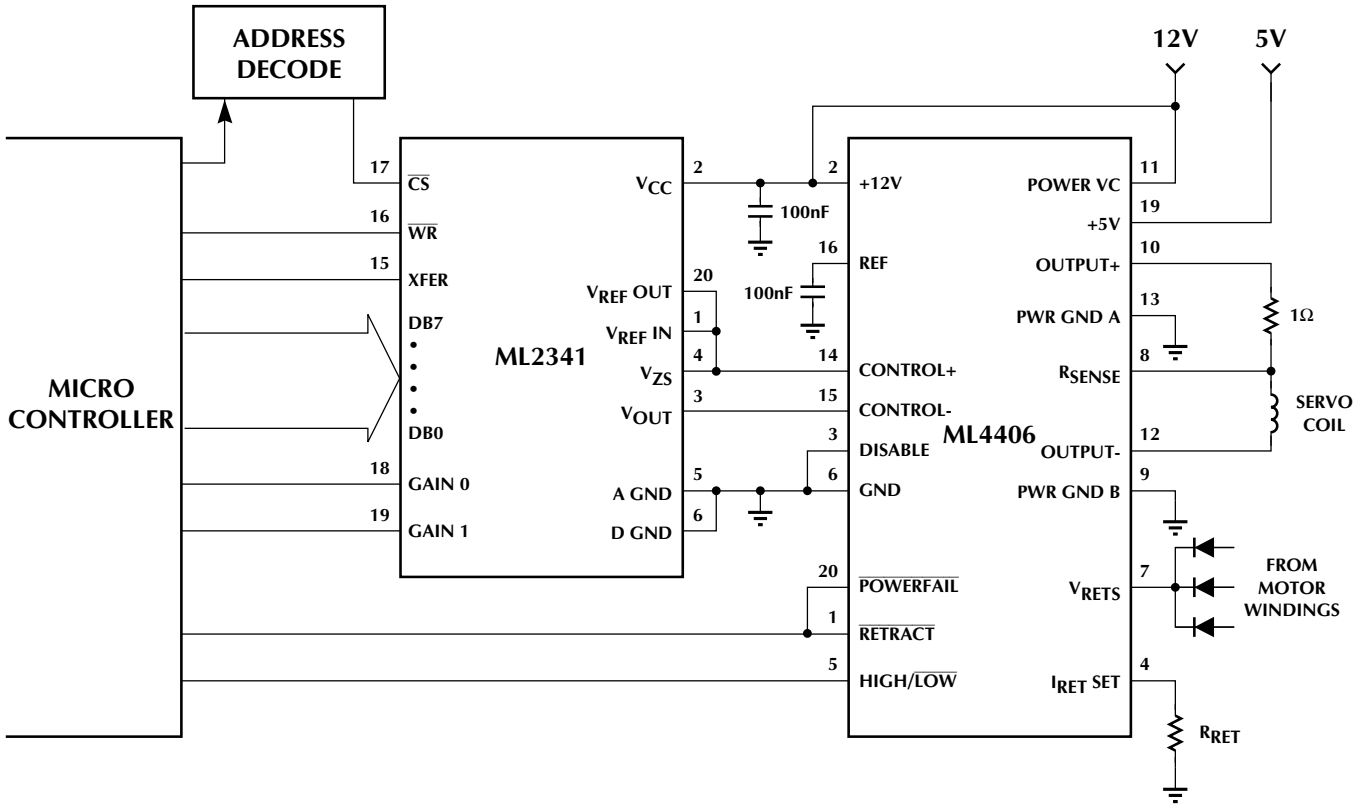
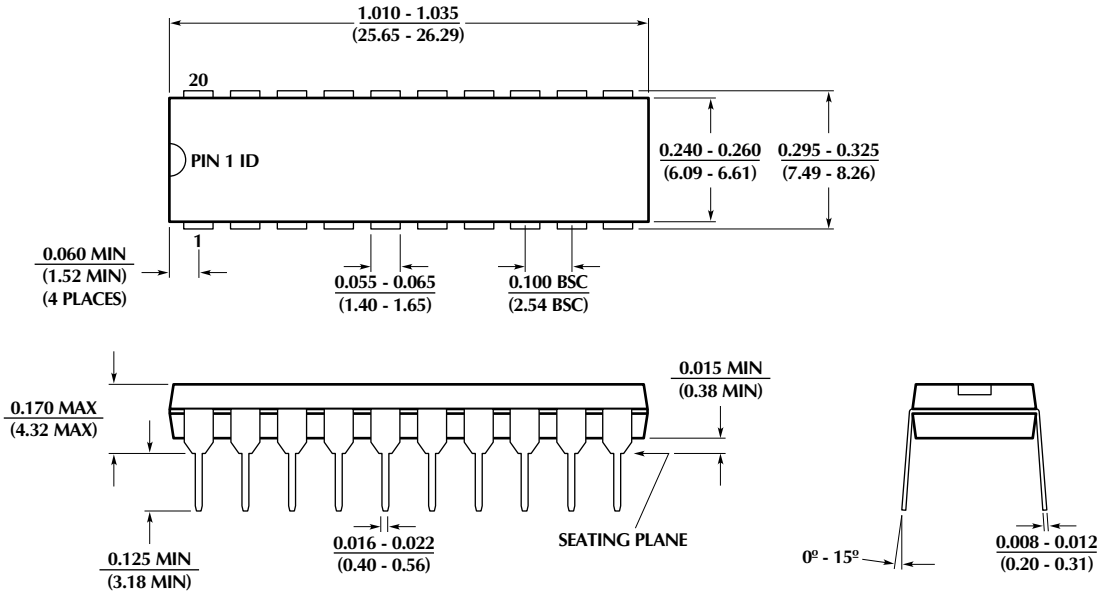


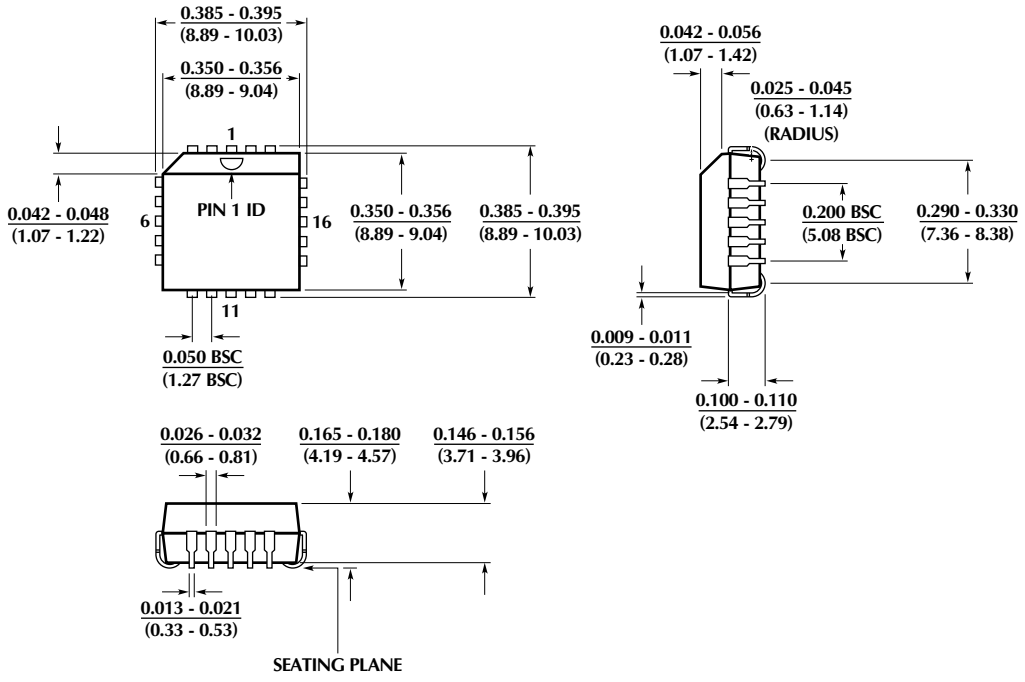
Figure 9. Servo Coil Driver Providing 13-Bit Effective Resolution

PHYSICAL DIMENSIONS inches (millimeters)

Package: P20
20-Pin PDIP

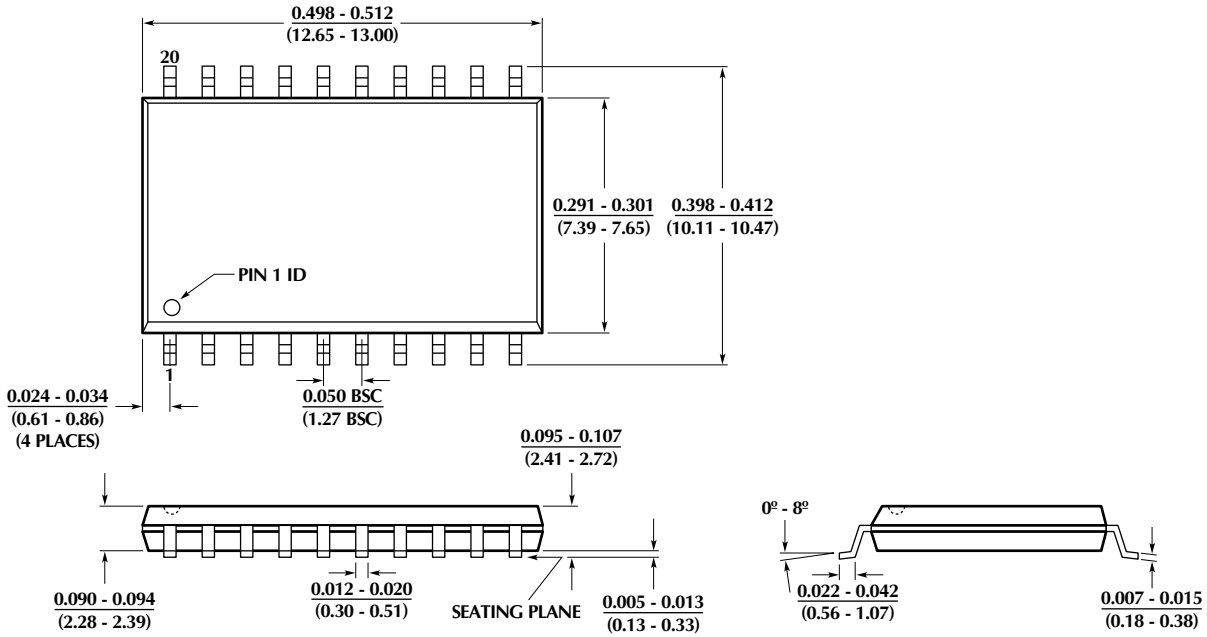


Package: Q20
20-Pin PLCC



PHYSICAL DIMENSIONS inches (millimeters)

Package: S20
20-Pin SOIC



ORDERING INFORMATION

PART NUMBER	V_{CC}/V_{REF} OUT	NON-LINEARITY	TEMPERATURE RANGE	PACKAGE
ML2341CCP-5	5V/2.25V	±½ LSB	0°C to 70°C	20-Pin PDIP (P20)
ML2341CCQ-5	5V/2.25V	±½ LSB	0°C to 70°C	20-Pin PLCC (Q20)
ML2341CCS-5	5V/2.25V	±½ LSB	0°C to 70°C	20-Pin SOIC (S20)
ML2341CCP-12	12V/4.5V	±½ LSB	0°C to 70°C	20-Pin PDIP (P20)
ML2341CCQ-12	12V/4.5V	±½ LSB	0°C to 70°C	20-Pin PLCC (Q20)
ML2341CCS-12	12V/4.5V	±½ LSB	0°C to 70°C	20-Pin SOIC (S20)
ML2351CCP-5	5V/2.5V	±½ LSB	0°C to 70°C	20-Pin PDIP (P20)
ML2351CCQ-5	5V/2.5V	±½ LSB	0°C to 70°C	20-Pin PLCC (Q20)
ML2351CCS-5	5V/2.5V	±½ LSB	0°C to 70°C	20-Pin SOIC (S20)
ML2351CCP-12	12V/5V	±½ LSB	0°C to 70°C	20-Pin PDIP (P20)
ML2351CCQ-12	12V/5V	±½ LSB	0°C to 70°C	20-Pin PLCC (Q20)
ML2351CCS-12	12V/5V	±½ LSB	0°C to 70°C	20-Pin SOIC (S20)

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565761; 5,592,128; 5,594,376. Japan: 2,598,946; 2,619,299. Other patents are pending.

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2092 Concourse Drive
San Jose, CA 95131
Tel: (408) 433-5200
Fax: (408) 432-0295