National Semiconductor

DM54L85/DM74L85 4-Bit Magnitude Comparators

General Description

These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input and low-level voltages applied to the A > B and A < B inputs.

Features

- Typical power dissipation 20 mW
- Typical delay (4-bit words) 55 ns

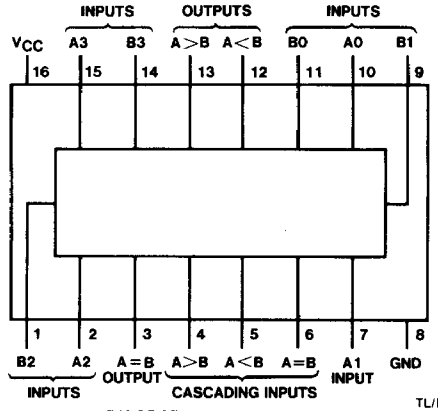
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



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54L85 (J) 74L85 (N)

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = High Level, L = Low Level, X = Don't Care (Either Low or High Logic Level)

Recommended Operating Conditions

Sym	Parameter	DM54L85			DM74L85			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	A < B			0.1	mA
			A > B			0.1	
			A = B			0.1	
			Others			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	A < B			10	μA
			A > B			10	
			A = B			10	
			Others			30	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	A < B			−0.18	mA
			A > B			−0.18	
			A = B			−0.18	
			Others			−0.54	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)				6.6	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)				7.0	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with all outputs open and all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

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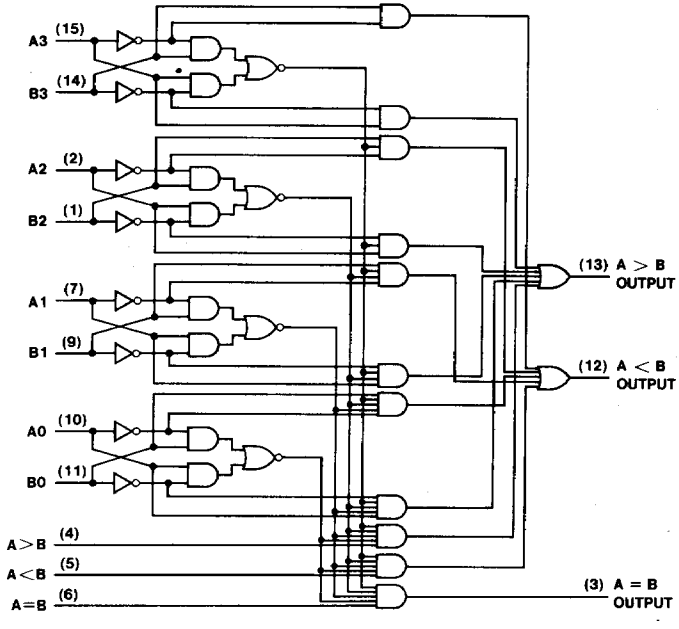
Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From Input	To Output	Number of Gate Levels	$R_L = 4\ k\Omega$, $C_L = 50\ pF$ Min	Typ	Max	Units
t_{PLH} Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A<B, A>B	1		70	115	ns
			2		70	115	
			3		70	115	
		A=B	4		70	115	
t_{PHL} Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A<B, A>B	1		55	90	ns
			2		55	90	
			3		55	90	
		A=B	4		55	90	
t_{PLH} Propagation Delay Time Low-to-High Level Output	A<B or A=B	A>B	1		55	100	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A<B or A=B	A>B	1		40	65	ns
t_{PLH} Propagation Delay Time Low-to-High Level Output	A=B	A=B	2		55	100	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A=B	A=B	2		40	65	ns
t_{PLH} Propagation Delay Time Low-to-High Level Output	A>B or A=B	A<B	1		55	100	ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	A>B or A=B	A<B	1		40	65	ns

Logic Diagram



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