HIGH RATE ACCUMULATOR/CORRELATOR
STEL-2410

ASIC
Custom
Products
Division

STANFORD
TELECOM®

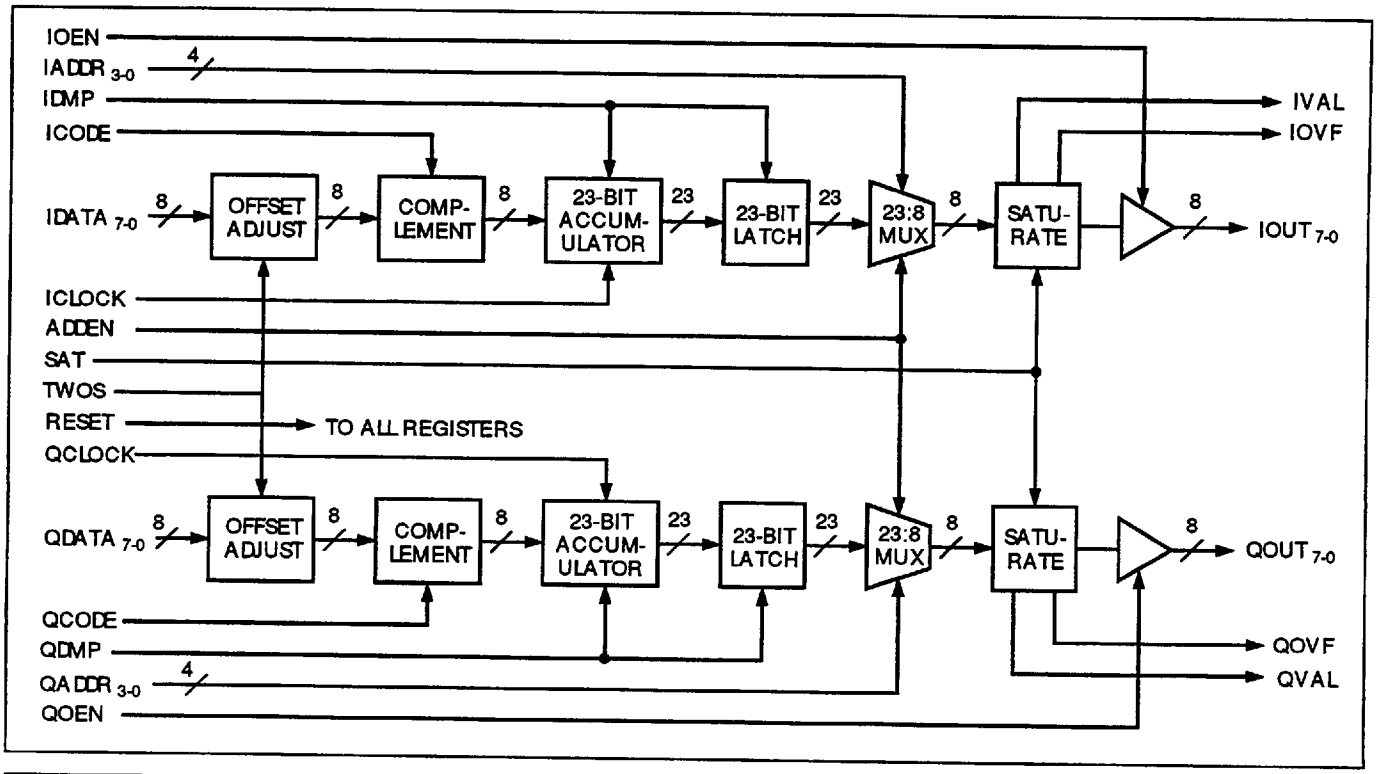
FEATURES

- **Up to 70 MHz accumulate rate**
- **Dual accumulators for quadrature signal applications**
- **Up to 32,768 cycles without overflow between dumps**
- **Accumulator latch and hold registers with selectable 8-bit output fields for easy interfacing**
- **Saturate-on-overflow capability**
- **Two's Complement or Offset Two's Complement signal inputs**
- **68-pin Plastic PGA package**

DESCRIPTION

The STEL-2410 is a dual high-speed accumulator/correlator circuit which can be used in many data communications applications. The dual circuits, which are completely independent, can be used to correlate dual data streams such as QPSK demodulated data. The 8-bit inputs can be in either regular 2's complement code (00_H = zero) or offset 2's complement code (FF_H = minimum negative value, 00_H = minimum positive value, no code corresponding to true zero). The inputs are multiplied by the reference code and accumulated in 23-bit accumulators, thereby ensuring at least 2^{15} cycles of accumulation without overflow. The outputs of the accumulators are viewed through 8-bit viewports (windows) for easy microprocessor interfacing, and the significance of each window is controlled by independent multiplexers. The data viewed in each window can be set to saturate on overflow, thereby eliminating the ambiguity caused when the accumulator value exceeds the range seen through the 8-bit viewport. Separate overflow flags allow the most significant bit of the data to be found rapidly. The device may be used to digitally despread direct sequence spread spectrum signals or may be used as a digital integrate and dump filter. The circuit is designed in 1.5 µ CMOS and will operate clock speeds up to 70 MHz.

BLOCK DIAGRAM

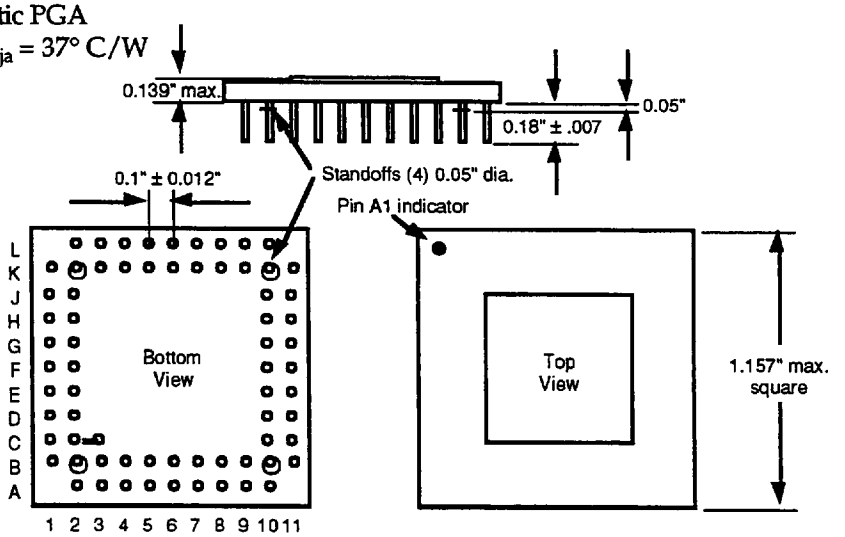


CIRCUIT DESCRIPTION

The STEL-2410 is a high speed accumulator/correlator capable of 2^{15} cycles of accumulation of the 70 Msample/sec. input signals without overflow. The high speed operation of the circuit is achieved through the pipelining of the accumulator, and this is made transparent to the user by means of proprietary I/O circuits. The accumulator contents can be dumped into the output latches in a single clock cycle, whereupon the accumulation process immediately restarts, from zero, without a break. The contents of the 23-bit output latch can then be viewed through the 8-bit output port. The position of the viewport can be selected by means of the multiplexers to view any contiguous group of eight bits in the 23-bit output latch. An overflow flag is provided to indicate whenever the position of the viewport is such that the signals appearing at the outputs are in an overflow condition. It is possible to set the output data to saturate under this condition, so that a false output value is not created. In addition, the input signal can be multiplied by ±1 by a single bit data stream before accumulation, allowing the device to operate as a correlator, as well as a simple accumulator. Two complete circuits are incorporated in the STEL-2410, making the device ideal for use with quadrature signals.

PIN CONFIGURATION

Package: 68 pin Plastic PGA
Thermal coefficient θ_{ja} = 37° C/W



Notes:
1. Pin diameter = 0.018" ± 0.02"
2. Tolerances on pin spacing are not cumulative.
3. Pins C2 and C3 are connected together.

PIN CONNECTIONS

A2	$IDATA_7$	B6	V_{SS}	E1	V_{DD}	H10	$QOUT_4$	K8	QDMP
A3	$IDATA_6$	B7	$QDATA_7$	E2	ICODE	H11	$QOUT_5$	K9	$QADDR_2$
A4	$IDATA_4$	B8	$QDATA_5$	E10	QCODE	J1	$IOUT_1$	K10	$QOUT_0$
A5	$IDATA_2$	B9	$QDATA_3$	E11	QCLK	J2	$IOUT_2$	K11	$QOUT_1$
A6	$IDATA_0$	B10	$QDATA_1$	F1	$IOUT_7$	J10	$QOUT_2$	L2	$IADDR_3$
A7	V_{DD}	B11	$QDATA_0$	F2	V_{SS}	J11	$QOUT_3$	L3	$IADDR_1$
A8	$QDATA_6$	C1	TWOS	F10	V_{SS}	K1	$IOUT_0$	L4	IDMP
A9	$QDATA_4$	C2	SAT	F11	V_{DD}	K2	I.C.	L5	IOVF
A10	$QDATA_2$	C10	ADDEN	G1	$IOUT_5$	K3	$IADDR_2$	L6	V_{DD}
B1	N.C.	C11	V_{SS}	G2	$IOUT_6$	K4	$IADDR_0$	L7	QVAL
B2	V_{SS}	D1	ICLK	G10	$QOUT_6$	K5	IVAL	L8	$QADDR_3$
B3	$IDATA_5$	D2	IOEN	G11	$QOUT_7$	K6	V_{SS}	L9	$QADDR_1$
B4	$IDATA_3$	D10	QOEN	H1	$IOUT_3$	K7	QOVF	L10	$QADDR_0$
B5	$IDATA_1$	D11	RESET	H2	$IOUT_4$				

Note: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

INPUT SIGNALS

RESET

The RESET input is asynchronous and active low. When RESET goes low, all registers are cleared within 15 nsecs. When RESET returns to a high level the data on the $IOUT_{7-0}$ and $QOUT_{7-0}$ buses will be invalid for 19 clock cycles, and both IVAL and QVAL will remain low during this period.

ICLK and QCLK

All synchronous functions performed within the I and Q channels of the device are referenced to the rising edge of the ICLK and QCLK inputs respectively. The ICLK and QCLK signals should nominally be square waves at a maximum frequency of 70 MHz. Non-repetitive ICLK and QCLK waveforms are permissible as long as the minimum durations of the positive and negative pulses are always greater than 4 nanoseconds.

$IDATA_{7-0}$ and $QDATA_{7-0}$

The 8-bit $IDATA_{7-0}$ and $QDATA_{7-0}$ buses are the inputs to the I and Q channels of the device, respectively. The signals can be presented in either two's complement or offset two's complement format. The formats are defined in the table below:

Code	Value in Two's comp.	Value in Offset two's comp.
80_H	Most negative	Most negative
FF_H	–1	$-1/2$ LSB
00_H	Zero	+

TWOS

The formats of the data used on the $IDATA_{7-0}$ and $QDATA_{7-0}$ buses is determined by the state of the TWOS input. When this input is high the input data is assumed to be in two's complement format, and when low the data is assumed to be in offset two's complement format.

ICODE and QCODE

When the STEL-2410 is being used as a correlator the ICODE and QCODE signals are multiplied with the data on the $IDATA_{7-0}$ and $QDATA_{7-0}$ buses, respectively. A high level on these inputs multiplies the data on the $IDATA_{7-0}$ and $QDATA_{7-0}$ buses by –1, and a low level multiplies the data by +1. The contents of the I and Q accumulators will then give the correlation product of the I and Q channels, respectively. When the device is being used as an accumulator the ICODE and QCODE inputs will normally be set to a high level.

IDMP and QDMP

The IDMP and QDMP and inputs control the framing of data in the I and Q accumulators, respectively. On the rising edge of the ICLK or QCLK following the falling edge of IDMP or QDMP, respectively, the contents of the corresponding accumulator is dumped into the dump register and the accumulator is cleared. The accumulator immediately restarts accumulating at the next rising edge of the clock, without any break. The data at the accumulator input at the rising edge of the clock following the falling edge of the dump signal will be accumulated before the dump occurs. Following the falling edge of IDMP or QDMP, IVAL or QVAL, respectively, will go low 4 clock cycles later, signifying that the corresponding output has become invalid. The IVAL or QVAL output will go high again after 16 clock cycles, indicating that the new accumulator value is now valid in the output port.

$IADDR_{3-0}$ and $QADDR_{3-0}$

The two address buses $IADDR_{3-0}$ and $QADDR_{3-0}$ control the significance of the 8-bit output windows of the I and Q channels, respectively. The dump register bits viewable in the output windows are set as shown in the table below:

$ADDR_{3-0}$	Acc. Field View
0_H	Bits 0 (LSB) - 7
1_H	Bits 1 - 8
2_H	Bits 2 - 9
3_H	Bits 3 - 10
4_H	Bits 4 - 11
5_H	Bits 5 - 12
6_H	Bits 6 - 13
7_H	Bits 7 - 14
8_H	Bits 8 - 15
9_H	Bits 9 - 16
A_H	Bits 10 - 17
B_H	Bits 11 - 18
C_H	Bits 12 - 19
D_H	Bits 13 - 20
E_H	Bits 14 - 21
F_H	Bits 15 - 22 (MSB)

This table applies to both the I and Q channels, and they are set independently.

SAT

The SAT input controls the overflow characteristics of the output data appearing at the $IOUT_{7-0}$ and $QOUT_{7-0}$ buses. When SAT is set high the data will saturate on overflow, as indicated by the corresponding overflow flag being set. If the overflow is positive the output value will be set to $7F_H$, and if it is negative the value will be set to 80_H, so that the MSB will always indicate the sign of the output data. When SAT is set low the output data will be the same as the corresponding bits in the dump register and the data will not be valid if the corresponding overflow flag is set.

ADDEN

When the ADDEN input is set low the $IADDR_{3-0}$ and $QADDR_{3-0}$ bus inputs are enabled, and when it is set high they are disabled and remain set to their previous values.

IOEN and QOEN

The IOEN and QOEN inputs control the I and Q channel outputs, respectively. When either of these signals is set low the corresponding output channel is enabled, and when set high the corresponding output channel bus is set to a high impedance.

OUTPUT SIGNALS

$IOUT_{7-0}$ and $QOUT_{7-0}$

The $IOUT_{7-0}$ and $QOUT_{7-0}$ buses allow the contents of the I and Q dump registers, respectively, to be read by a control processor. The output fields are determined by the $IADDR_{3-0}$ and $QADDR_{3-0}$ values as shown in the table on Page 4, and the bus states are controlled by the IOEN and QOEN signals. When the bus values are valid the IVAL and/or QVAL outputs will be set high. The outputs signals are in offset two's complement code.

IVAL and QVAL

The IVAL and QVAL signals indicate the validity of the data on the $IOUT_{7-0}$ and $QOUT_{7-0}$ buses. When either of these signals is low the data on the corresponding bus will be invalid, and when high it will be valid. IVAL and QVAL will both go low after a reset, and either one will also go low after the falling edge of the corresponding dump signal.

IOVF and QOVF

The IOVF and QOVF outputs are the overflow flags of the I and Q outputs, respectively. When either one is set high it indicates that the data on the corresponding output bus is in an overflow condition. These signals can be used to find the most significant bit of the output data very quickly by incrementing the appropriate address until the overflow flag resets.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	−40 to +125 −65 to +150	°C (Plastic package) °C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	−0.3 to + 7	volts
$V_{I(max)}$	Input voltage	−0.3 to V_{DD} + 0.3	volts
I_i	DC input current	± 10	mA

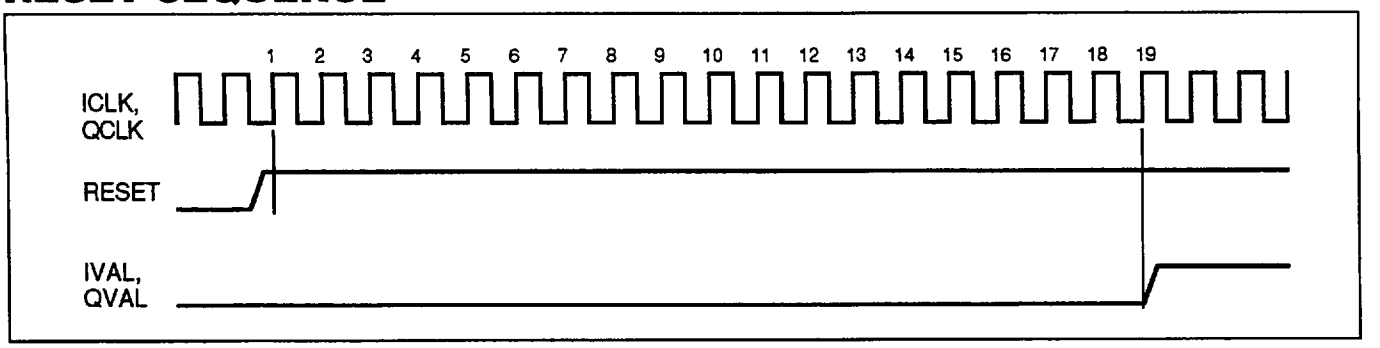
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units	
V_{DD}	Supply Voltage	+5 ± 5% +5 ± 10%	Volts Volts	(Commercial) (Military)
T_a	Operating Temperature (Ambient)	0 to +70 −55 to +125	°C °C	(Commercial) (Military)

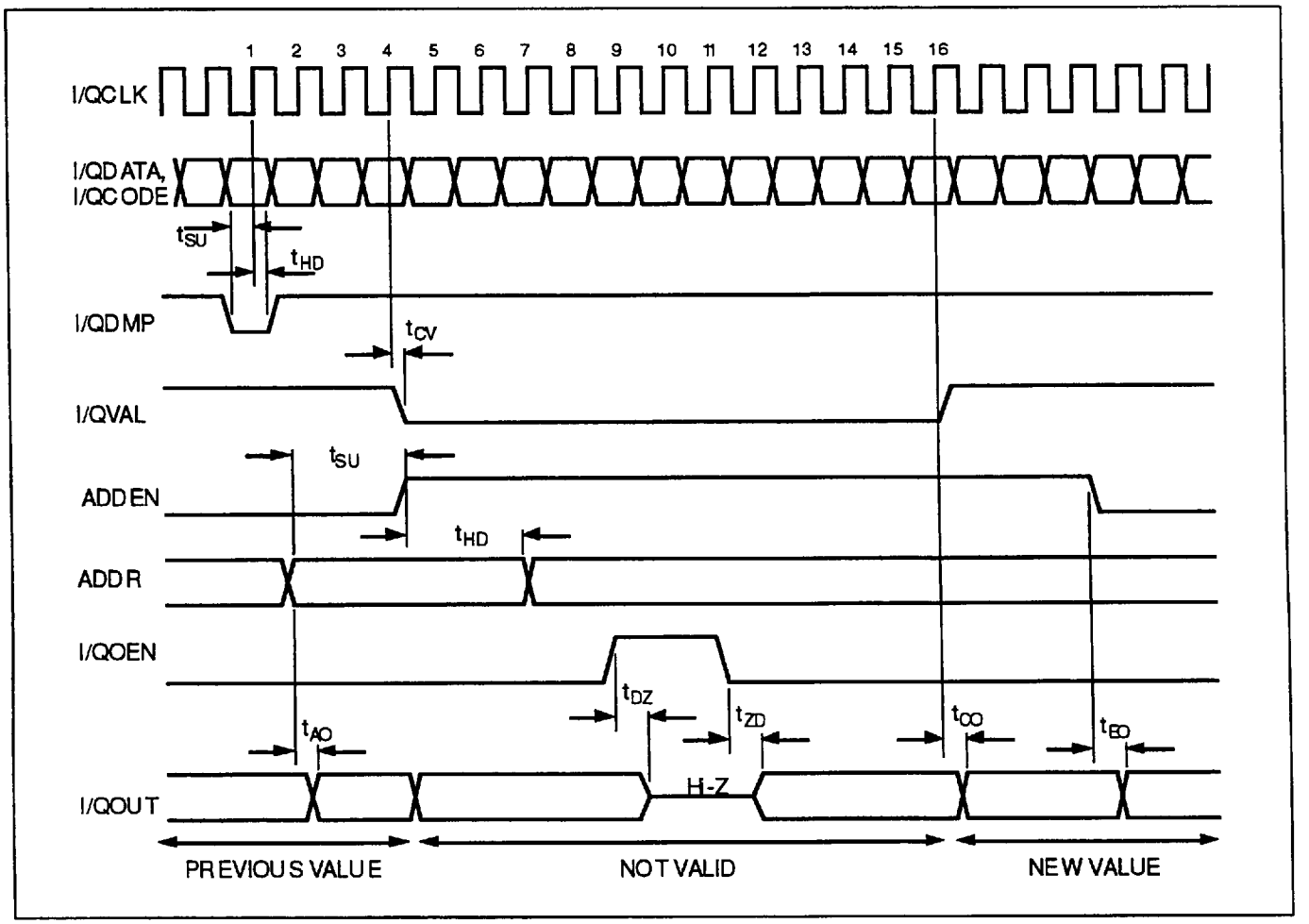
D.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{SS} = 0 V, T_a = 0° to 70° C, Commercial
V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, T_a = −55° to 125° C, Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			2.0	mA/MHz	f_{MCLK}= 70 MHz
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110		µA $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current			−10		µA $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = −4.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		−10	−45	−130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

RESET SEQUENCE



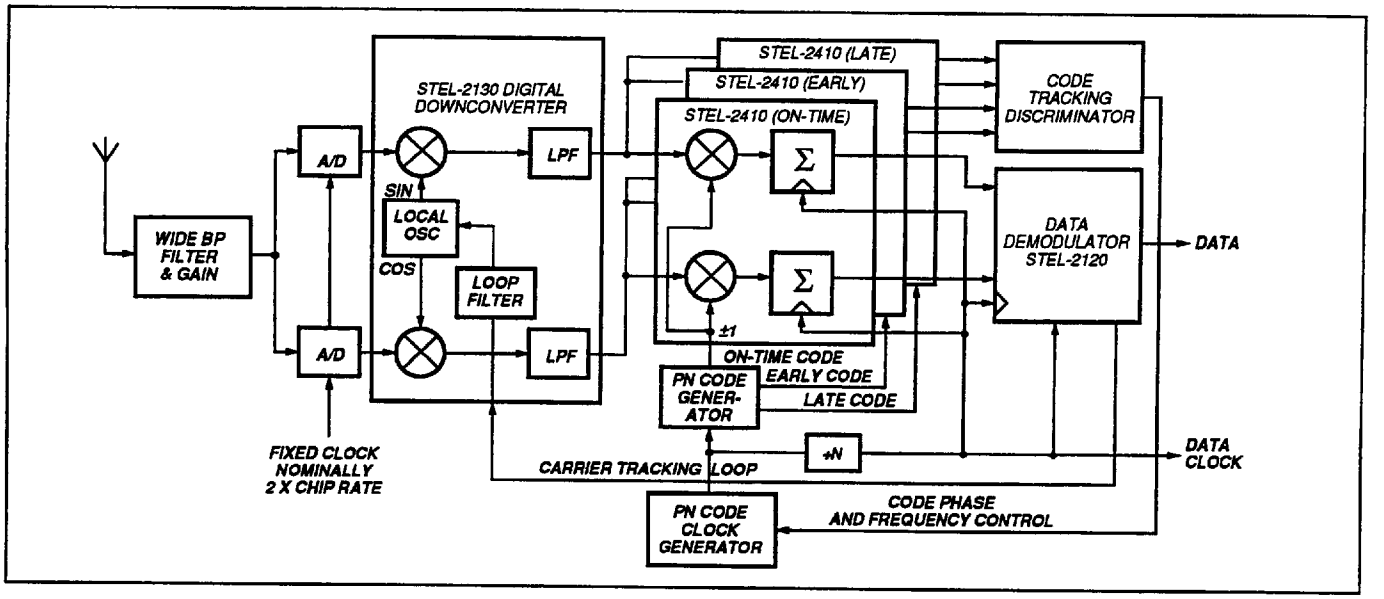
DUMP SEQUENCE



A.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 V ±5%, V_{SS} = 0 V, T_a = 0° to 70° C, Commercial
V_{DD} = 5.0 V ±10%, V_{SS} = 0 V, T_a = –55° to 125° C, Military)

Symbol	Parameter	Commercial		Military		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{RS}	RESET Pulse Width	30				nsec.	
t_{CH}	CLK High	4		6		nsec.	f_{MCLK}= 70 MHz
t_{CL}	CLK Low	4		6		nsec.	f_{MCLK}= 70 MHz
t_{SU}	I/QDMP, I/QCODE or I/QDATA to CLK and ADDR to ADDEN Setup	5		7		nsec.	
t_{HD}	I/QDMP, I/QCODE or I/QDATA to CLK and ADDR to ADDEN Setup	5		7		nsec.	
t_{LS}	I/QDMP pulse width	20		25		nsec.	
t_{DZ}	Delay, I/QOEN to I/QVAL Hi-Z	3	9	2	11	nsec.	Load = 20 pF max.
t_{DZ}	Delay, I/QOEN to I/QVAL valid	3	9	2	11	nsec.	Load = 20 pF max.
t_{CV}	Delay, I/QCLK to I/QVAL		20		24	nsec.	Load = 20 pF max.
t_{CO}	Delay, I/QCLK to I/QOUT		30		35	nsec.	Load = 20 pF max.
t_{AO}	Delay, ADDR to I/QOUT		35		42	nsec.	Load = 20 pF max.
t_{EO}	Delay, ADDEN to I/QOUT		35		42	nsec.	Load = 20 pF max.

TYPICAL APPLICATION - LONG CODE SPREAD SPECTRUM RECEIVER



FOR FURTHER INFORMATION
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