Advanced Information

# Five Band Graphic Equalizer Filter and Display Driver

## GENERAL INFORMATION

The XR-1094 is a single chip graphic equalizer and display driver containing switched-capacitor band-pass filters, filter multiplexer, data latches and high voltage vacuum fluorescent display driver. The five band-pass filters have two octave spacing from 63Hz up to 16kHz. The high filter can be selected for either 10kHz or 16kHz center frequency. They are followed by five peak detectors, a filter multiplexer, and high voltage driver. A digital peak detector is provided for he maximum signal level (total output) in the band-pass filter frequency range. An on-chip power on reset circuit blanks the display outputs for one second after power up to eliminate power up noise on the display.

The output multiplexer is designed to interface with most vacuum florescent display drivers. The display can have up to 13 levels and 5 frequency bands, as well as peak sum. The high voltage P-channel drive transistors can drive up to 45 volts.

The XR-1094 is fabricated in a 3um double polysilicon CMOS process, resulting in accurate filters, tight gain tolerances and low noise. The nominal operating voltage is +/-5VDC. The chip includes a self contained RC oscillator with a nominal frequency of 400kHz. Only an external resistor and capacitor are needed.

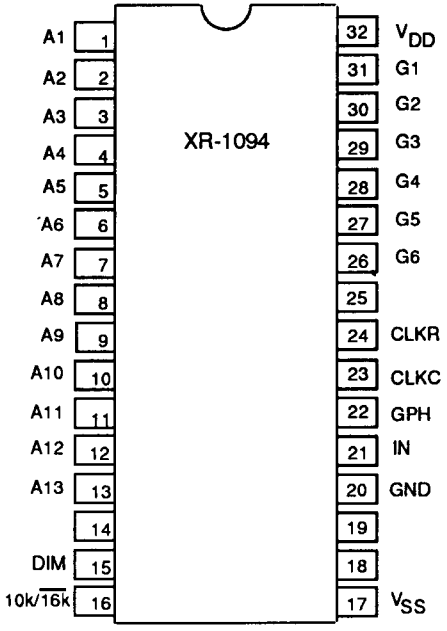
## FEATURES

Single Chip Equalizer and Display Driver
Accurate Switched-Capacitor Filters
30dB of Gain
Peak Hold Display Drive
Simple Resistor and Capacitor Oscillator
DIM Control for Display Brightness
Low Noise, Low Power CMOS
Selectable 10kHz/16kHz Filter

## APPLICATIONS

Graphic Equalizers
Tape Recorders
Receivers
Portable Systems
Spectrum Analyzers

## PIN ASSIGNMENT




## ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-1094 CP | 32 Pin Plastic SDIP | -30°C to 75°C |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{DD}$ | 7VDC |
| $V_{SS}$ | -7VDC |
| VDS of High Voltage P-Channel Driving Transistors Relative to $V_{DD}$ | - 45 V |
| Power Dissipations (package limitation) | |
| 32 Pin Plastic Package | 1W |
| Derate above 25°C | 9 mW/°C |
| Storage Temperature | -60 to +150°C |

5

## ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| VDD | +Supply | 4.5 | 5.0 | 6.0 | VDC | |
| VSS | -Supply | -4.5 | -5.0 | -6.0 | VDC | |
| IDD | Supply current | | 10 | | mA | VDD=5; VSS=-5 |
| Iil | Input leakage | -2 | | 2 | µA | Digital Inputs<br>Analog Inputs |
| Ioff | Output off leakage A & G Outputs | | | 10 | µA | Vin=0V; VD=-38V |
| Vih | Digital input high voltage threshold | | 1.6 | 2.4 | VDC | |
| Vil | Digital input low voltage threshold | 0.8 | 1.6 | | VDC | |
| Fclk | Clock frequency accuracy | 375 | 400 | 425 | kHz | |
| $f_o$ | Filter Center Frequency | -7 | 0 | 7 | % | |
| VOUTG | All G outputs | -1.0 | 2.5 | 5 | V | VDD=5V<br>IGL=14mA |
| VOUTA | All A outputs | 2.5 | 3.75 | 5 | V | VDD=5V<br>IAL=2.5mA |
| $T_D$ | Output Decay Time | | 330 | | ms | |
| $t_d$ | Duty cycle | | 1/11.4<br>1/39.5 | | | Dim = 0<br>Dim = V+ |
| GPH | Display peak hold time | | 0.5 | | S | R=100KΩ, C=1µf |

**ELECTRICAL CHARACTERISTICS (cont.)**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| A1(Note1) | -12dB | 7.5 | 8.4 | 9.5 | mvpk | |
| A2 | -10dB | 9.5 | 11 | 12 | mvpk | |
| A3 | -8dB | 12 | 13 | 15 | mvpk | |
| A4 | -6dB | 15 | 17 | 19 | mvpk | |
| A5 | -4dB | 19 | 21 | 24 | mvpk | |
| A6 | -2dB | 24 | 26.7 | 29 | mvpk | |
| A7 | -0dB | 29 | 34 | 38 | mvpk | |
| A8 | +2dB | 38 | 42 | 47.5 | mvpk | |
| A9 | +4dB | 47.5 | 53 | 59.8 | mvpk | |
| A10 | +6dB | 59.8 | 67 | 75.3 | mvpk | |
| A11 | +8dB | 75.3 | 84 | 95 | mvpk | |
| A12 | +10dB | 95 | 106 | 119 | mvpk | |
| A13 | +12dB | 119 | 134 | 150 | mvpk | |

*Note 1: Amplified levels are relative to VSS at -5 volts nominal. Levels will vary linearly with voltage on VSS.*

5

**PIN DESCRIPTION**

| PIN# | SYMBOL | DESCRIPTION |
|---|---|---|
| 1-13 | A1-A13 | Display levels 1-13, indicating signal strength on G1-G6 |
| 26-31 | G6-G1 | Time allocation for display function<br>G1 63Hz<br>G2 250Hz<br>G3 1kHz<br>G4 4kHz<br>G5 10kHz/16kHz<br>G6 Total Output |
| 15 | DIM | DIM Display: This pin, when high, reduces the brightness of the display by adjusting the on-time of the segments |
| 16 | 10k/$\overline{16k}$ | 10kHz/$\overline{16kHz}$ filter select input. Logic "0" (low) will select the 16kHz filter and logic "1" (high) will select the 10kHz filter |
| 17 | VSS | Minus supply, nominally -5VDC |
| 20 | GND | Analog input reference |
| 21 | IN | Audio input |
| 22 | GPH | Filter amplitude display duration control resistor and a timing capacitor from this pin to VSS will control the duration of peak hold for all six outputs |
| 23 | CLKC | Oscillator timing capacitor between this pin and VSS |
| 24 | CLKR | Oscillator timing resistor between this pin and CLKC pin |
| 32 | VDD | Plus supply, nominally 5VDC |

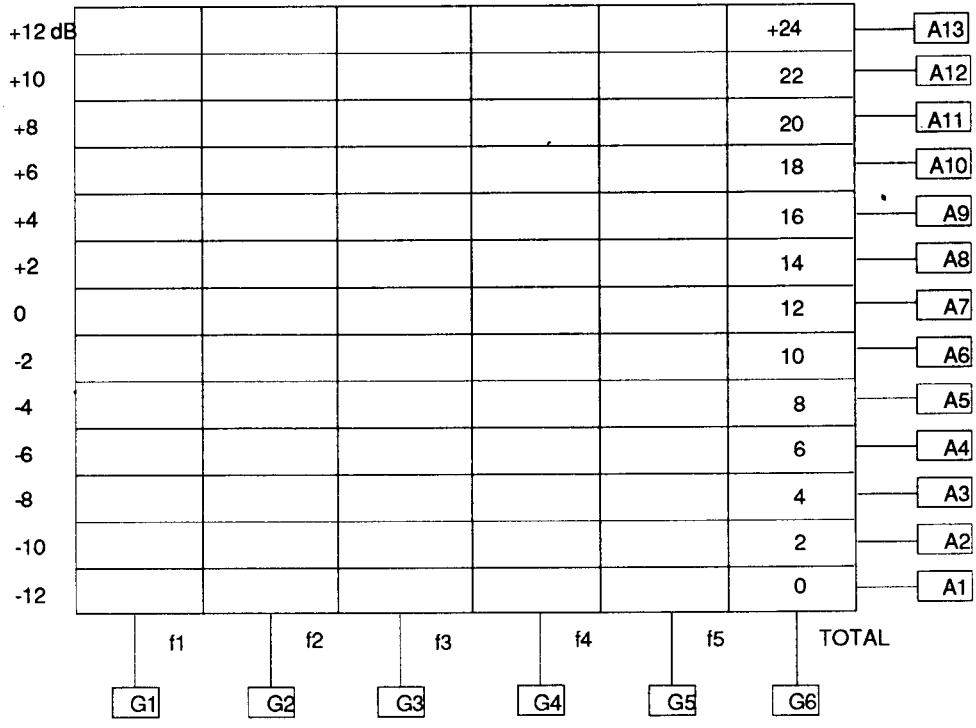



**Figure 1. Typical Display**

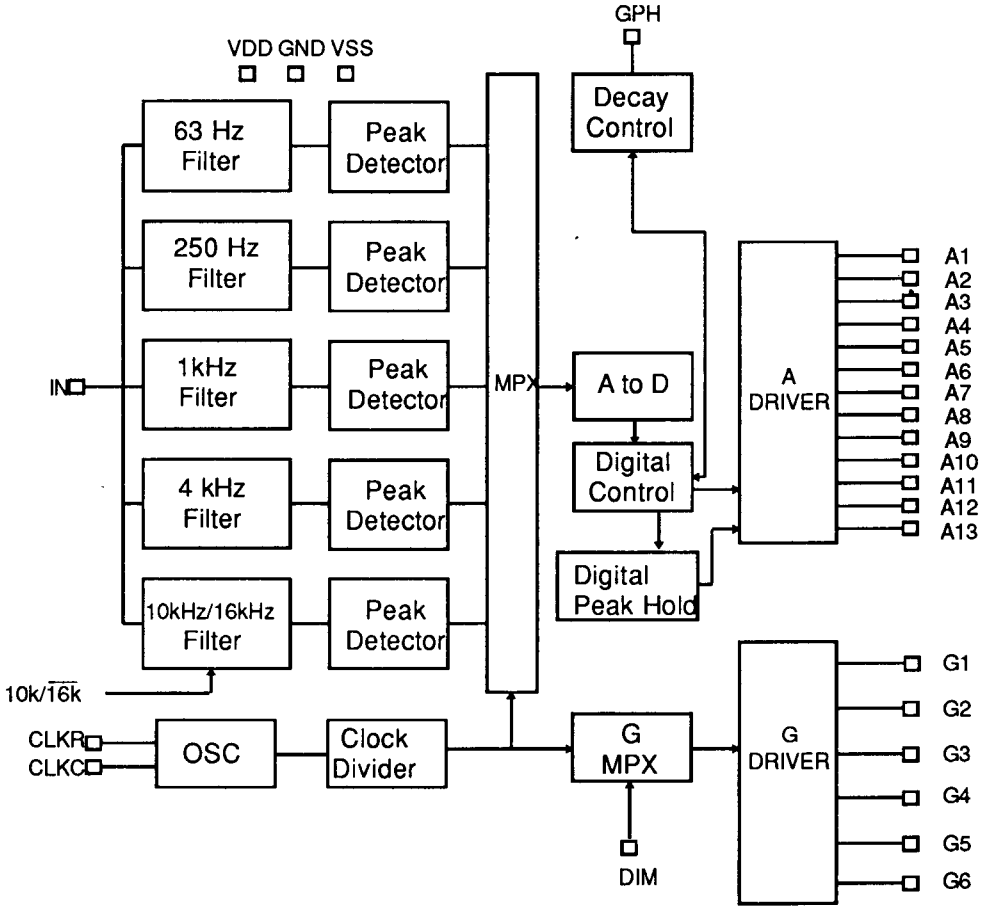



**Figure 2. Block Diagram**

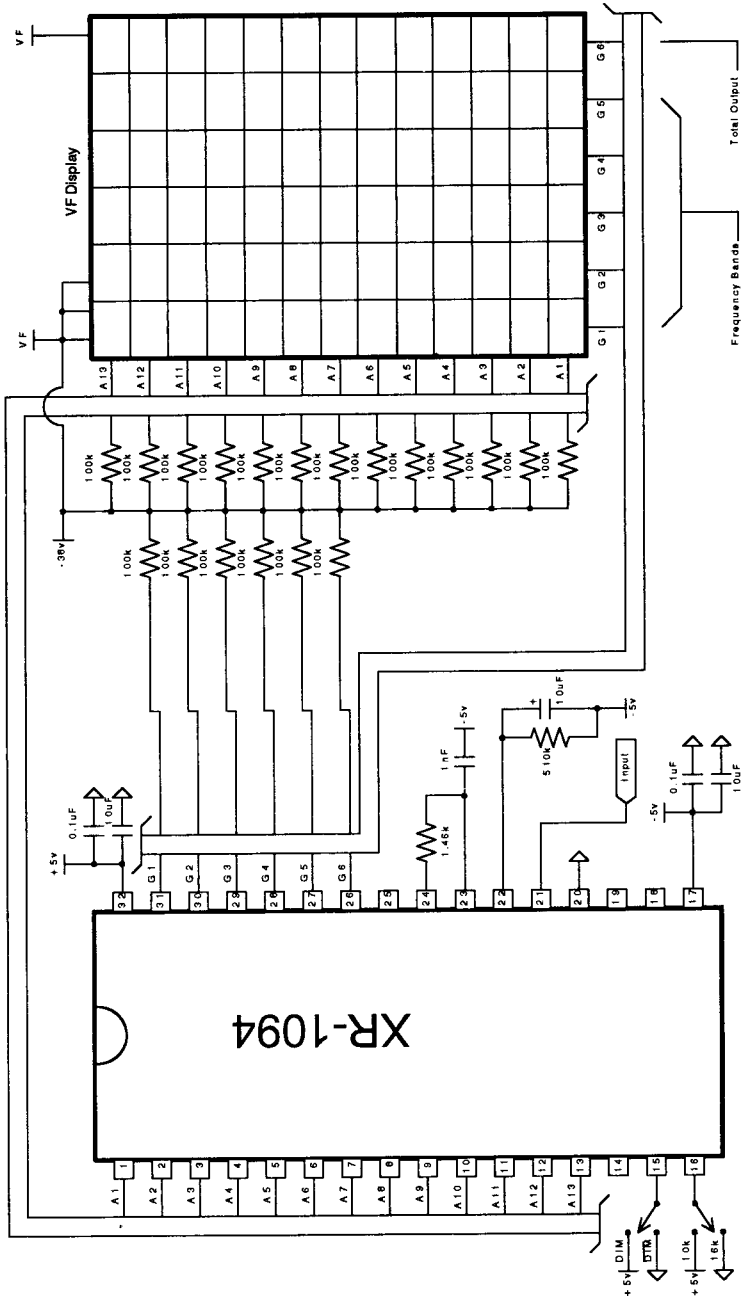



**Figure 3. Typical Application Schematic**