MOTOROLA

MC3419
MC3519

Advance Information

TELEPHONE LINE FEED AND 2- TO 4-WIRE CONVERSION CIRCUIT

. . . designed to replace the hybrid transformer circuit in Class 5, PABX and Subscriber carrier equipment, providing signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. It provides dc line current for powering the telset, operating from up to a 60 V supply.

- Transmit and Receive Gain is Externally Selected
- On-Hook Power Below 5.0 mW
- Current Sensing Outputs Provided for Off-Hook Status from Both Tip and Ring Leads
- Size and Weight Reduction Over Present Approaches
- Compatible with IEEE and REA Specifications
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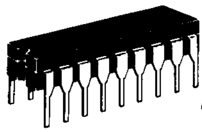
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 701

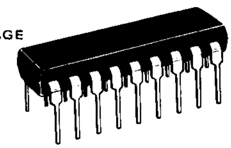


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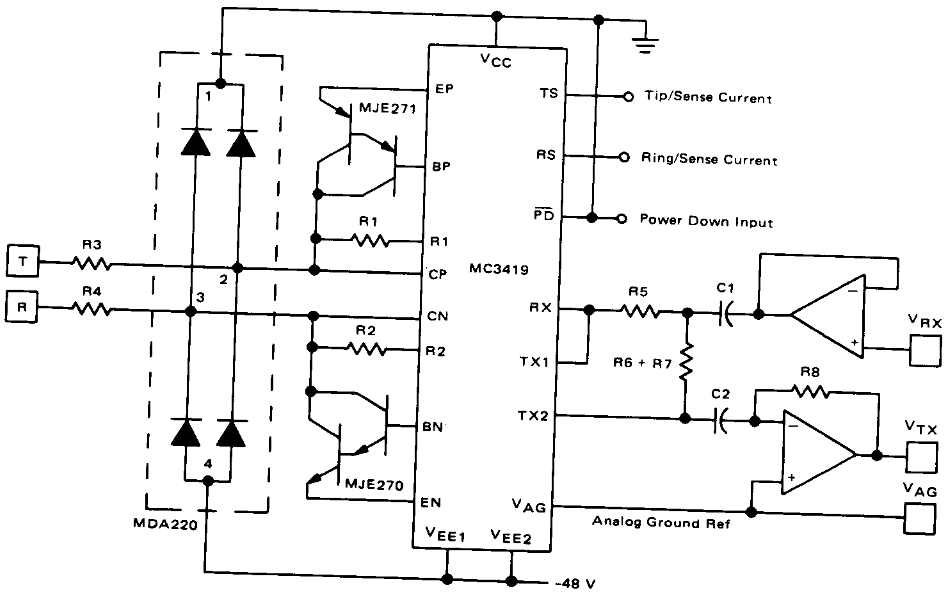
FIGURE 1 – SUBSCRIBER LOOP INTERFACE CIRCUIT DIAGRAM



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Maximum Rated Voltage		V_{EE1}, V_{EE2}	60	Vdc
Maximum Power Dissipation $T_A = 25^oC$ Derate above $+25^oC$		P_D	1.5	Watts
Operating Ambient Temperature Range	MC3419 MC3519	T_A	0 to +70 -40 to +85	^oC
Storage Temperature Range		T_{stg}	-65 to +150	^oC
Operating Junction Temperature		T_J	150	^oC

ELECTRICAL CHARACTERISTICS ($V_{EE1} = V_{EE2} = -48$ V, $V_{CC} = 0$, $V_{AG} = -6.0$ V, $T_A = 25^oC$)

Characteristic	Symbol	Min	Typ	Max	Unit
Loop Current Range ($R_{Loop} = 0 - 1900$ Ω)	I_{Lp}	20	–	120	mA
Transhybrid Reception Ratio – Figure 2 ($R_L = 900$ Ω, $V_{RX} = 0.775$ V_{RMS}, $V_G = 0$)	V_{RL}/V_{RX}	-0.1	0	+0.1	dB
Transhybrid Transmission Ratio – Figure 2 ($R_L = 900$ Ω, $V_{RX} = 0$, $V_G = 0.775$ V_{RMS})	V_{TX}/V_{RL}	-0.1	0	+0.1	dB
Transhybrid Rejection Ratio – Figure 2 ($R_L = 900$ Ω, $V_{RX} = 0.775$ V_{RMS}, $V_G = 0$)	V_{TX}/V_{RX}	–	-46	–	dB
Input Resistance (@R and T)—Figure 2	R_{in}		900		Ω
In-Band Longitudinal Suppression Ratio – Figure 3 ($e_{Lon} = 0.775$ V_{RMS}, f = 1 kHz, $R_L = 900$ Ω)	V_{TX}/e_{Lon}	–	-66	–	dB
60 Cycle Longitudinal Suppression Ratio – Figure 3 ($e_{Lon} = 30$ V_{RMS}, f = 60 Hz, $R_L = 1900$ Ω)	V_{TX}/e_{Lon}	–	-66	–	dB
Longitudinal Capacity – Figure 3 (60 Hz)	i_{Lon}	–	35	–	mA_{RMS}
Level Linearity (f = 300 Hz to 3400 Hz, Reception $V_{RX} = 0.775$ V_{RMS}, Transmission $V_{RL} = 0.775$ V_{RMS})	 V_{RX}/V_{RL} V_{RL}/V_{TX}	 -0.1 -0.1	 – –	 +0.1 +0.1	 dB dB
Idle Noise		–	0	–	$dBrnC_O$
Off-Hook Power Dissipation (IC) ($I_{Loop} = 120$ mA)	$P_{D(Off)}$	–	0.6	–	Watts
On-Hook Power Dissipation	$P_{D(On)}$	–	5.0	–	mW
Tip Status Current ($I_{Loop} = 0$ to 120 mA)	I_{TS}/I_T	–	0.0104	–	mA/mA
Ring Status Current ($I_{Loop} = 0$ to 120 mA)	I_{RS}/I_R	–	0.0104	–	mA/mA
Voltage Range of Analog Ground	V_R	0	–	-12	Volts
Analog Ground Input Current	I_{Gnd}	–	1.0	–	µA
Fault Currents (Tip to V_{CC} – Figure 2) (Ring to V_{CC} – Figure 2) (Ring and Tip to V_{CC} – Figure 2) (Tip to Ring Short – Figure 2)	 I_T I_R $\|I_T\|+\|I_R\|$ $I_T + I_R$	 – – – -	 0 5.0 5.0 120	 – – – –	 mA mA mA mA
Power Down Input Levels Logic High Logic Low	 V_{IH} V_{IL}	 V_{CC}-1.0 –	 – –	 – V_{CC}-2.0	Vdc

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FIGURE 2 – AC TRANSMISSION TESTS OF MC3419 AT BALANCE

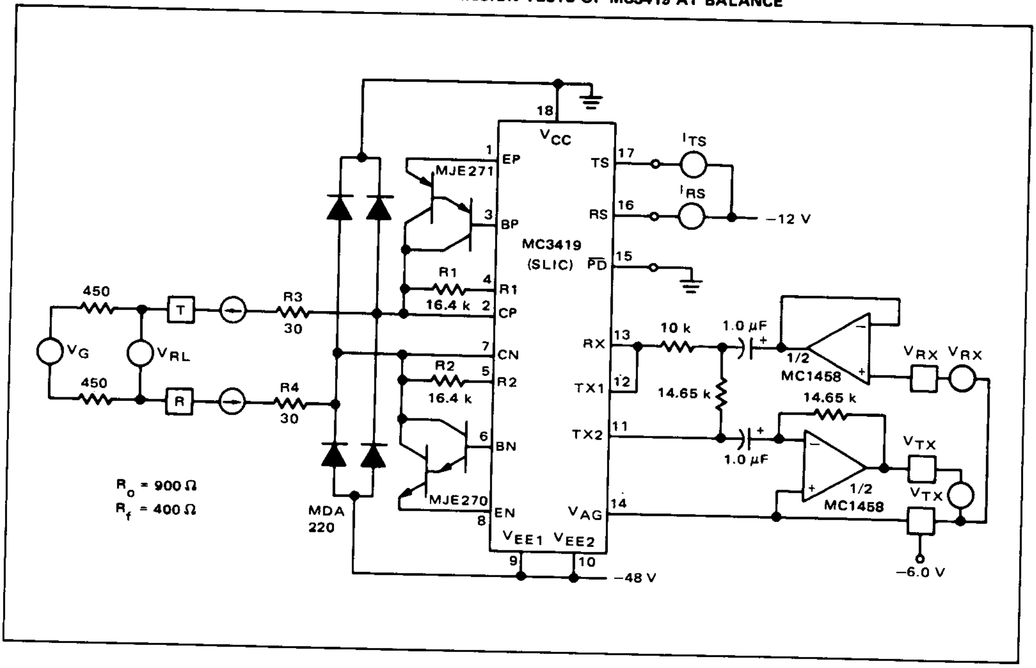


FIGURE 3 – LONGITUDINAL TEST

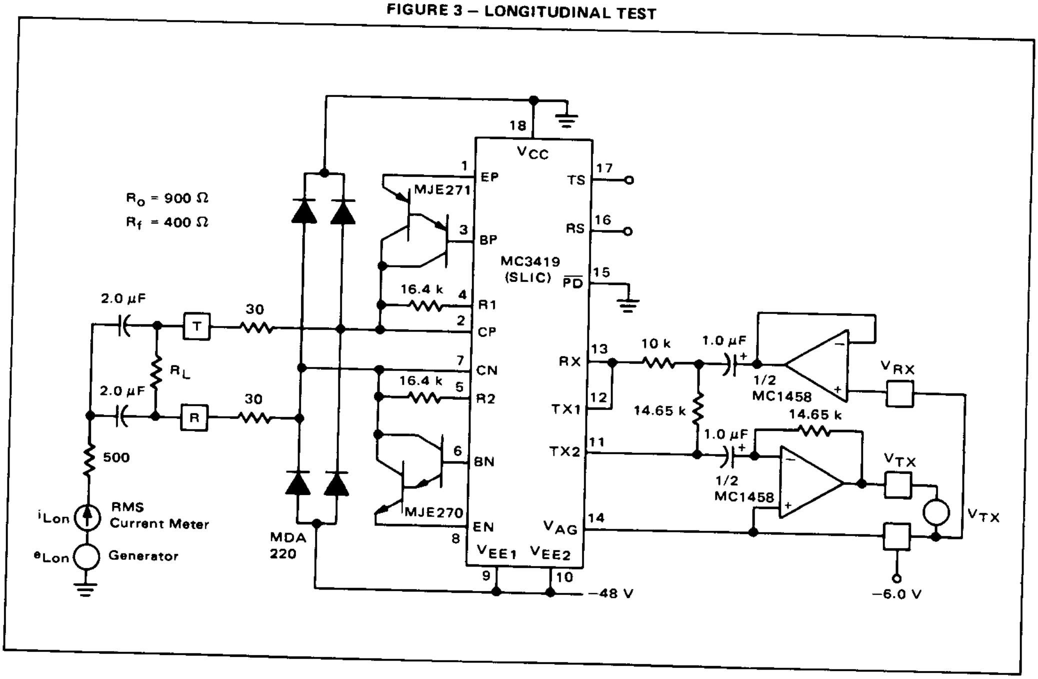
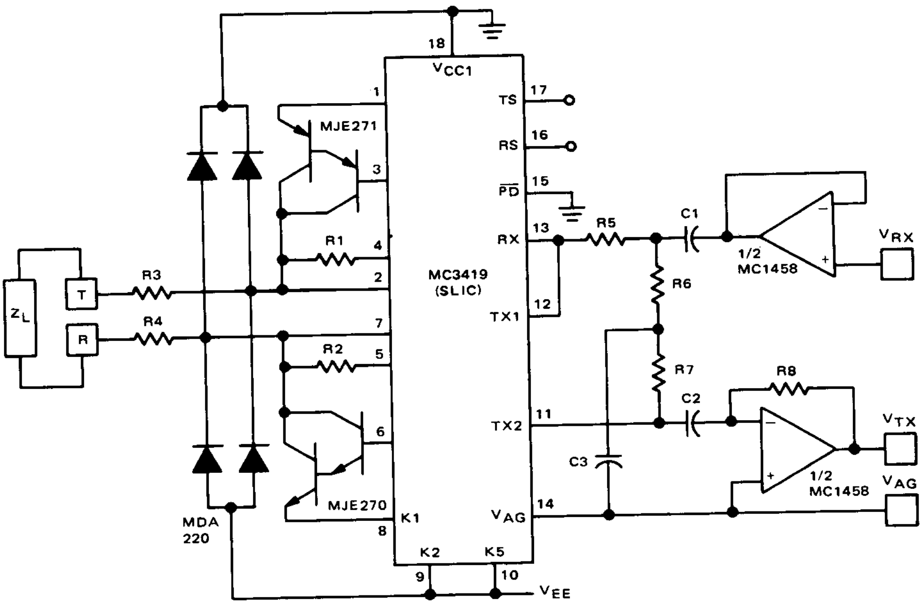


FIGURE 4 — DESIGN EQUATIONS



Internal to the MC3419 are three precise gain constants

K1 = 4 K2 = 23.75 K5 = 0.4 K5′ = 0.6

K5 and K5′ are selected by connecting TX1 or TX2 to RX respectively. The remaining TX pin is connected to R6 and R7.

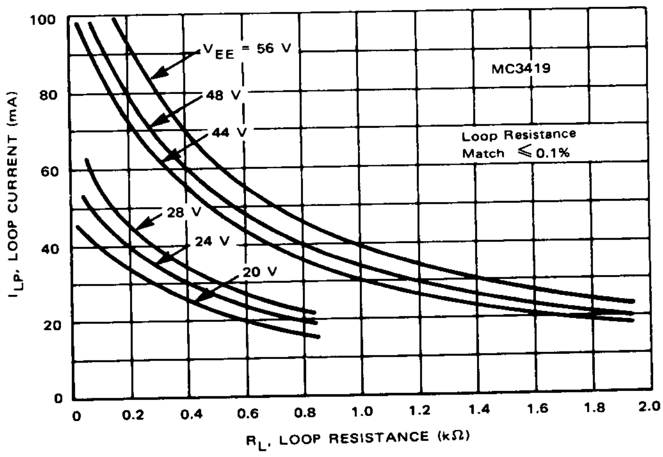
1. The dc feed resistance is R_f

$$R_f = \frac{R1 + R2}{1 + K1K2} + R3 + R4$$

2. The termination resistance is R_o

$$R_o = \frac{R1 + R2}{1 + K1K2K5} + R3 + R4$$

FIGURE 5 — HYBRID LOOP CURRENT versus LOOP RESISTANCE (FOR 24 AND 48 V SUPPLY)



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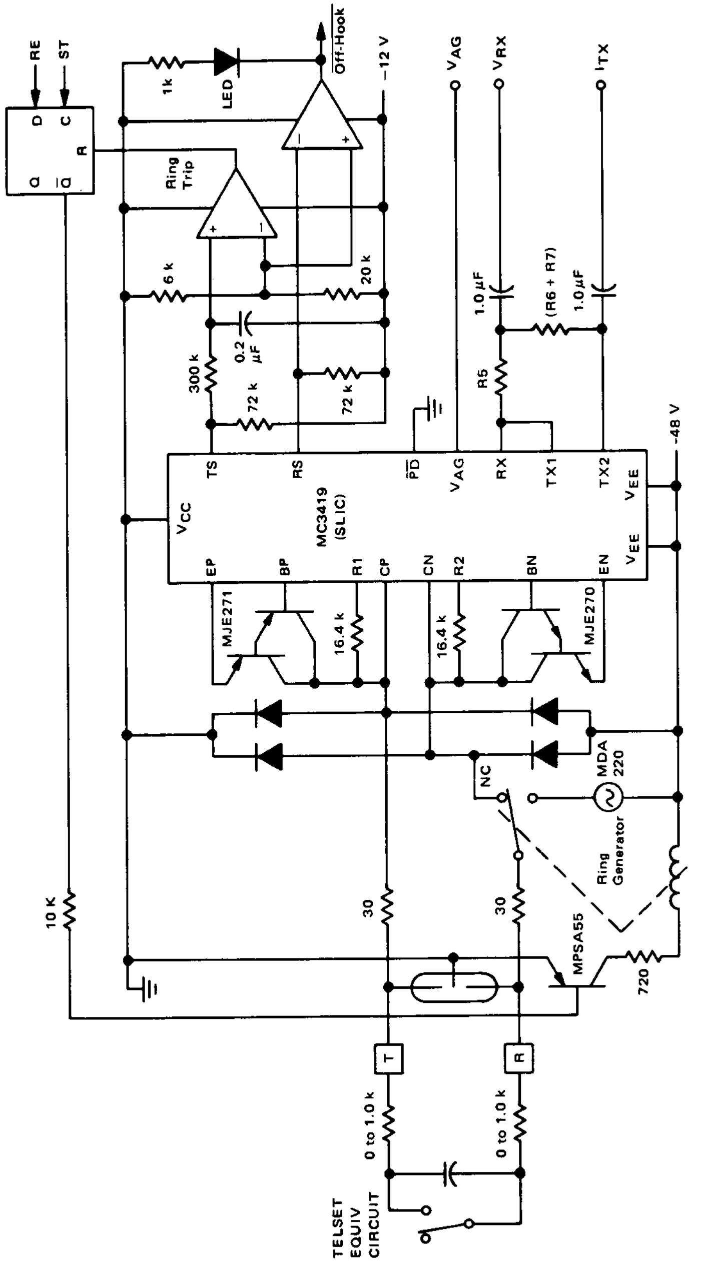

FIGURE 6 — RING TRIP USING MC3419

FIGURE 7 — MOTOROLA 3-CHIP SUBSCRIBER CHANNEL UNIT

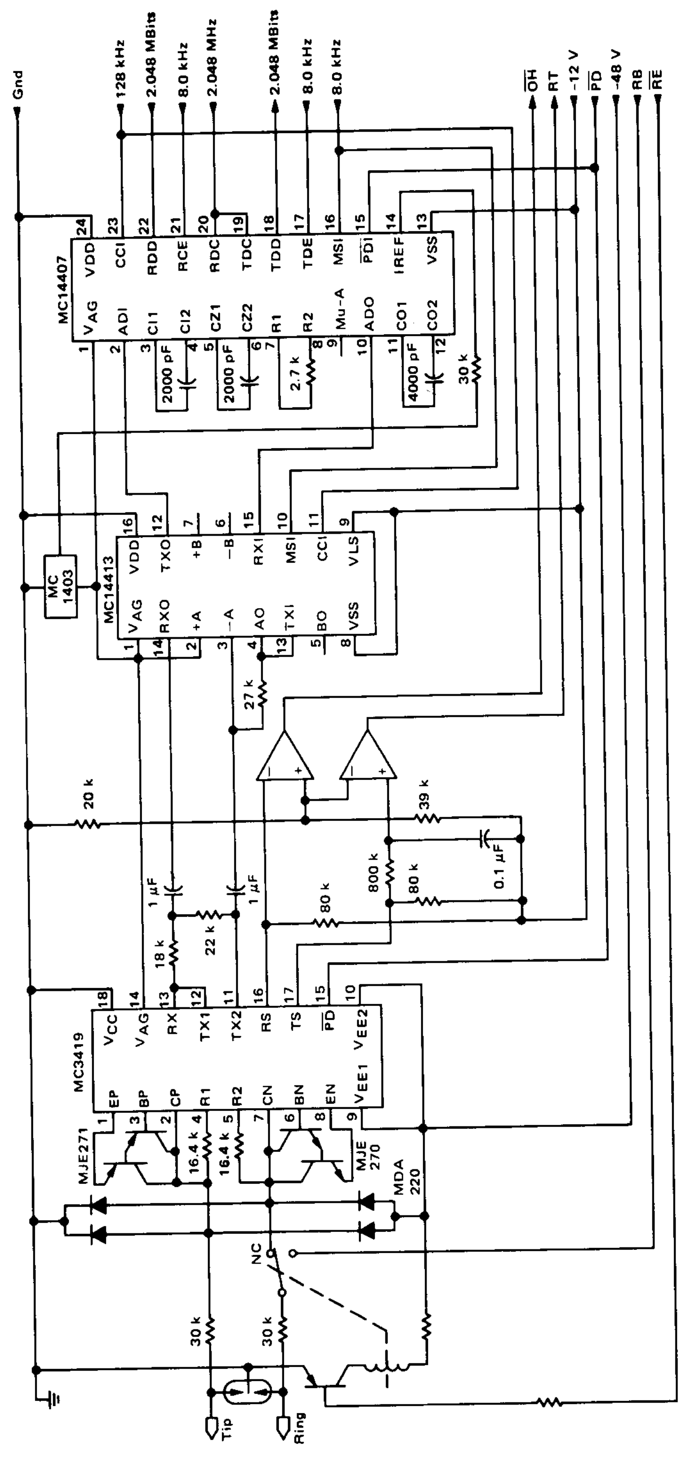

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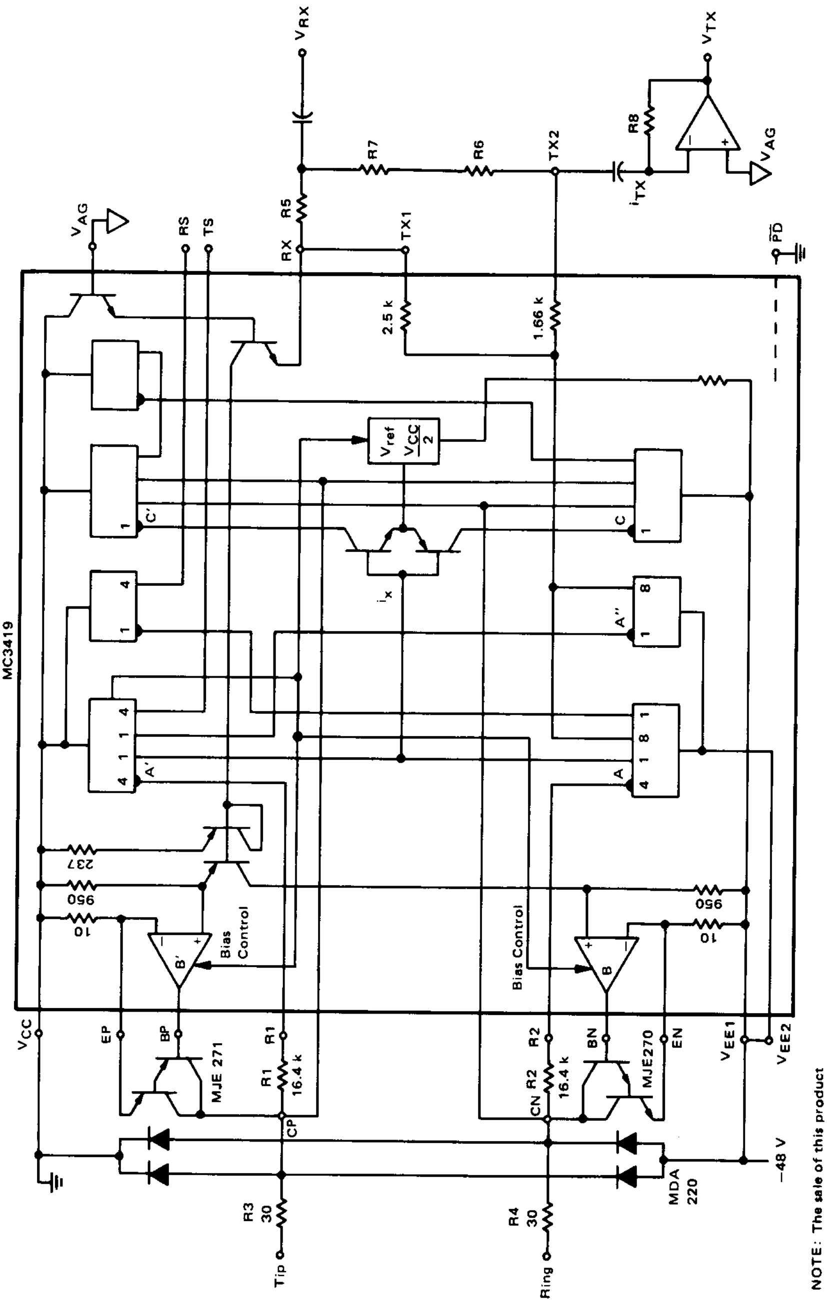
FIGURE 8 – SUBSCRIBER LOOP INTERFACE CIRCUIT, MC3419



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DESCRIPTION OF MC3419 SUBSCRIBER LOOP INTERFACE CIRCUIT

Figure 8 depicts a complete subscriber loop interface circuit for standard end-office telephone loop connections. The circuit consists of an 18 pin dual in-line MC3419, MJE271 PNP and MJE270 NPN power darlington transistors, an MDA220 bridge rectifier and six resistors. This composite circuit provided the following line interface functions:

1. 2-wire balanced to 4-wire single-ended signal conversion.
2. Independent Receive Gain selection (R5).
3. Independent Transmit Gain selection (R8).
4. Independent Transhybrid null selection (R6 + R7)*
5. 600 to 900 Ω resistance ac loop termination (R1, R2, R3, R4)*.
6. Resistive dc power-feed from 400 to 800 Ω (R1, R2, R3, R4).
7. Ring to ground, Tip to ground, Ring and Tip to ground fault current limiting (10 mA).
8. Rejection of longitudinal or common mode interference from 50 to 3400 Hz (30 mA RMS).
9. 1500 volt secondary lightning protection.
10. Temporary power line fault protection.
11. Proportional ring current sense indication in RS.
12. Proportional tip current sense indication in TS.
13. Suppression of longitudinal component in RS and TS normal connections.
14. Independent 4-wire common input for noise isolation.
15. Independent quiet battery supply input for battery noise rejection.
16. Near zero power dissipation in normal on-hook condition.
17. Level linearity of better than 0.1 dB over the entire level and frequency range.

*Reflected complex impedances may also be provided with an additional capacitor.

DC CHARACTERISTICS

The first function the SLIC must perform is to enable and disable itself on the basis of the switch-hook condition in the attached instrument. With the station on-hook, the Ring and Tip terminals are open. No metallic current can flow in resistors R1 and R2, thus the input and various outputs of circuit A and A' are zero. The control outputs of A and A' are off, causing the op amps B and B' and the voltage reference to have no bias. The reference pull down resistor pulls the reference voltage to V_{EE}. No current flows in any part of the circuit if the Tip and Ring terminals are open. The power dissipation in this state is back bias leakage only.

When a load resistance (R_L) is connected to Tip and Ring, the dc current flows in R1, R2, and circuits A and A', The control outputs, op amps B, B', and the voltage reference are now on. The current gain of circuit A and A' to the TX outputs is K2 = 4. The current gain of circuits B and B' is K1 = 23.75. For a current in R1 and R2 of I_N, the current in the collector of circuits B and B' is $K1K2I_N$. The total current in the load is $(1+K1K2)I_N$. The dc feed resistance at the Tip and Ring terminals is

$$R_f = \frac{(R1 + R2)}{1+K1K2} + R3 + R4$$

The current which flows in the load will be:

$$I_{Loop} = \frac{V_{CC} - V_{EE2}}{R_L + R_f}$$

The dc feed current is thus determined by the loop resistance.

The dc component of i_x is a measure of the mismatch between the source and the sink current of the various differential stages. Circuit C and C' source or sink current through CN and CP until the dc component of $i_x = 0$. C and C' also keep the mid-point voltage of the load at $V_{CC}/2$. Thus, with a metallic current in the load, the SLIC supplies current to the load with impedance R_f.

Various fault dc conditions must be accounted for in practice. The Tip and Ring leads can be shorted to ground in the field in any combination. The SLIC limits these fault currents by the arrangement of the control outputs of circuit A and A'. If the Ring lead is tied to ground, a current through R2 will turn on the control output of circuit A. This enables op amp B' and provides a sinking path for the voltage reference. If the Tip lead is open or connected to ground, the current in R1 is zero. The i_x control lead is sinking current but cannot turn on circuit C' because the voltage reference is V_{EE}. Circuit B is also off since the control output of circuit A' is off. The current in the Ring lead is now $[(V_{CC}-V_{EE})/(R4 + R2)]$. The Ring fault current in the SLIC is less than 10 mA.

SMALL SIGNAL AC CHARACTERISTICS

With a load R_L applied across Tip and Ring, the flow of metallic current in R_L enables and biases the SLIC circuit. Now consider an ac generator in series with R_L causing differential signal across Ring and Tip at a frequency between 300 and 3400 Hz. The impedance presented to the generator is $R_L + R_o$ where R_o is the ac input impedance of the SLIC at the two-wire part. R_o is derived by a method similar to R_f.

The gain of circuits A, A', B, and B' is K1 = 4 and K2 = 23.75 as before. However, the TX2 path to i_{TX} is an

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added load for ac signals and the current returned to R_X is divided by the current divider of 2.5 kΩ and 1.66 kΩ. As connected, the ratio of these resistors creates another constant K5 = 0.4. (TX1 and TX2 connection can be reversed to produce K5' = 0.6).

The ac termination is thus:

$$R_f = \frac{R1 + R2}{1+K1K2K5} + R3 + R4$$

The ac current in SLIC is then

$$i_g = \frac{v_g}{R_L + R_o} \text{ where } v_g \text{ is the generator voltage.}$$

The current in R1 and R2 is given by $\frac{i_g}{1+K1K2K5}$

and the output signal current is

$$i_{TX} = \frac{K1(1\text{-}K5)}{i_g\,(1+K1K2K5)} \quad \text{thus}$$

$$\frac{V_{TX}}{v_g} = \frac{K1(1\text{-}K5)}{1+K1K2K5}\left(\frac{R8}{R_L + R_o}\right)$$

The differential signal in the load is input, as two out of phase signals, into circuits A' and A. The A' signal is inverted and summed in phase with the output of A in A''. The transmit gain voltage of the SLIC can be set at any arbitrary value by selecting R8.

Now assume a two-wire load R_L and a generator v_g at V_{RX}. The generator sees a low impedance at R_X, assuming V_{AG} is connected to a dc potential.The current into R_X is simply $i_{RX} = v_g/R5$.

This current is multiplied by K1 in circuits B and B'. The output transistors drive a load R_L + R3 + R4 in parallel with (R1+R2)/(1+K1K2K5) so that the voltage gain from V_{RX} to Tip and Ring is

$$\frac{V_{RL}}{V_{RX}} = -K2\,\frac{R_L}{R5} \times C_1 \text{ where}$$

$$C_1 = \left[\frac{R1 + R2}{(R1+R2)+(R_L+R3+R4)(1+K1K2K5)}\right]$$

The signal current across the load is in phase with V_{RX} and out of phase with the termination R_o. The current in R_o causes a signal at i_{TX}.

This current may be cancelled for any load R_L by selecting the sum of (R6 + R7).

Balance is achieved for a load R_L by designing

$$(R6 + R7) = \frac{R5(1+K1K2K5)}{K1K2(1\text{-}K5)} \times C_2 \text{ where}$$

$$C_2 = \left[\frac{(R1+R2) + (R_L+R3+R4)(1+K1K2K5)}{R1 + R2}\right]$$

The current amplifiers within the SLIC are all wide-band amplifiers such that essentially no group delay occurs for 4 kHz band limited signals and resistive loads. Thus, the SLIC functions as a near ideal transimpedance converter for ports V_{RX},V_{RL}, and V_{TX}. Complex loads Z_L may be balanced by replacing (R6 + R7) with a complex balance network z.

LONGITUDINAL SIGNAL SUPPRESSION

Both low frequency and voice-band longitudinal rejection are produced by the same mechanisms within this SLIC.

A longitudinal interference from 0 to 3400 Hz in the loop produces a common mode voltage at Ring and Tip. Circuit A and A' sense these in phase currents in R1 and R2 and cause an ac signal i_x. Circuit C and C' are driven by the Class B transistor pair to produce currents which will reduce the common mode component at nodes CN and CP by the open loop ac gain of the circuit C and C'. The high compliance of the i_x output and a large current gain in circuit C and C' allow the open loop gain to be quite large.

Constants K1, K2 are held in close tolerance within the integrated circuit. If R1 + R3 = R2 + R4, then the longitudinal balance at Tip and Ring will be good. Thus, the remaining component of common mode signal at CP and CN will be equal. The phase inversion in A'' will cause the common mode remainder to sum out of phase at TX2 and thus will contribute little output at V_{TX}. The overall performance of this common mode rejection loop is determined by the matching of R1 + R3 and R4 + R2, as well as the matching of constants within the chip. 60 dB appears readily achievable.

The circuit C and C' outputs are limited to 30 mA to insure longitudinal capacity for both the IEEE and REA standards.

LOOP CONDITION SENSING

Three analog sensing outputs are provided for detecting the condition of the subscriber loop. Each output consists of the open collector of a current sourcing device. The RS and TS outputs are derived from the sense currents in circuits A and A'. Thus, in a normal metallic connection the TS and RS currents are related to Ring and Tip currents by constants.

DC Metallic

$$I_{RS} = \frac{I_R}{1+K1K2} = \frac{V_{CC}-V_{EE}}{(R_L + R_f)(1+K1K2)}$$

$$I_{TS} = \frac{I_T}{1+K1K2} = \frac{V_{CC}-V_{EE}}{(R_L+R_f)(1+K1K2)}$$

AC Metallic

$$i_{RS} = \frac{V_{RL}}{(R_L+R_o)(1+K1K2K5)}$$

$$i_{TS} = \frac{V_{RL}}{(R_L+R_o)(1+K1K2K5)}$$

Note that if the current has a metallic path from Tip to Ring, but also an unbalanced load to ground in Ring or Tip, that the RS current will be proportional to the Ring current and the TS current will be proportional to the Tip current. Second party detection and ground start detection can be handled using this feature. Providing a metallic path does exist, the longitudinal component in RS and TS will be suppressed in RS and TS by circuit C and C'. With no metallic connection, circuit B and B' are off such that the longitudinal impedance is R1 + R3 and the induced current from a given source will be decreased by 1 + K1K2. In this case, the longitudinal current will produce peak outputs at RS and TS which are less than the average output of a long-loop metallic current.

The longitudinal sense output provides a full-wave rectified current proportional to the longitudinal loop current once metallic connection has been established. Simple filtering of this lead can produce a dc measure of the longitudinal status of an operating loop. Excessive longitudinal current can produce a fault indication.

NOISE AND POWER SUPPLY REJECTION

The main 48-volt battery in a large office can supply considerable power but is often quite noisy and difficult to filter. Without a means of rejecting supply noise, the channel to channel crosstalk can also become excessive. In this SLIC, two V_{EE} pins are provided to allow for quiet battery and power battery connection. Circuits A and A' support the sensing resistors and control all other current in the SLIC. If the voltage across V_{CC} and V_{EE2} is filtered, noise at V_{CC} will not effect the performance of the loop. In a short circuit condition, the V_{EE} current will be about 130 mA while the V_{EE2} current is 3 mA. It is, therefore, possible to supply V_{EE2} from a far quieter supply.

Furthermore, an analog ground input (V_{AG}) is provided to allow for proper noise grounding for the V_{RX} and V_{TX} terminals. The true input signal is the ac voltage between V_{AG} and V_{RX}. The true output voltage should be taken between V_{AG} and V_{TX}.

PROTECTION

Two types of electrical hazards can be expected at the Ring and Tip terminals of the SLIC. Transient currents caused by electrical storms and power line cross connects during installation and maintenance. The diode bridge, coupled with R3 and R4, provide this protection. Ring and Tip are normally protected by a gas tube or carbon blocks against the primary effects of a near lightning strike. The SLIC itself must provide secondary protection for 1500-volt transients. A transient voltage at Ring or Tip will turn on one of the four diodes. The resistors limit the maximum current to 50 amps, which is the rated surge current of the diodes. A typical turn on time of 200 ns is readily achievable with silicon rectifiers.

Power line faults from 120-volt lines will be half-wave rectified by the upper and lower pair resulting in a current of 2 amp RMS in each with 30 ohm source resistors.

Extended short circuit conditions will cause R3 and R4 to burn open, eliminating the fault and causing no further damage. The externalization of the R3 and R4 resistors from the SLIC's feedback loop is a critical step in providing sufficient electrical hazard protection.