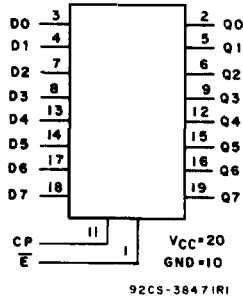


High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop with Data Enable

Type Features:

- Buffered common clock
- Buffered inputs
- Typical propagation delay = 17ns @ $C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$
- 60 MHz typical maximum clock frequency @ $V_{CC} = 5\text{V}$, $C_L = 15\text{pF}$, $T_A = 25^\circ\text{C}$

The RCA-CD54/74HC377 and CD54/74HCT377 are octal D-type flip-flops with a buffered clock (CP) common to all eight flip-flops. All the flip-flops are loaded simultaneously on the positive edge of the clock (CP) when the Data Enable (E) is LOW.

The CD54HC377 and CD54HCT377 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC377 and CD74HCT377 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

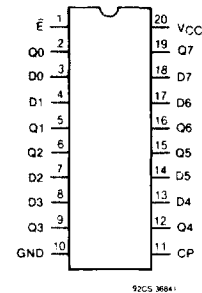
TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	E	Dn	Qn
Load "1"	↗	L	h	H
Load "0"	↗	L	L	L
Hold (do nothing)	↗	h	X	no change
	X	H	X	no change

- H = HIGH voltage level steady state.
- h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
- L = LOW voltage level steady state
- L = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
- X = Don't care.
- ↗ = LOW-to-HIGH clock transition.

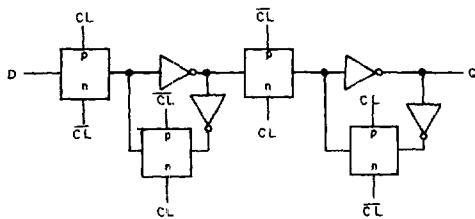
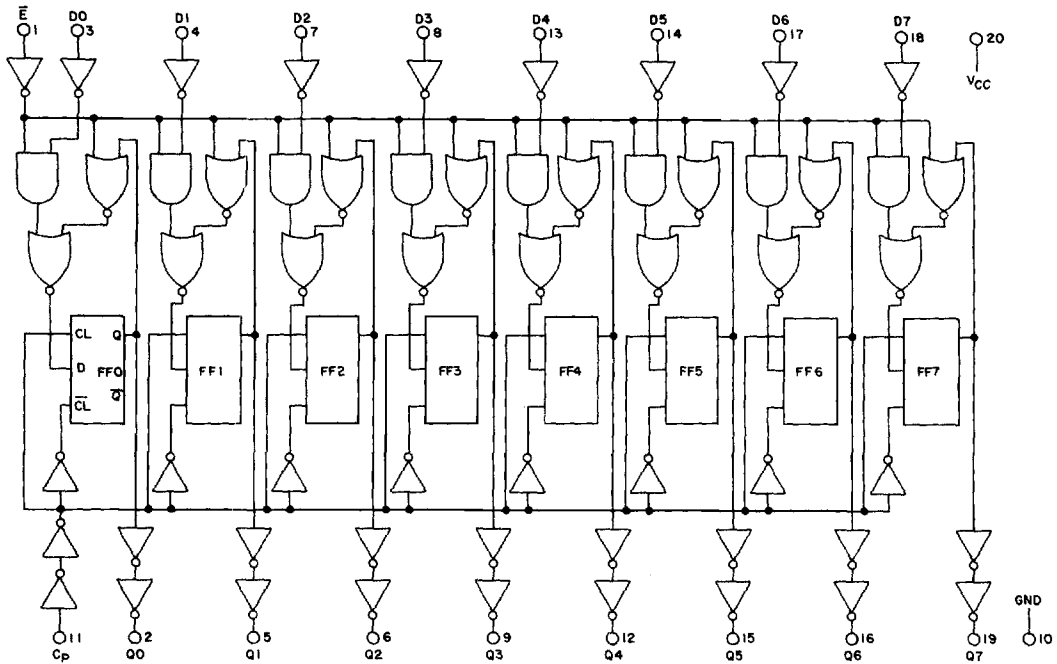
Family Features:

- Fanout (over temperature range):
Standard outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- Wide operating temperature range:
CD74HC/HCT: -40 to +85°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC types:
2 to 6 V operation
High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}
@ $V_{CC} = 5\text{V}$
- CD54HCT/CD74HCT types:
4.5 to 5.5 V operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8\text{V max.}$, $V_{IH} = 2\text{V min.}$
CMOS input compatibility
 $I_I \leq 1\ \mu\text{A}$ @ V_{OL} , V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC377
CD54/74HCT377



92CL-38576R1

Flip-Flop Detail

Fig. 1 - Logic diagram.

CD54/74HC377 CD54/74HCT377

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V _{CC}):	
(Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I _{IK} (FOR V _i < -0.5 V OR V _i > V _{CC} + 0.5V)	±20mA
DC OUTPUT DIODE CURRENT, I _{OK} (FOR V _o < -0.5 V OR V _o > V _{CC} + 0.5V)	±20mA
DC DRAIN CURRENT, PER OUTPUT (I _o) (FOR -0.5 V < V _o < V _{CC} + 0.5V)	±25mA
DC V _{CC} OR GROUND CURRENT (I _{CC})	±50mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60° C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +100° C (PACKAGE TYPE F, H)	500 mW
For T _A = +100 to +125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -40 to +70° C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125° C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPE F, H	-55 to +125° C
PACKAGE TYPE E, M	-40 to +85° C
STORAGE TEMPERATURE (T _{stg})	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)	
with solder contacting lead tips only	+300° C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range) V _{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V _i , V _o	0	V _{CC}	V
Operating Temperature T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t _r , t _f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC377 CD54/74HCT377

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC377/CD54HC377										CD74HCT377/CD54HCT377										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE			
	V_i V	I_o mA	V_{cc} V	+25° C			-40/ +85° C		-55/ +125° C		V_i V	V_{cc} V	+25° C			-40/ +85° C		-55/ +125° C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{ih}			2	1.5	—	—	1.5	—	1.5	—	—	4.5								V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—		
			6	4.2	—	—	4.2	—	4.2	—	—	5.5									
Low-Level Input Voltage V_{il}			2	—	—	0.5	—	0.5	—	0.5	—	4.5								V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	—	to	—	—	0.8	—	0.8	—	0.8	
			6	—	—	1.8	—	1.8	—	1.8	—	—	5.5								
High-Level Output Voltage V_{oh}	V_{ik} or V_{ih}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{ik} or V_{ih}	4.5	4.4	—	—	4.4	—	4.4	—	V	
CMOS Loads			4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	4.4	—	—	4.4	—	4.4	—		
			6	5.9	—	—	5.9	—	5.9	—	V_{ih}										
TTL Loads	V_{ik} or V_{ih}	-4 -5.2	4.5	3.98	—	—	3.84	—	3.7	—	V_{ik} or V_{ih}	4.5	3.98	—	—	3.84	—	3.7	—	V	
Low-Level Output Voltage V_{ol}	V_{ik} or V_{ih}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{ik} or V_{ih}	4.5	—	—	0.1	—	0.1	—	0.1	V	
CMOS Loads			4.5	—	—	0.1	—	0.1	—	0.1	or	4.5	—	—	0.1	—	0.1	—	0.1		
			6	—	—	0.1	—	0.1	—	0.1	V_{ih}										
TTL Loads	V_{ik} or V_{ih}	4 5.2	4.5	—	—	0.26	—	0.33	—	0.4	V_{ik} or V_{ih}	4.5	—	—	0.26	—	0.33	—	0.4	V	
Input Leakage Current I_i	V_{cc} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{cc} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current I_{cc}	V_{cc} or Gnd	0	6	—	—	8	—	80	—	160	V_{cc} or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{cc}^*											$V_{cc}-2.1$ to 5.5	4.5	—	100	360	—	450	—	490	μA	

*For dual-supply systems theoretical worst case ($V_i = 2.4$ V, $V_{cc} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
\bar{E}	1.5
CP	0.5
All Dn Inputs	0.25

*Unit Load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25° C.

CD54/74HC377 CD54/74HCT377

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	C_L (pF)	SYMBOL	TYPICAL		UNITS
			HC	HCT	
Maximum Clock Frequency	15	f_{max}	60	50	MHz
Propagation Delay CP \longrightarrow Q	15	t_{PLH} t_{PHL}	14	16	ns
Power Dissipation Capacitance*	—	C_{PD}	31	35	pF

* C_{PD} is used to determine the dynamic power consumption, per flip flop.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) \text{ where:}$$

f_i = input frequency

f_o = output frequency

C_L = output load capacitance.

V_{CC} = supply voltage.

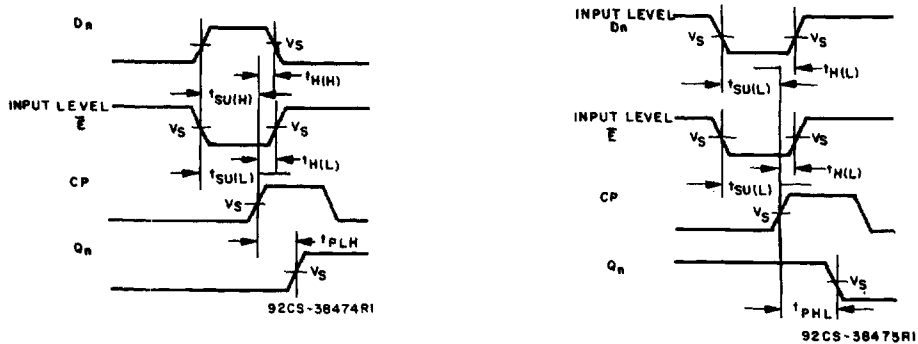
PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Clock Frequency f_{max}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	25	—	25	—	20	—	20	—	16	—	
	6	35	—	—	—	29	—	—	—	23	—	—	—	
Clock Pulse width t_w	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	20	—	20	—	25	—	24	—	30	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time \bar{E} , Data to CP t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
	4.5	12	—	12	—	15	—	15	—	18	—	18	—	
	6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time, Data to CP t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
	4.5	3	—	3	—	3	—	3	—	3	—	3	—	
	6	3	—	—	—	3	—	—	—	3	—	—	—	
Hold Time \bar{E} to CP t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	ns
	4.5	5	—	5	—	5	—	5	—	5	—	5	—	
	6	5	—	—	—	5	—	—	—	5	—	—	—	

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, CP to Q t_{PLH} t_{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	4.5	—	35	—	38	—	44	—	48	—	53	—	57	
	6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition Time t_{TLH} t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_i		—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC377
CD54/74HCT377



	54/74HC	54/74HCT
Input Level	V _{CC}	3V
Switching Voltage, V _S	50% V _{CC}	1.3 V

Fig. 2 - Setup and hold times and propagation delay times.