

# Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

**MPC9993**



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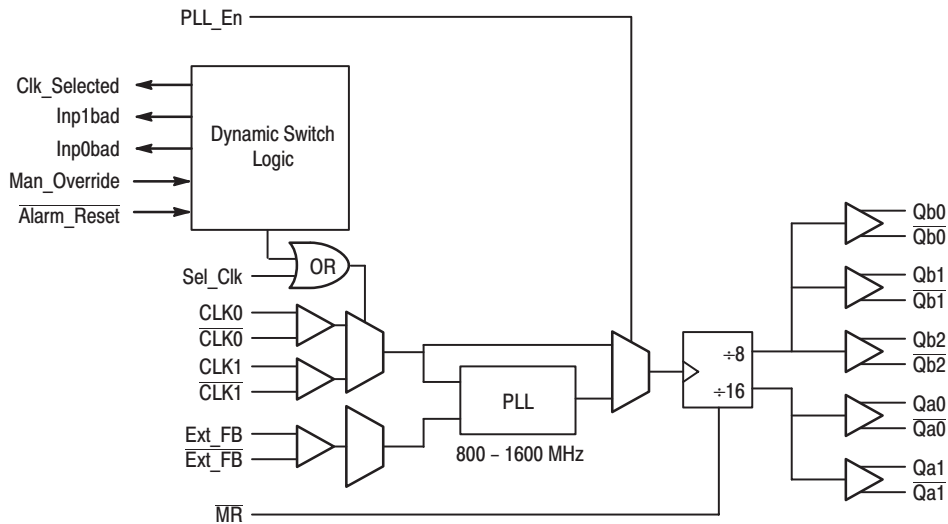
The MPC9993 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 2x, phase aligned clock outputs.

**Features:**

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3V Operation
- 32-Lead LQFP Packaging

**Functional Description**

The MPC9993 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP\_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).



**Figure 1. Block Diagram**

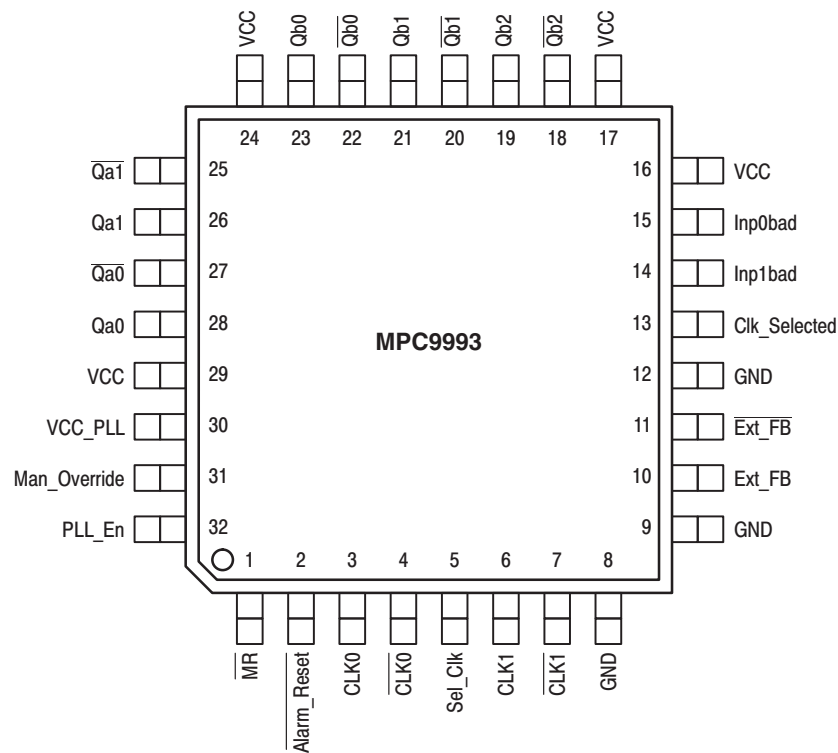


Figure 2. 32-Lead Pinout (Top View)

## PIN DESCRIPTIONS

Pin Name	I/O	Pin Definition
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa0:1, $\overline{\text{Qa0:1}}$	LVPECL Output	Differential 1x output pairs
Qb0:2, $\overline{\text{Qb0:2}}$	LVPECL Output	Differential 2x output pairs
Inp0bad	LVC MOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Inp1bad	LVC MOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Clk_Selected	LVC MOS Output	'0' if clock 0 is selected, '1' if clock 1 is selected
$\overline{\text{Alarm\_Reset}}$	LVC MOS Input	'0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is "one-shotted" (50k $\Omega$ pullup)
Sel_Clk	LVC MOS Input	'0' selects CLK0, '1' selects CLK1 (50k $\Omega$ pulldown)
Manual_Override	LVC MOS Input	'1' disables internal clock switch circuitry (50k $\Omega$ pulldown)
PLL_En	LVC MOS Input	'0' bypasses selected input reference around the phase-locked loop (50k $\Omega$ pullup)
$\overline{\text{MR}}$	LVC MOS Input	'0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50k $\Omega$ pullup)
VCCA	Power Supply	PLL power supply
VCC	Power Supply	Digital power supply
GND A	Power Supply	PLL ground
GND	Power Supply	Digital ground

**Table 1. ABSOLUTE MAXIMUM RATINGS<sup>a</sup>**

Symbol	Characteristics	Min	Max	Unit	Condition
V <sub>CC</sub>	Supply Voltage	-0.3	3.9	V	
V <sub>IN</sub>	DC Input Voltage	-0.3	V <sub>CC</sub> +0.3	V	
V <sub>OUT</sub>	DC Output Voltage	-0.3	V <sub>CC</sub> +0.3	V	
I <sub>IN</sub>	DC Input Current		±20	mA	
I <sub>OUT</sub>	DC Output Current		±50	mA	
T <sub>S</sub>	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 2. GENERAL SPECIFICATIONS**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V <sub>TT</sub>	Output termination voltage		V <sub>CC</sub> - 2		V	
MM	ESD Protection (Machine model)	175			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model)	1000			V	
LU	Latch-up immunity	100			mA	
C <sub>IN</sub>	Input Capacitance		4.0		pF	Inputs
θ <sub>JA</sub>	Thermal resistance junction to ambient JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ <sub>JC</sub>	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T <sub>J</sub>	Operating junction temperature <sup>a</sup> (continuous operation) MTBF = 9.1 years			110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9993 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9993 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

**Table 3. DC CHARACTERISTICS** ( $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ$  to  $+85^\circ\text{C}$ )

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ( $\overline{MR}$ , PLL_En, Sel_Clk, Man_Override, Alarm_Reset)						
$V_{IH}$	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
$V_{IL}$	Input Low Voltage			0.8	V	
$I_{IN}$	Input Current <sup>a</sup>			$\pm 100$	$\mu\text{A}$	$V_{IN}=V_{CC}$ or GND
LVCMOS control outputs (Clk_selected, Inp0bad, Inp1bad)						
$V_{OH}$	Output High Voltage	2.0			V	$I_{OH}=-24$ mA
$V_{OL}$	Output Low Voltage			0.55	V	$I_{OL}= 24$ mA
LVPECL clock inputs (CLK0, CLK1, Ext_FB) <sup>b</sup>						
$V_{PP}$	DC Differential Input Voltage <sup>c</sup>	0.1		1.3	V	Differential operation
$V_{CMR}$	Differential Cross Point Voltage <sup>d</sup>	$V_{CC}-1.8$		$V_{CC}-0.3$	V	Differential operation
$I_{IN}$	Input Current <sup>a</sup>			$\pm 100$	$\mu\text{A}$	$V_{IN}=V_{CC}$ or GND
LVPECL clock outputs (QA[1:0], QB[2:0])						
$V_{OH}$	Output High Voltage	$V_{CC}-1.20$	$V_{CC}-0.95$	$V_{CC}-0.70$	V	Termination $50\Omega$ to $V_{TT}$
$V_{OL}$	Output Low Voltage	$V_{CC}-1.90$	$V_{CC}-1.75$	$V_{CC}-1.45$	V	Termination $50\Omega$ to $V_{TT}$
Supply Current						
$I_{GND}$	Maximum Power Supply Current			180	mA	GND pins
$I_{CC\_PLL}$	Maximum PLL Supply Current			15	mA	$V_{CC\_PLL}$ pin

- a. Inputs have internal pull-up/pull-down resistors affecting the input current.
- b. Clock inputs driven by differential LVPECL compatible signals.
- c.  $V_{PP}$  is the minimum differential input voltage swing required to maintain AC characteristics.
- d.  $V_{CMR}$  (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the  $V_{CMR}$  (DC) range and the input swing lies within the  $V_{PP}$  (DC) specification.

**Table 4. AC Characteristics** ( $V_{CC} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )<sup>a</sup>

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
$f_{ref}$	Input Reference Frequency +16 feedback	50		100	MHz	PLL locked
$f_{VCO}$	VCO Frequency Range <sup>b</sup> +16 feedback	800		1600	MHz	
$f_{MAX}$	Output Frequency QA[1:0] QB[2:0]	50 100		100 200	MHz MHz	PLL locked
$f_{refDC}$	Reference Input Duty Cycle	25		75	%	
$t(\phi)$	Propagation Delay SPO, static phase offset <sup>c</sup> CLK0, CLK1 to any Q	-2.0 0.9		+2.0 1.8	ns ns	PLL_EN=1 PLL_EN=0
$V_{PP}$	Differential input voltage <sup>d</sup> (peak-to-peak)	0.25		1.3	V	
$V_{CMR}$	Differential input crosspoint voltage <sup>e</sup>	$V_{CC}-1.7$		$V_{CC}-0.3$	V	
$t_{sk(O)}$	Output-to-output Skew within QA[2:0] or QB[1:0] within device			50 80	ps ps	
$\Delta_{per/cycle}$	Rate of change of period QA[1:0] <sup>f</sup> QB[2:0] <sup>f</sup> QA[1:0] <sup>g</sup> QB[2:0] <sup>g</sup>		20 10 200 100	50 25 400 200	ps ps ps ps	
DC	Output Duty Cycle	45	50	55	%	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter RMS (1 $\sigma$ )			47	ps	
$t_{LOCK}$	Maximum PLL Lock Time			10	ms	
$t_r, t_f$	Output Rise/Fall Time	0.05		0.70	ns	20% to 80%

- a. AC characteristics apply for parallel output termination of  $50\Omega$  to  $V_{CC} - 2V$ .
- b. The input reference frequency must match the VCO lock range divided by the feedback divider ratio (FB):  $f_{ref} = f_{VCO} \div FB$ .
- c. CLK0, CLK1 to Ext\_FB.
- d.  $V_{PP}$  is the minimum differential input voltage swing required to maintain AC characteristics including SPO and device-to-device skew. Applicable to CLK0, CLK1 and Ext\_FB.
- e.  $V_{CMR}$  (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the  $V_{CMR}$  (AC) range and the input swing lies within the  $V_{PP}$  (AC) specification. Violation of  $V_{CMR}$  (AC) or  $V_{PP}$  (AC) impacts the SPO, device and part-to-part skew. Applicable to CLK0, CLK1 and Ext\_FB.
- f. Specification holds for a clock switch between two input signals (CLK0, CLK1) no greater than 400 ps out of phase. Delta period change per cycle is averaged over the clock switch excursion.
- g. Specification holds for a clock switch between two input signals (CLK0, CLK1) at any phase difference ( $\pm 180^\circ$ ). Delta period change per cycle is averaged over the clock switch excursion.

## APPLICATIONS INFORMATION

The MPC9993 is a dual clock PLL with on-chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

### Definitions

**primary clock:** The input CLK selected by Sel\_Clk.

**secondary clock:** The input CLK NOT selected by Sel\_Clk.

**PLL reference signal:** The CLK selected as the PLL reference signal by Sel\_Clk or IDCS. (IDCS can override Sel\_Clk).

### Status Functions

**Clk\_Selected:** Clk\_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk\_Selected (H) indicates CLK1 is selected as the PLL reference signal.

**INP\_BAD:** Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext\_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of Alarm\_Reset.

### Control Functions

**Sel\_Clk:** Sel\_Clk (L) selects CLK0 as the primary clock. Sel\_Clk (H) selects CLK1 as the primary clock.

**Alarm\_Reset:** Asserted by a negative edge. Generates a one-shot reset pulse that clears INPUT\_BAD latches and Clk\_Selected latch.

**PLL\_En:** While (L), the PLL reference signal is substituted for the VCO output.

**MR:** While (L), internal dividers are held in reset which holds all Q outputs LOW.

### Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk\_Selected) will always be the CLK selected by Sel\_Clk. The status function INP\_BAD is active in Man Override (H) and (L).

### Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP\_BAD (H) status flag and select the other input as the Clk\_Selected for the PLL reference clock. Once latched, the Clk\_Selected and INP\_BAD remain latched until assertion of Alarm\_Reset which clears all latches (INP\_BADs are cleared and Clk\_Selected = Sel\_Clk). NOTE: If both CLKs are bad when Alarm\_Reset is asserted, both INP\_BADs will be latched (H) after one Ext\_FB period and Clk\_Selected will be

latched (L) indicating CLK0 is the PLL reference signal. While neither INP\_BAD is latched (H), the Clk\_Selected can be freely changed with Sel\_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext\_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC9993's, the following procedure should be used. Assuming that the input CLKs to all MPC9993's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC9993 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

### Hot insertion and withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC9993 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

### Acquiring Frequency Lock

1. While the MPC9993 is receiving a valid CLK signal, assert Man\_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm\_Reset to reset Input Bad flags.
4. De-assert Man\_Override LOW to enable Intelligent Dynamic Clock Switch mode.

