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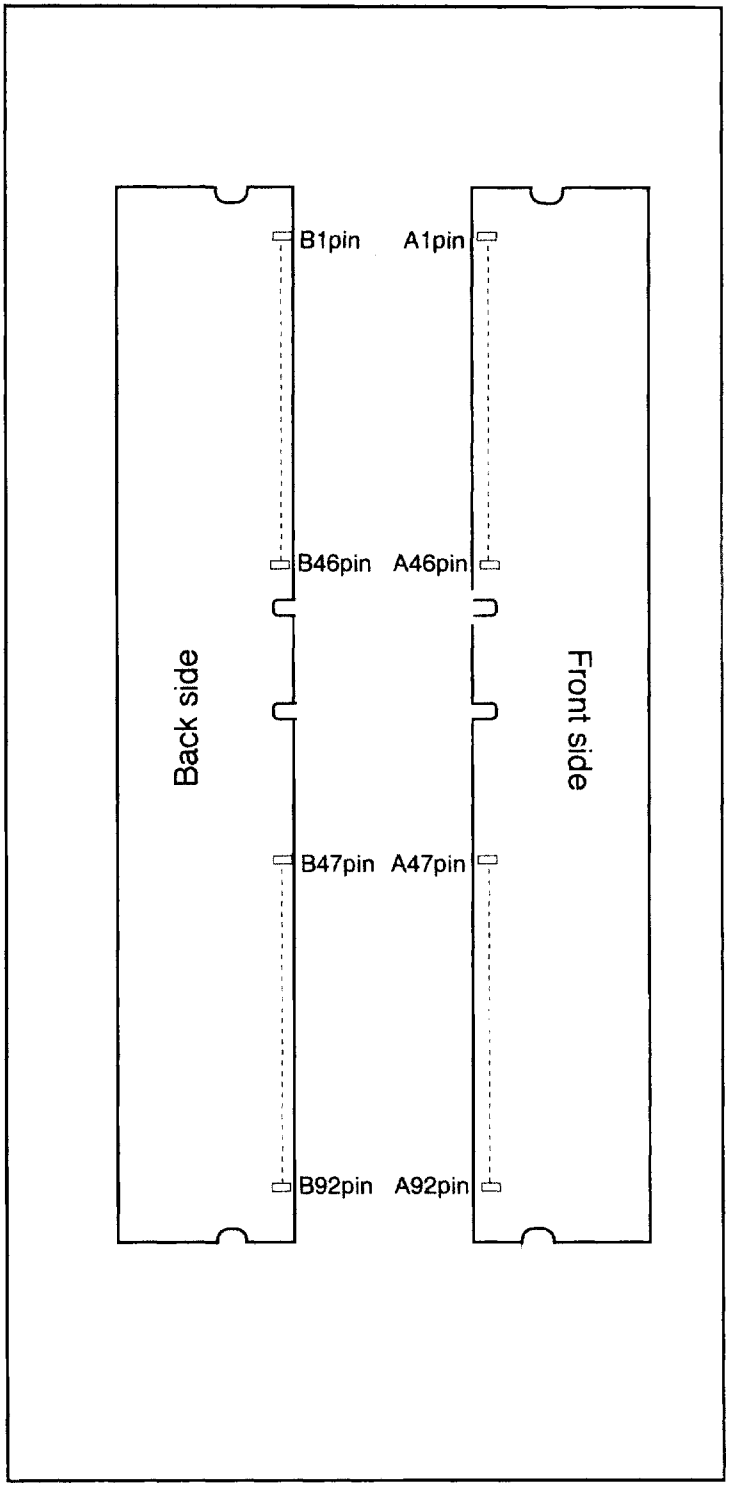
MH32/64R18BUP-408,458,536

DESCRIPTION

The MH32/64R18BUP is the Direct Rambus™ RIMM™ module. This consists of eight/sixteen industry 4Mx18 Direct Rambus DRAM(Direct RDRAM™) in M-CSP and one industory standard EEPROM in TSSOP and heatspreader.

The use of Rambus Signaling Level (RSL) technology permits 600MHz or 800MHz transfer rates while using conventional system and board design technologies.Direct RDRAM™ devices are capable of sustained data transfers at 1.25ns per two bytes (10 ns per sixteen bytes).

This is a socket type - memory modules, suitable for easy interchange or addition of modules.



FEATURES

	Data transfer rate	tRAC
-408	800MHz	40ns
-458	800MHz	45ns
-536	600MHz	53ns

- Utilizes industry 4Mx18Direct RDRAM™ M-CSP and industry standard EEPROM in TSSOP and Heatspreadar.
- 184-pin (92-pin dual in-line package)
- 2.5V±5% power supply
- Data transfer rate 600/800MHz
- Fully synchronous operation referenced to clock rising and fall edge
- 64/128MByte Direct RDRAM™ storage.
- Card Size: 133.35mm x 34.93mm x 1.27mm
- Heatspreadar on module
- Each RDRAM has 16banks.
- Low power and powerdown self refresh modes
- Separete Row and Column buses for higher efficiency
- RDRAM and module design conform to Rambus specification.
- Serial Presence Detect support

APPLICATION

PC main memory

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Pin	Pin Name	Pin	Pin Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTMN	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTM	B14	NC
A15	Gnd	B15	Gnd
A16	NC	B16	LROW2
A17	Gnd	B17	Gnd
A18	LROW1	B18	LROW0
A19	Gnd	B19	Gnd
A20	LCOL4	B20	LCOL3
A21	Gnd	B21	Gnd
A22	LCOL2	B22	LCOL1
A23	Gnd	B23	Gnd
A24	LCOL0	B24	LDQB0
A25	Gnd	B25	Gnd
A26	LDQB1	B26	LDQB2
A27	Gnd	B27	Gnd
A28	LDQB3	B28	LDQB4
A29	Gnd	B29	Gnd
A30	LDQB5	B30	LDQB6
A31	Gnd	B31	Gnd
A32	LDQB7	B32	LDQB8
A33	Gnd	B33	Gnd
A34	LSCK	B34	LCMD
A35	V_{CMOS}	B35	V_{CMOS}
A36	SOUT	B36	SIN
A37	V_{CMOS}	B37	V_{CMOS}
A38	NC	B38	NC
A39	Gnd	B39	Gnd
A40	NC	B40	NC
A41	V_{DD}	B41	V_{DD}
A42	V_{DD}	B42	V_{DD}
A43	NC	B43	NC
A44	NC	B44	NC
A45	NC	B45	NC
A46	NC	B46	NC

Pin	Pin Name	Pin	Pin Name
A47	NC	B47	NC
A48	NC	B48	NC
A49	NC	B49	NC
A50	NC	B50	NC
A51	V_{REF}	B51	V_{REF}
A52	Gnd	B52	Gnd
A53	SCL	B53	SA0
A54	V_{DD}	B54	V_{DD}
A55	SDA	B55	SA1
A56	SV_{DD}	B56	SV_{DD}
A57	SWP	B57	SA2
A58	V_{DD}	B58	V_{DD}
A59	RSCK	B59	RCMD
A60	Gnd	B60	Gnd
A61	RDQB7	B61	RDQB8
A62	Gnd	B62	Gnd
A63	RDQB5	B63	RDQB6
A64	Gnd	B64	Gnd
A65	RDQB3	B65	RDQB4
A66	Gnd	B66	Gnd
A67	RDQB1	B67	RDQB2
A68	Gnd	B68	Gnd
A69	RCOL0	B69	RDQB0
A70	Gnd	B70	Gnd
A71	RCOL2	B71	RCOL1
A72	Gnd	B72	Gnd
A73	RCOL4	B73	RCOL3
A74	Gnd	B74	Gnd
A75	RROW1	B75	RROW0
A76	Gnd	B76	Gnd
A77	NC	B77	RROW2
A78	Gnd	B78	Gnd
A79	RCTM	B79	NC
A80	Gnd	B80	Gnd
A81	RCTMN	B81	RCFMN
A82	Gnd	B82	Gnd
A83	RDQA0	B83	RCFM
A84	Gnd	B84	Gnd
A85	RDQA2	B85	RDQA1
A86	Gnd	B86	Gnd
A87	RDQA4	B87	RDQA3
A88	Gnd	B88	Gnd
A89	RDQA6	B89	RDQA5
A90	Gnd	B90	Gnd
A91	RDQA8	B91	RDQA7
A92	Gnd	B92	Gnd

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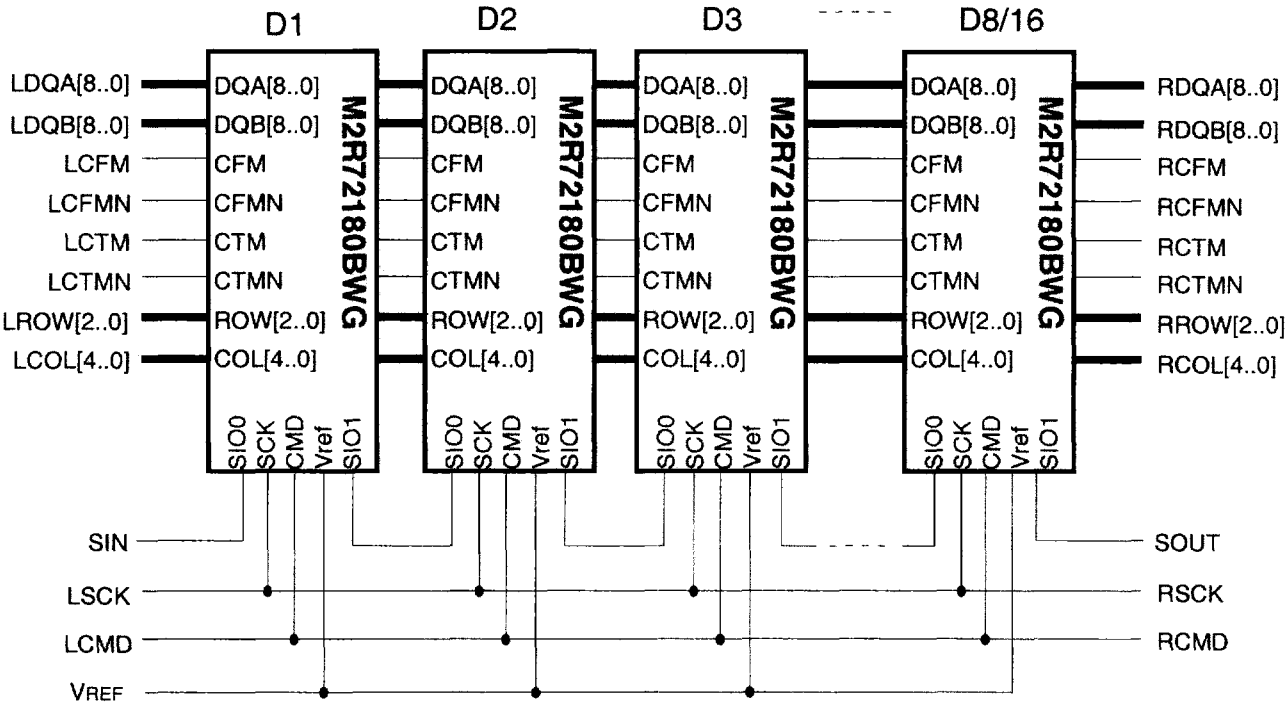
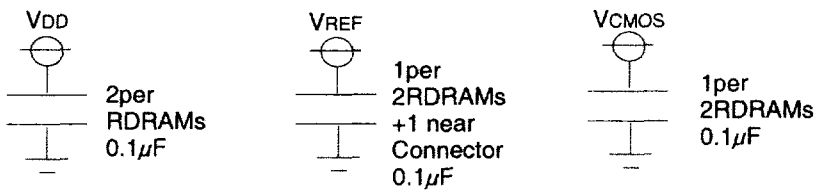
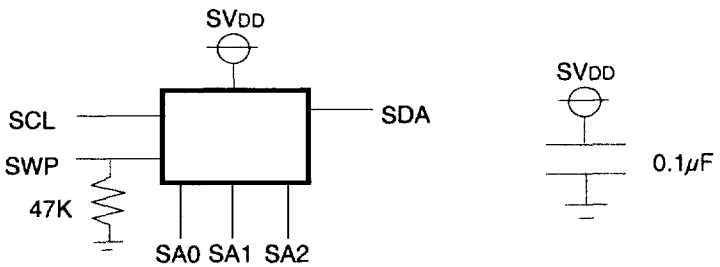
Block Diagram

MH32R18BUP=D1....D8 , MH64R18BUP=D1....D16





Serial Presence Detect



PIN FUNCTION

Signal	I/O	Type	Description
LCFM RCFM	input	RSL	Clock from master.Interface clock used for receiving RSL signals from the Channel.Positive polarity.
LCFMN RCFMN	input	RSL	Clock from master.Interface clock used for receiving RSL signals from the Channel.Negative polarity.
LCTM RCTM	input	RSL	Clock to master.Interface clock used for transmitting RSL signals to the Channel.Pogitive polarity.
LCTMN RCTMN	input	RSL	Clock to master.Interface clock used for transmitting RSL signals to the Channel.Negative polarity.
LCMD RCMD	input	VCMOS	Serial Command Pin used to read from and write to the control registers.Also used for power management.
LCOL4..0 RCOL4..0	input	RSL	Column bus.5-pin bus containing control and address information for colum accesses.
LROW2..0 RROW2..0	input	RSL	Row bus.3-pin bus containing control and address information for row accesses.
LDQA8..0 LDQB8..0 RDQA8..0 RDQB8..0	input/output	RSL	Data bus.9-pin bus carrying a byte of read or write data between the Channel and the RDRAM.
SIN	input/output	VCMOS	Serial I/O. Pin for reading from and writing to the control registers.Attaches to SIO0 of the first RDARM on the module.
SOUT	input/output	VCMOS	Serial I/O. Pin for reading from and writing to the control registers.Attaches to SIO1 of the last RDARM on the module.
LSCK RSCK	input	VCMOS	Clock input.Pin used to read from and write to the control registers.
SA2..0	input	SVDD	Serial Presence Detect Addresses.
SDA	input/output	SVDD	Serial Presence Detect Data (Open Collector I/O)
SCL	input	SVDD	Serial Presence Detect Clock.
SWP	input	SVDD	Serial Presence Detect Write Protect (active high). When low,the SPD can be written as well as read.
VDD			Supply voltage for the RDRAM core and interface logic.
VREF			Logic threshold reference voltage for RSL signals.
VCMOS			CMOS I/O Voltage.Used for signals CMD, SCK, SIN, SOUT.
SVDD			SPD voltage.Used for signalsSCL,SDA,SWE,SA2..0.
Gnd			Ground reference for RDRAM core and interface.

Absolute Maximum Rating (module level)

Symbol	Parameter and Conditions	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to Gnd	-0.3	V_{DD}+0.3	V
$V_{DD,ABS}$	Voltage on V_{DD} with respect to Gnd	-0.5	V_{DD}+1.0	V
T_{STORE}	Storage temperature	-50	100	°C

DC Recommended Electrical Conditions (module level)

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O pin power supply - for 2.5V controllers	2.5 - 0.13	2.5 + 0.25	V
	CMOS I/O pin power supply - for 1.8V controllers	1.8 - 0.1	1.8 + 0.2	
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	V
V_{IL}	RSL input low voltage	V_{REF} - 0.5	V_{REF} - 0.2	V
V_{IH}	RSL input high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL,CMOS}$	CMOS input low voltage	-0.3	0.5V_{CMOS} - 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	0.5V_{CMOS} + 0.25	V_{CMOS} + 0.3	V
$V_{OL,CMOS}$	CMOS output low voltage@ $I_{OL,CMOS}$ = 1mA		0.3	V
$V_{OH,CMOS}$	CMOS output high voltage@ $I_{OH,CMOS}$ = -0.25mA	V_{CMOS} - 0.3		V
I_{REF}	V_{REF} current@ $V_{REF,MAX}$	-160	160	μA
$I_{SCK,CMD}$	CMOS input leakage current @ (0≤V_{CMOS}≤V_{DD})	-160	160	μA
$I_{SIN,SOUT}$	CMOS input leakage current @ (0≤V_{CMOS}≤V_{DD})	-10.0	10.0	μA

AC Electrical Specifications (module level)

Symbol	Parameter and Conditions	Min	Max	Unit
Z	Module Impedance	25.2	30.8	Ohms
T_{PD}	Propagation Delay,all RSL signals	-	2.1	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to an average clock delay*	-0.01	0.01	ns
$\Delta T_{PD\ CMOS}$	Propagation delay variation of SCK and CMD signals with respect to an average clock delay*	-0.1	0.1	ns
V_a/V_{IN}	Attenuation Limit		13.5	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input risetime 20% - 80%)		0.8	%
V_{XB}/V_{IN}	Backward crosstalk cofficient (300ps input risetime 20% - 80%)		1	%

* Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM,CTMN,CFM,and CFMN)

I_{DD} - V_{DD} Supply Current Profile (module level)

I_{DD}	RIMM module power test conditions		MH32R-MAX	MH64R-MAX	Unit
I_{DD1}	All RDRAMs in powerdown,self-reflesh mode		TBD		mA
I_{DD2}	All RDRAMs in NAP mode		TBD		
I_{DD3}	All RDAMs in Stanby mode,no commands	-xx6	TBD	TBD	
		-xx8	TBD	TBD	
I_{DD4}	All RDRAMs in Active mode,no command	-xx6	TBD	TBD	
		-xx8	TBD	TBD	
I_{DD5}	All RDRAMs running reflesh cycles,with t_{RC} = $t_{RC,MIN}$	-xx6	TBD	TBD	
		-xx8	TBD	TBD	
I_{DD6}	All RDRAMs running reflesh cycles,with t_{RC} = t_{REF},# of rows	-xx6	TBD	TBD	
		-xx8	TBD	TBD	
I_{DD7}	One RDRAM cycling t_{RC} = min,1bank,no COL packats, remainder of RDRAMs in Stanby	-xx6	TBD	TBD	
		-xx8	TBD	TBD	
I_{DD8}	One RDRAM cycling t_{RC} = min,1 bank,two dualocts per active (32-byte transfers),remainder of RDRAMs in Stanby	-xx6	TBD	TBD	
		-xx8	TBD	TBD	
I_{DD9}	One RDRAM burst read/write,1 bank,open,full bandwidth,COL address changing every dualoct,remainder of RDRAMs in Stanby	-xx6	TBD	TBD	
		-xx8	TBD	TBD	

I_{CMOS} - V_{CMOS} Supply Current Profile (module level)

Symbol	RIMM module power test conditions	Max	Unit
I_{CMOS1}	Current when RDRAMs are in powerdown,self-refresh state	TBD	mA
I_{CMOS2}	Current when CMOS pins are used for register read/write operations(f=1MHz)	TBD	
I_{CMOS3}	Current when CMOS pins are used for power management operations(f=100MHz)	TBD	

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Timing Parameters (device level)

parameter	Description		Min	Max	Unit
tRC	Row Cycle time of RDRAM banks -the interval between ROWA packets with ACT commands to the same bank.		28	-	tCYCLE
tRAS	RAS - asserted time of RDRAM banks - the interval between ROWA packet with ACT command and next ROWR packet with PRER command to the same bank.		20	-	
tRP	ROWPrecharge time of RDRAM banks - the interval between ROWR packet with PRER* command and next ROWA packet with ACT command to the same bank.		8	-	
tPP	Precharge-to-precharge time of RDRAM device - the interval between successive ROWR packets with PRER* commands to any banks of the same device.		8	-	
tRR	RAS - to - RAS time of RDRAM device - the interval between successive ROWA packets with ACT commands to any banks of the same device.		8	-	
tRCD	RAS - to - CAS Delay - the interval from ROWA packet with ACT command to COLC packet with RD or WR command). Note - the RAS - to -CAS delay seen by the RDRAM core ($t_{RCD,CORE}$) is equal to $t_{RCD,CORE} = 1 + t_{RCD}$ because of differences in the row and column paths through the RDRAM interface.	-408 -536	7	-	
		-458	9	-	
tCAC	CAS Access delay - the minimum interval from RD command to Q read data.		8	12	
tCWD	CAS Write Delay - interval from WR command to D write data.		6	6	
tCC	CAS - to - CAS time of RDRAM bank - the interval between successive COLC commands.		4	4	
tPACKET	Length of ROWA,ROWR,COLC,COLM or COLX packet.		4	4	
tRTR	Interval from COLC packet with WR command to COLC packet which causes retire,and to COLM packet with bymask.		8	8	
tOFFP	The interval (offset) from COLC packet with RDA command,or from COLC packet with retire command (after WRA autmatic precharge),or from COLX packet with PREX command to the equivalent ROWR packet with PRER.		4	4	
tRDP	Interval from last COLC packet with RD command to ROWR packet with PRER.		4	-	
tRTP	Interval from last COLC packet with automatic retire command to ROWR packet with PRER.		4	-	

* Or equivalent PREC or PREX command.

Electrical Conditions (device level)

Symbol	Parameter and Conditions	Min	Max	Unit
Tj	Junction temperature under bias	TBD	TBD	°C
V_{DD},V_{DDA}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
$V_{DD,N}$,$V_{DDA,N}$	Supply voltage droop (DC) during NAP interval (t_{NLIMIT})	-	2.0	%
$V_{DD,N}$,$V_{DDA,N}$	Supply voltage ripple (AC) during NAP interval (t_{NLIMIT})	-2.0	2.0	%
V_{CMOS}	Supply voltage for CMOS pins (2.5V controllers)	2.50 - 0.13	2.50 + 0.25	V
	Supply voltage for CMOS pins (1.8V controllers)	1.80 - 0.1	1.80 + 0.2	V
V_{TERM}	Termination voltage	1.80 - 0.1	1.80 + 0.1	V
V_{REF}	Reference voltage	1.40 - 0.2	1.40 + 0.2	V
V_{DIL}	RSL data input - low voltage	V_{REF} - 0.5	V_{REF} - 0.2	V
V_{DIH}	RSL data input - high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
V_{DIS}	RSL data input swing:V_{DIS}=V_{DIH}-V_{DIL}	0.4	1.0	V
A_{DI}	RSL data asymmetry : A_{DI} = [(V_{DIH}-V_{REF}) + (V_{DIL} -V_{REF})] / V_{DIS}	-10	10	%
V_X	RSL clock input - crossing point of true and complement signals	1.3	1.8	V
$V_{CIS,CTM}$	RSL clock input swing:V_{CIS}=V_{CIH}-V_{CIL}(CTM,CTMN pins)	0.35	0.70	V
$V_{CIS,CFM}$	RSL clock input swing:V_{CIS}=V_{CIH}-V_{CIL}(CFM,CFMN pins)	0.10	0.70	V
$V_{IL,CMOS}$	CMOS input low voltage	-0.3	V_{CMOS}/2-0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	V_{CMOS}/2+0.25	V_{CMOS}+0.3	V

Timing Conditions (device level)

Symbol	Parameter		Min	Max	Unit
tCYCLE	CTM and CFM cycle times	-xx6	3.33	3.76	ns
		-xx8	2.50	3.34	ns
tCR,tCF	CTM and CFM input rise and fall times		0.2	0.5	ns
tCH,tCL	CTM and CFM input high and low times		40%	60%	tCYCLE
tTR	CTM - CFM differential	(MSE/MS = 0/0)	0.0	1.0	tCYCLE
		(MSE/MS = 1/1)	0.9	1.0	
tDCW	Domain crossing window		-0.1	0.1	tCYCLE
tDR,tDF	DQA/DQB/ROW/COL input rise/fall times		0.2	0.65	ns
tS,tH	DQA/DQB/ROW/COL-to-CFM setup/hold	tCYCLE =2.5ns @tCYCLE =3.3ns	0.200 0.275	-	ns
tDR1,tDF1	SIO0,SIO1 input rise and fall times		-	5.0	ns
tDR2,tDF2	CMD,SCK input rise and fall times		-	2.0	ns
tCYCLE1	SCK cycle time - Serial control register transactions		1000	-	ns
	SCK cycle time - Power transitions		10	-	ns
tCH1,tCL1	SCK high and low time		4.25	-	ns
tS1	CMD setup time to SCK rising or falling edge		1	-	ns
tH1	CMD hold time to SCK rising or falling edge		1	-	ns
tS2	SIO0 setup time to SCK falling edge		40	-	ns
tH2	SIO0 hold time to SCK falling edge		40	-	ns
tS3	PDEV setup time on DQA5..0 to SCK rising edge		0	-	ns
tH3	PDEV hold time on DQA5..0 to SCK rising edge		5.5	-	ns
tS4	ROW2..0,COL4..0 setup time for quiet window		-1	-	tCYCLE
tH4	ROW2..0,COL4..0 hold time for quiet window		5	-	tCYCLE
VIL,CMOS	CMOS input low voltage - over/undershoot voltage duration is less than or equal to 5ns		-0.7	VCMOS/2-0.6	V
tIH,CMOS	CMOS input high voltage - over/undershoot voltage duration is less than or equal to 5ns		VCMOS/2+0.6	VCMOS/2+0.7	V
tNPQ	Quiet on ROW/COL bits during NAP/PDN entry		4	-	tCYCLE
tREADTOCC	Offset between read data and CC packets (same device)		12	-	tCYCLE
tCCSAMTOREAD	Offset between CC packet and read data (same device)		8	-	tCYCLE

Symbol	Parameter	Min	Max	Unit
tCE	CTM/CFM stable before NAP/PDN exit	2	-	tCYCLE
tCD	CTM/CFM stable after NAP/PDN entry	100	-	tCYCLE
tFRM	ROW packet to COL packet ATTN framing delay	7	-	tCYCLE
tNLIMIT	Maximum time in NAP mode		10.0	μs
tREF	Reflesh interval		32	ms
tCCTRL	Current control interval	34tCYCLE	100ms	-
tTEMP	Temperature control interval		100	ms
tTCEN	TCE command to TCAL command	150	-	tCYCLE
tTCAL	TCAL command to quiet window	6	6	tCYCLE
tTCQUIET	Quiet window (no read data)	140	-	tCYCLE
tRAS	RAS interval (time a row may stay activated)		64	μs
tPAUSE	RDRAM delay (no RSL operations allowed)		200.0	μs

Electrical Characteristics (device level)

Symbol	Parameter and Conditions	Min	Max	Unit
Θjc	Junction - to - Case thermal resistance		TBD	°C/W
IREF	VREF current @ VREF,MAX	-10	10	μA
IOH	RSL output high current @ (0≤ VOUT ≤ VDD)	-10	10	μA
IALL	RSL IOL current @ VOL = 0.9V,VDD,MIN,TJ,MAX*	30.0	90.0	mA
ΔIOL	RSL IOL current resolution step	-	1.5	mA
rOUT	Dynamic output impedance	150	-	Ω
II,CMOS	CMOS input leakage current @ (0 ≤ VI,CMOS < VCMOS)	-10.0	10.0	μA
VOL,CMOS	CMOS output low voltage @ IOL,CMOS =1.0mA	-	0.3	V
VOH,CMOS	CMOS output high voltage @ IOH,CMOS =-0.25mA	VCMOS-0.3	-	V

*This measurement is made in manual current control mode; i.e. with all output device legs sinking current.

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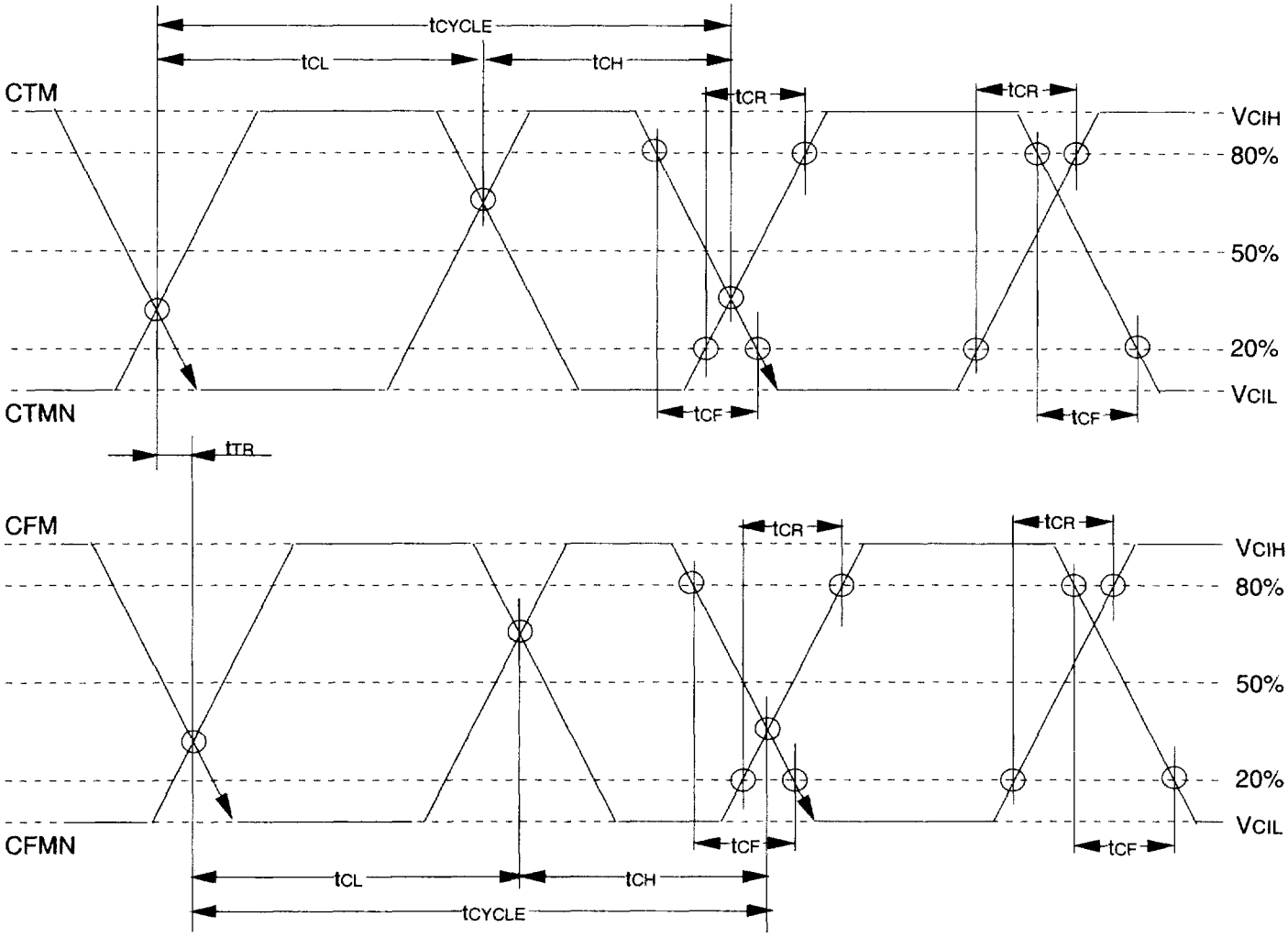
Timing Characteristics (device level)

Symbol	Parameter and Conditions	Min	Max	Unit
tQ	CTM - to - DQA/DQB output time @ tCYCLE = 2.5ns @ tCYCLE = 3.3ns	-0.275 -0.40	+0.275 +0.40	ns
tQR,tQF	DQA / DQB output rise and fall times	0.2	0.45	ns
tQ1	SCK -to- SIO0 delay @ CLOAD,MAX = 20pF (SD read packet).	-	10	ns
tQR1,tQF1	SIOOUT rise/fall @ CLOAD,MAX = 20pF	-	5	ns
tPROP1	SIO0-to-SIO1 or SIO1-to-SIO0 delay @ CLOAD,MAX = 20pF	-	10	ns
tNAPXA	NAP exit delay - phase A	-	50	ns
tNAPXB	NAP exit delay - phase B	-	40	ns
tPDNXA	PDN exit delay - phase A	-	4	μs
tPDNXB	PDN exit delay - phase B	-	9000	tCYCLE
tAS	ATTN - to - STBY power state delay	1	4	tCYCLE
tSA	STBY - to - ATTN power state delay	-	3	tCYCLE
tASN	ATTN/STBY - to - NAP power state delay	-	8	tCYCLE
tASP	ATTN/STBY - to - PDN power state delay	-	8	tCYCLE

RSL - Clocking

The following diagram shows the detailed requirements for the RSL clock signals on the Channel. The CTM and CTMN are differential clock inputs used for transmitting information on the DQA and DQB, outputs. Most timing is measured relative to the points where they cross. The tCYCLE parameter is measured from the falling CTM edge to the falling CTM edge. The tCL and tCH parameters are measured from falling to rising and rising to falling edges of CTM. The tCR and tCF rise- and fall-time parameters are measured at the 20% and 80% points.



The CFM and CFMN are differential clock outputs used for receiving information on the DQA, DQB, ROW and COL outputs. Most timing is measured relative to the points where they cross. The tCYCLE parameter is measured from the falling CFM edge to the falling CFM edge. The tCL and tCH parameters are measured from falling to rising and rising to falling edges of CFM. The tCR and tCF rise- and fall-time parameters are measured at the 20% and 80 % points.

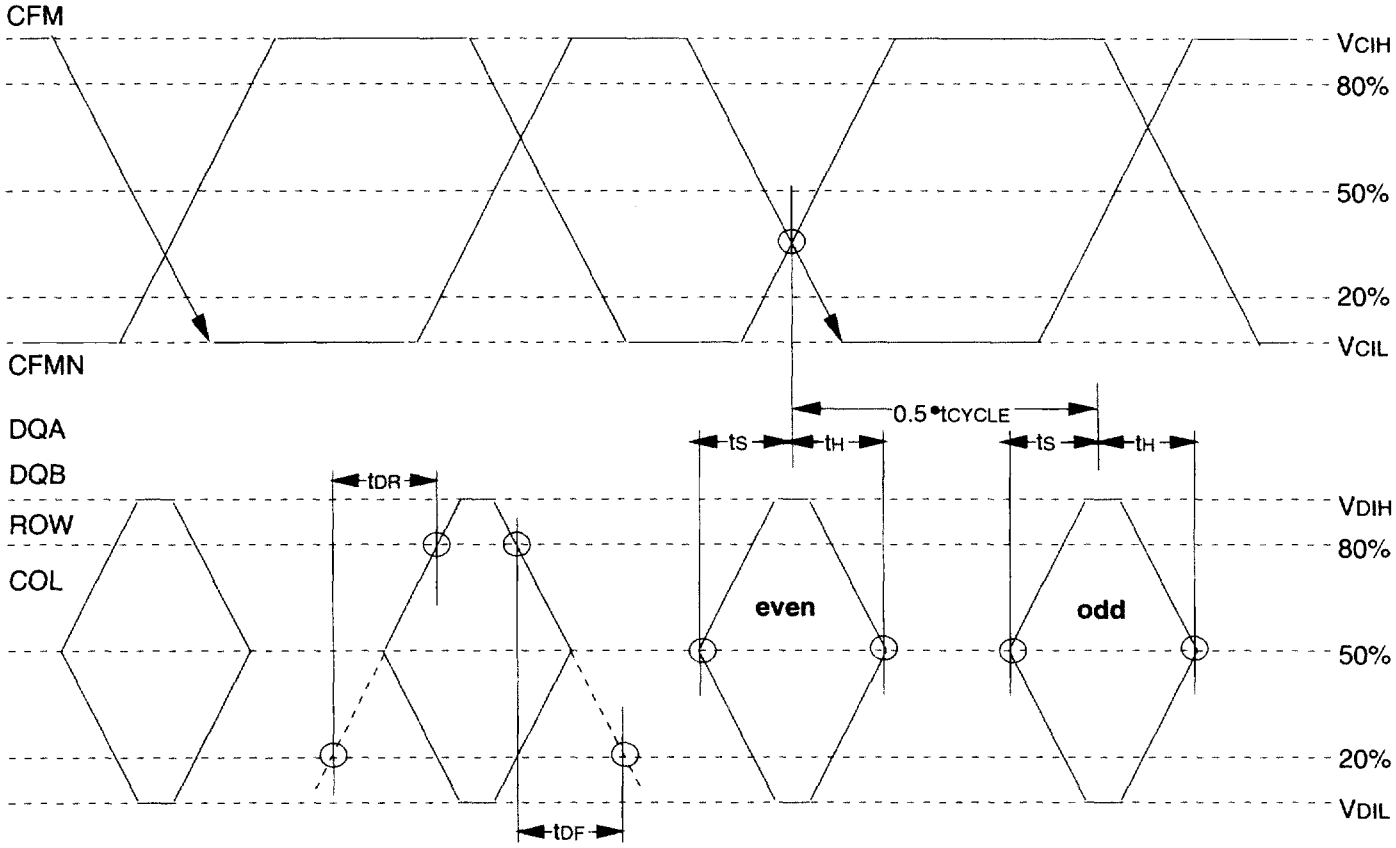
The tTR parameter specifies the phase difference that may be tolerated with respect to the CTM and CFM differential clock inputs (the CTM pair is always earlier.)

RSL - Receive Timing

The following diagram shows the detailed requirements for the RSL input signals on the Channel.

The DQA, DQB, ROW, and COL signals are inputs which recieve information transmitted by a Direct RAC on the Channel. Each signal is sampled twice per tCYCLE interval. The set / hold window of the sample points is tS/tH. The sample points are centered at the 0% and 50% points of a cycle, measured relative to the crossing points of the falling CFM clock edge. The set and hold parameters are measured at the VREF voltage point of the input transition.

The tDR and tDF rise- and fall-time parameters are measured at the 20% and 80% points of the input transition.

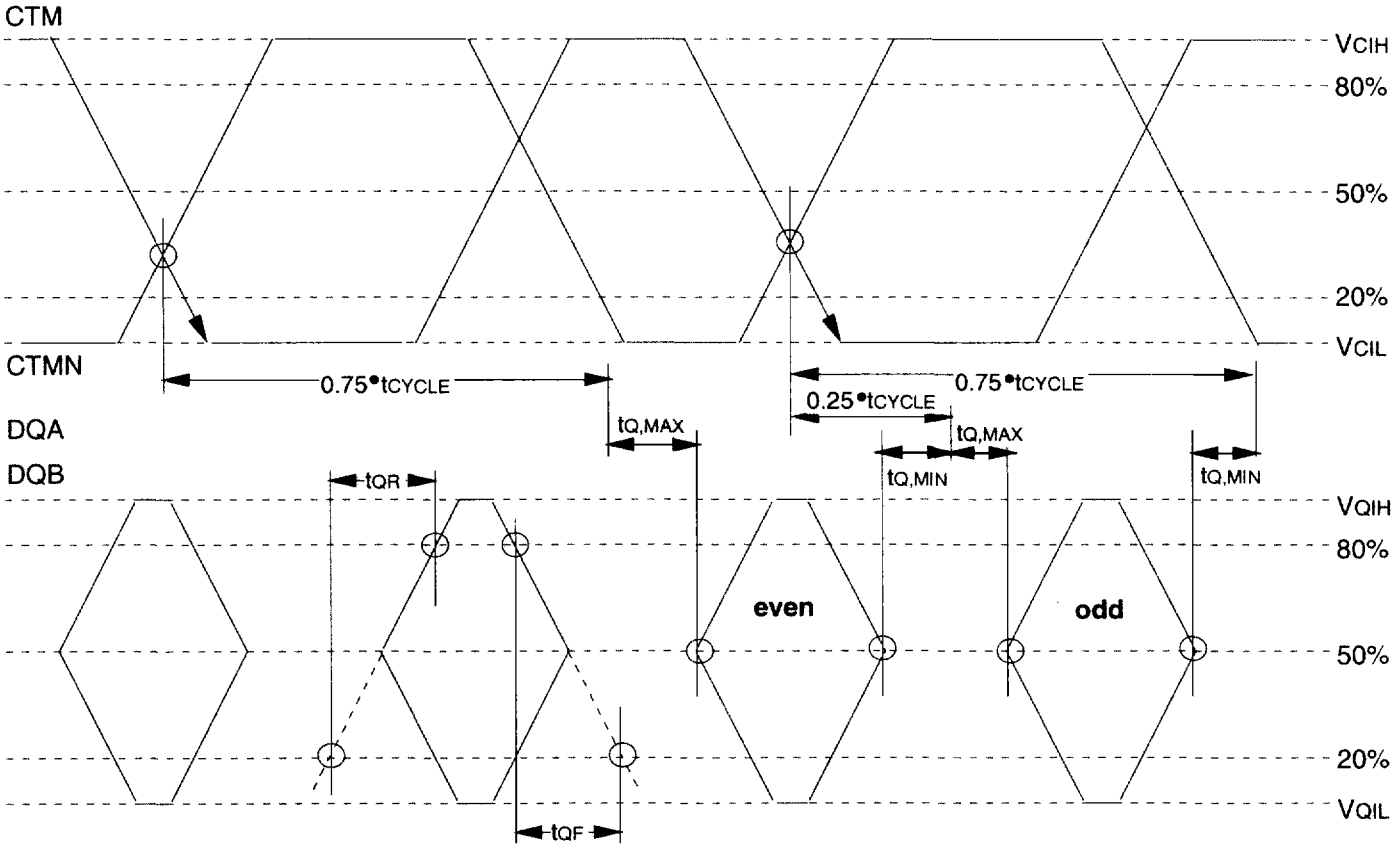


RSL - Transmit Timing

The following diagram shows the detailed requirements for the RSL output signals on the Channel.

The DQA and DQB signals are outputs to transmit information that is received by a Direct RAC on the Channel. Each signal is driven twice per tCYCLE interval. The beginning and end of the even transmit window is at the 75% point of the previous cycle and at the 25% point of the current cycle. The beginning and end of the odd transmit window is at the 25% point and at the 75% point of the current cycle. These transmit points are measured relative to the crossing points of the falling CTM clock edge. The size of the actual transmit window is less than the ideal tCYCLE/2, as indicated by the non-zero values of tQ,MIN and tQ,MAX. The tQ parameters are measured at the VREF voltage point of the output transition.

The tQR and tQF rise- and fall-time parameters are measured at the 20% and 80% points of the output transition.



CMOS - Receive Timing

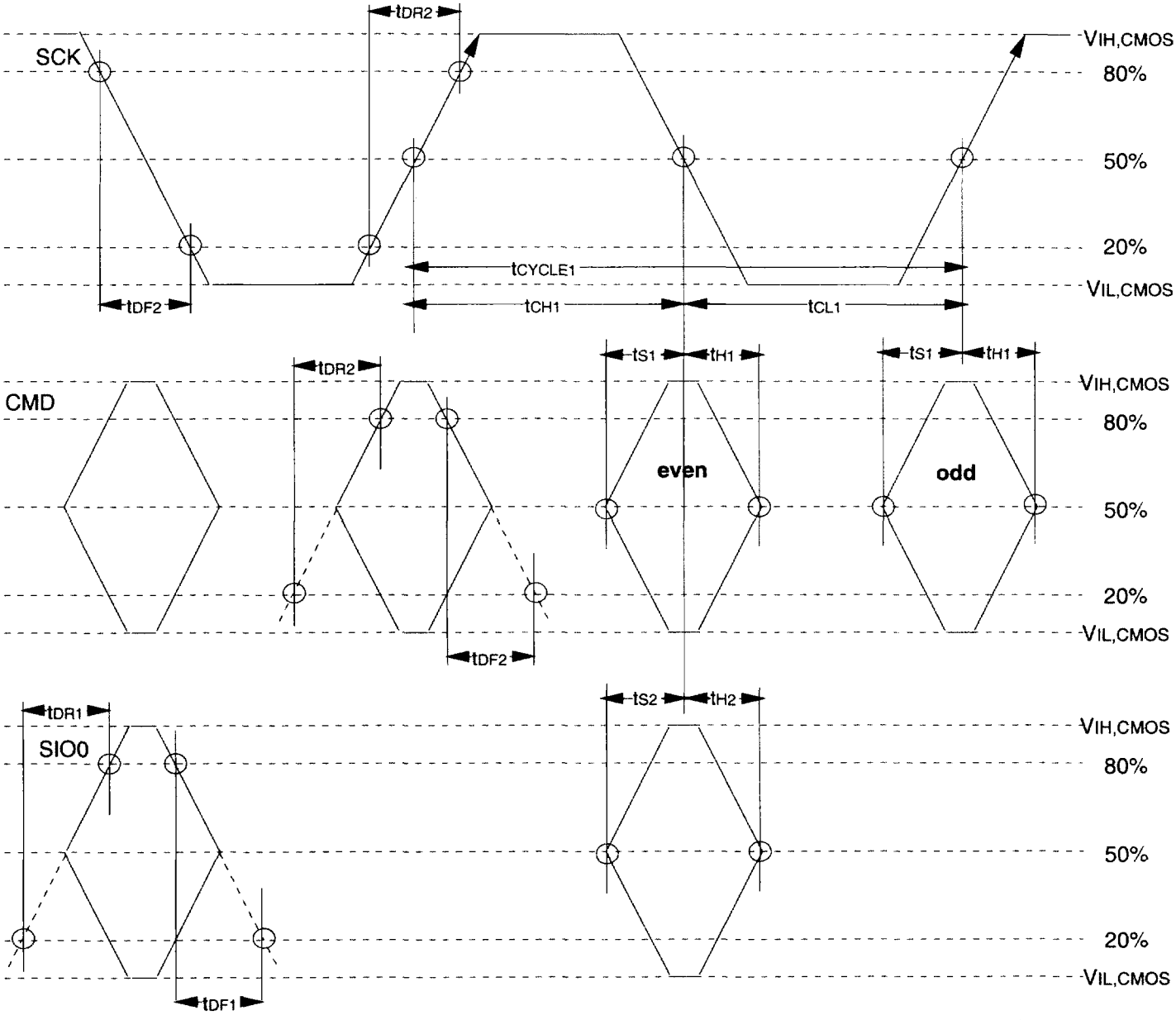
The following diagram shows the detailed requirements for the CMOS input signals.

The CMD and SIO0 signals are inputs which receive information transmitted by a controller (or by another RDRAM's SIO1 output. SCK is the CMOS clock signal driven by the controller. All signals are high true.

The cycle time, high phase time, and low phase time of the SCK clock are t_{CYCLE1}, t_{CH1} and t_{CL1}, all measured at the 50% level. The rise and fall times of SCK, CMD and SIO0 are t_{DR1} and t_{DF1}, measured at the 20% and 80% levels.

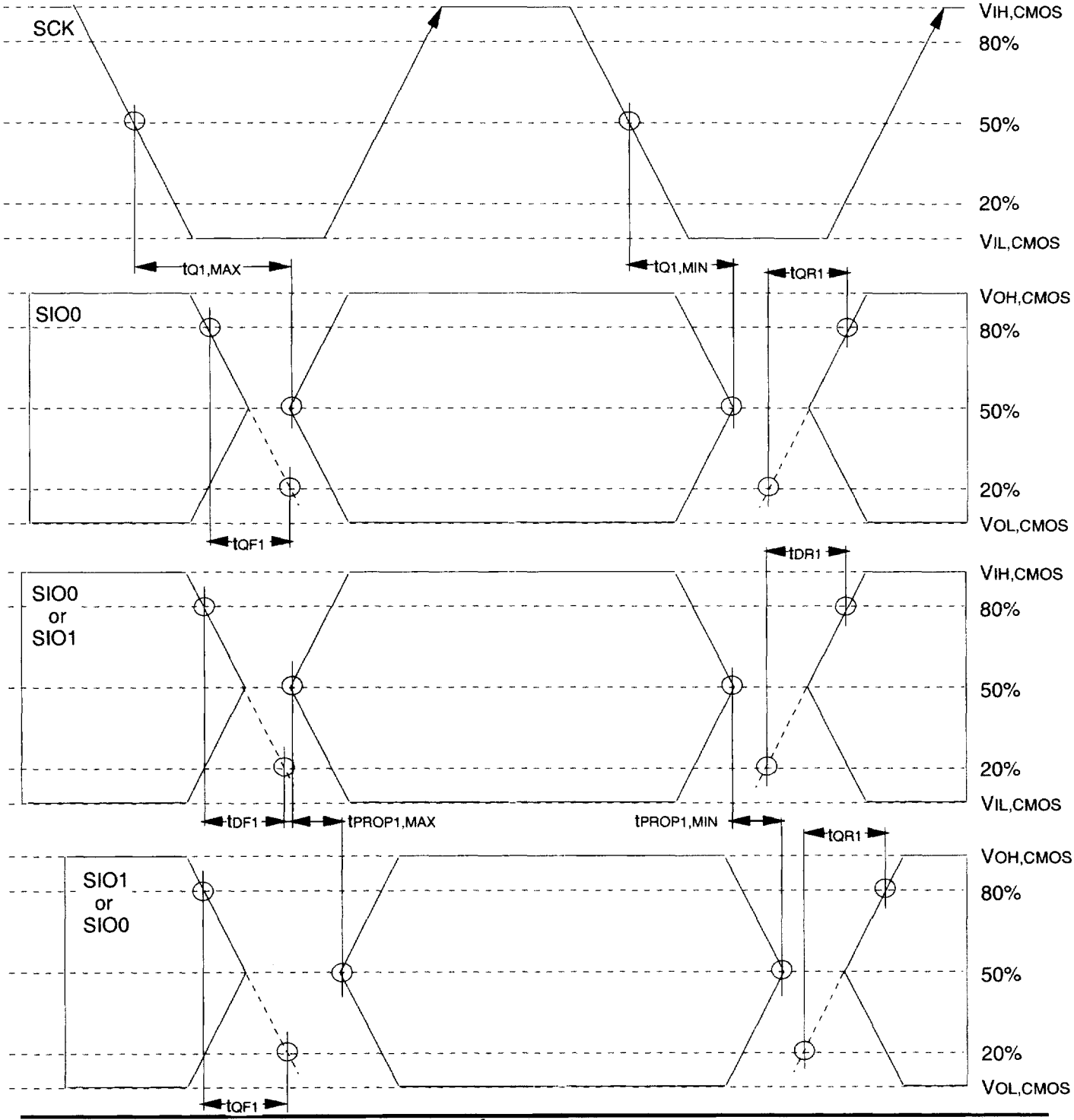
The CMD signal is sampled twice per t_{CYCLE1} interval, on the rising edge (odd data) and the falling edge (even data). The set/hold window of the sample points is t_{S1}/t_{H1}. The SCK and CMD timing points are measured at the 50% level.

The SIO0 signal is sampled once per t_{CYCLE1} interval on the falling edge. The set/hold window of the sample points is t_{S2}/t_{H2}. The SCK and SIO0 timing points are measured at the 50% level.



CMOS - Transmit Timing

The following diagram shows the detailed requirements for the CMOS output signals.
The SIO0 signal is driven once per t_{CYCLE1} interval on the falling edge. The clock-to-output window is $t_{Q1,MIN}$/$t_{Q1,MAX}$. The SCK and SIO0 timing points are measured at the 50% level. The rise and fall times of SIO0 are t_{QR1} and t_{QF1}, measured at the 20% and 80% levels.
The following diagram also shows the combinational path connecting SIO0 to SIO1 and the path connecting SIO1 to SIO0 (read data only). The t_{PROP1} parameter specified this propagation delay. The rise and fall times of SIO0 and SIO1 inputs must be t_{DR1} and t_{DF1}, measured at the 20% and 80% levels. The rise and fall times of SIO0 and SIO1 outputs are t_{QR1} and t_{QF1}, measured at the 20% and 80% levels.



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Serial Presence Detect Tablel

Byte	Description		SPD enrty data	Symbol	SPD DATA(hex)
0	SPD revision level		1		01
1	Total number of bytes in the SPD		256 Bytes		08
2	Device type		DRDRAM		01
3	Row address bits		9		09
4	Column address bits		6		06
5	Bank address bits and byte		16d		84
6	Banks per refresh		1		01
7	tREF - Refresh interval		32ms	tREF	20
8	Protocol version		1(5tTR)		02
9	Miscellaneous device configuration field		1.5tSCK	tDQS,Min	01
10	tRP -R,Min	-408	20ns	tRP-R,Min	14
		-458	20ns	tRP-R,Min	14
		-536	26ns	tRP-R,Min	1A
11	tRAS-R,Min	-408	50ns	tRAS-R,Min	32
		-458	50ns	tRAS-R,Min	32
		-536	66ns	tRAS-R,Min	42
12	tRCD-R,Min	-408	20ns	tRCD-R,Min	14
		-458	25ns	tRCD-R,Min	19
		-536	26ns	tRCD-R,Min	1A
13	tRR-R,Min	-408	20ns	tRR-R,Min	14
		-458	20ns	tRR-R,Min	14
		-536	26ns	tRR-R,Min	1A
14	tPP-R,Min	-408	20ns	tPP-R,Min	14
		-458	20ns	tPP-R,Min	14
		-536	26ns	tPP-R,Min	1A
15	Min tCYCLE for range A	-408	2.43ns	tCYCLE	13
		-458	2.43ns	tCYCLE	13
		-536	3.33ns	tCYCLE	1A
16	Max tCYCLE for range A	-408	3.33ns	tCYCLE	1A
		-458	3.33ns	tCYCLE	1A
		-536	3.71ns	tCYCLE	1D
17	tCDLY range for range A	-408	5-9	tCDLY	59
		-458	5-9	tCDLY	59
		-536	5-9	tCDLY	59
18	tCLS and tCAS range for range A	-408	tCLS = 2CYCLE	tCLS	AA
		-458	tCAS = 2CYCLE	tCAS	
		-536			
19	Min tCYCLE for range B		0		00
20	Max tCYCLE for range B		0		00
21	tCDLY range for range B		0		00
22	tCLS and tCAS range for range B		0		00
23	Min tCYCLE for range C		0		00
24	Max tCYCLE for range C		0		00
25	tCDLY range for range C		0		00
26	tCLS and tCAS range for range C		0		00
27	Min tCYCLE for range D		0		00
28	Max tCYCLE for range D		0		00
29	tCDLY range for range D		0		00
30	tCLS and tCAS range for range D		0		00

Serial Presence Detect Table I

31	$t_{PDNXA,Max}$		4μs	$t_{PDNXA,Max}$	04
32	$t_{PDNXB,Max}$		8μs	$t_{PDNXB,Max}$	08
33	$t_{NAPXA,Max}$		50ns	$t_{NAPXA,Max}$	32
34	$t_{NAPXB,Max}$		40ns	$t_{NAPXB,Max}$	28
35-38	Reserved				00
39	$t_{CCTRL,Max}$		100ms	$t_{CCTRL,Max}$	64
40	$t_{TEMP,Max}$		100ms	$t_{TEMP,Max}$	64
41	$t_{TCEN,Min}$		4t_{CYCLE}	$t_{TCEN,Min}$	04
42	$t_{RAS-R,Max}$		64μs	$t_{RAS-R,Max}$	40
43	$t_{NLIMIT,Max}$		10μs		0A
44	ACTREFPT		6t_{CYCLE}		06
45	PCHREFPT		6t_{CYCLE}		06
46	CPCHREFPT_DC		5t_{CYCLE}		05
47	RDREFPT_DC		5t_{CYCLE}		05
48	RETREFPT_DC		5t_{CYCLE}		05
49	WRREFPT_DC		13t_{CYCLE}		0D
50-62	Reserved				00
63	Checksum for locations 0-62	-408	17		17
		-458	1C		1C
		-536	49		49
64-71	Manufacture ID code		MITSUBISHI		1CFFFFFFFFFFFFFF
72	Module manufacturing location		Miyoshi		01
73-90	Module part number		MH64R18BUP-408		4D48363452313842555 02D34303820202020
			MH64R18BUP-458		4D48363452313842555 02D34353820202020
			MH64R18BUP-536		4D48363452313842555 02D35333620202020
			MH32R18BUP-408		4D48333252313842555 02D34303820202020
			MH32R18BUP-458		4D48333252313842555 02D34353820202020
			MH32R18BUP-536		4D48333252313842555 02D35333620202020
91-92	Module revision code		0.0		00
93	Module manufacturing year				YR
94	Module manufacturing week				WW
95-98	Module serial number				SN
99	Number of devices on module	MH64R	16		10
		MH32R	8		08
100	Module data width		x18		12
101-104	Device enables	MH64R	16		FFFF0000
		MH32R	8		FF000000
105	Module parameter X		TBD		00
106	Module parameter Y		TBD		00
107	Module parameter Z		TBD		00
108	Module V_{DD}		2.5V	V_{DD}	FA
109	Module V_{DD} tolerance		5%DC,2%AC		52
110	Module voltage interface level		1.8V	V_{TERM}	00
111	Module type		RIMM		01
112-126	Reserved		0		00
127	Checksum for bytes 0-126		now 00h		00
128-	Option for customer				00

References, Direct Rambus ™SPD Specification 0.7.1

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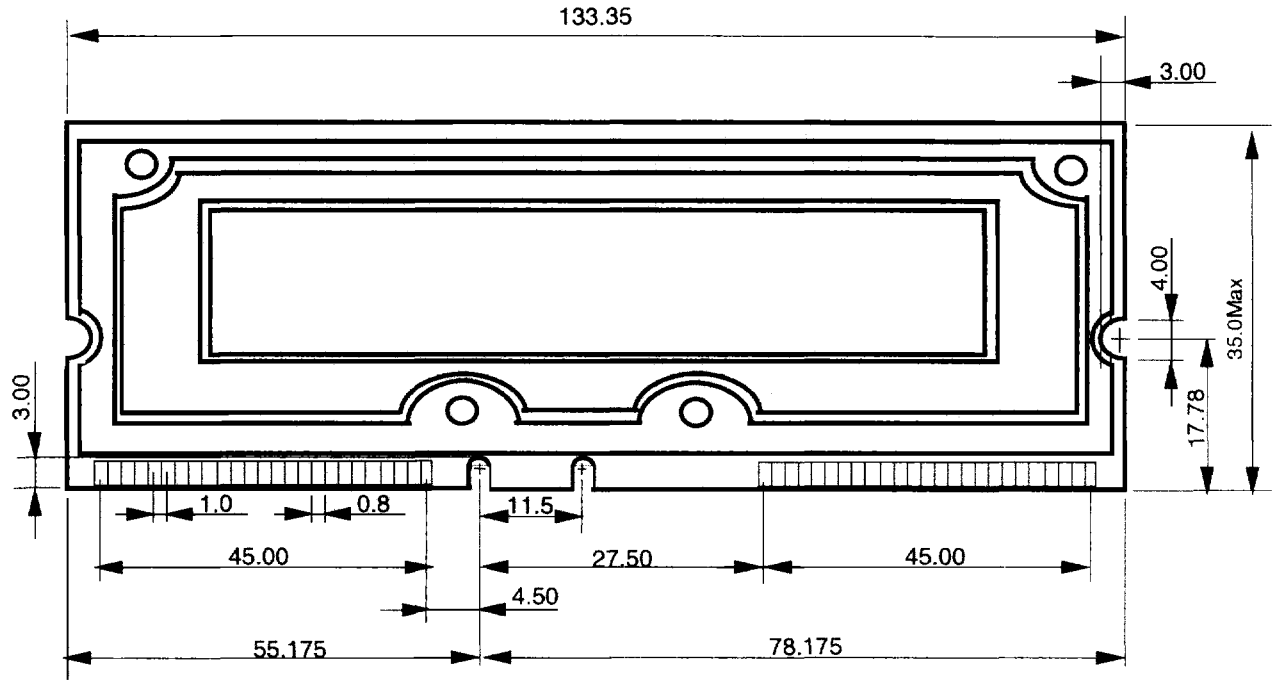
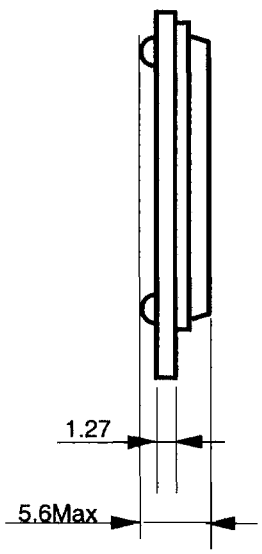
OUTLINE





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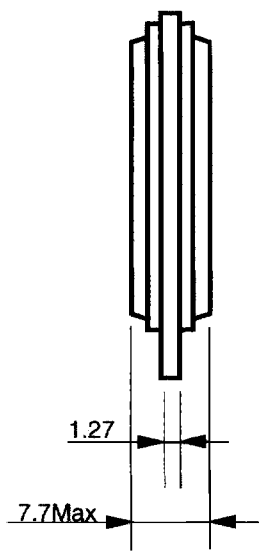

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unit : mm

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