Integrated Device Technology, Inc.

8K/16K x 9 CMOS DUAL-PORT STATIC RAM MODULES

PRELIMINARY
IDT7M1004
IDT7M1005

FEATURES:

- High density 8K/16K x 9 CMOS Dual-Port Static RAM modules
- Fast access times
  —commercial: 30, 35, 45, 55, 65ns
  —military: 40, 45, 55, 65, 80, 100ns
- Fully asynchronous read/write operation from either port
- Expand data bus width to 18 bits or more using external arbitration
- Surface mounted LCC packages allow through-hole module to fit on a 60-pin sidebrazed DIP
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

DESCRIPTION:

The IDT7M1004/1005 are 8K/16K x 9 high speed CMOS Dual-Port static RAM modules constructed on a co-fired ceramic substrate using 8 IDT7012 (2K x 9) Dual-Port RAMs or depopulated using only 4 IDT7012 Dual-Port RAMs. The IDT7M1004/1005 modules are designed to be used for stand alone 9-bit word width systems where on-chip arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

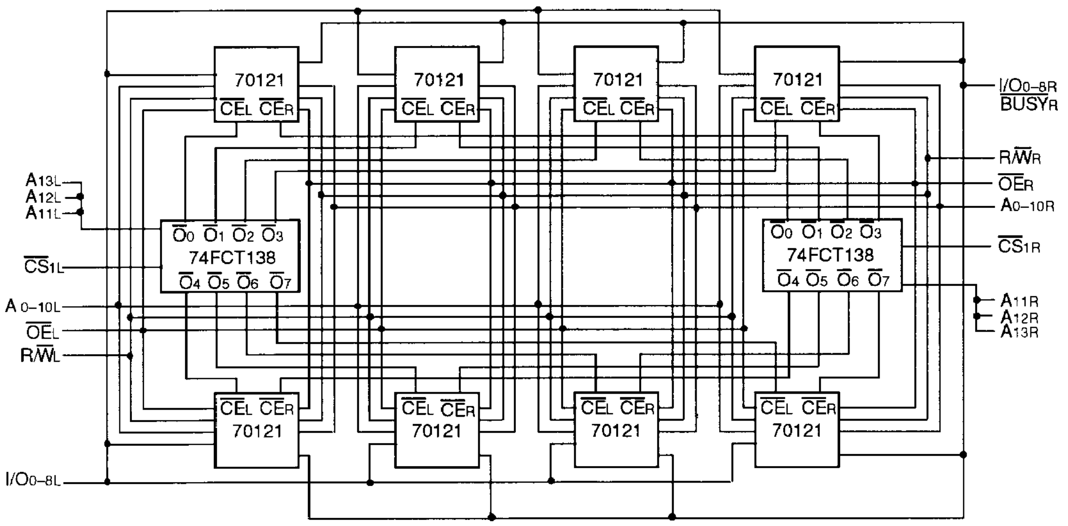
This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory.

The IDT7M1004/1005 modules are packaged in a 60-pin ceramic sidebrazed DIP (Dual In-line Package). Maximum access times as fast as 30ns are available over the commercial temperature range and 40ns over the military temperature range.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAMS

IDT7M1005 (16K x 9)



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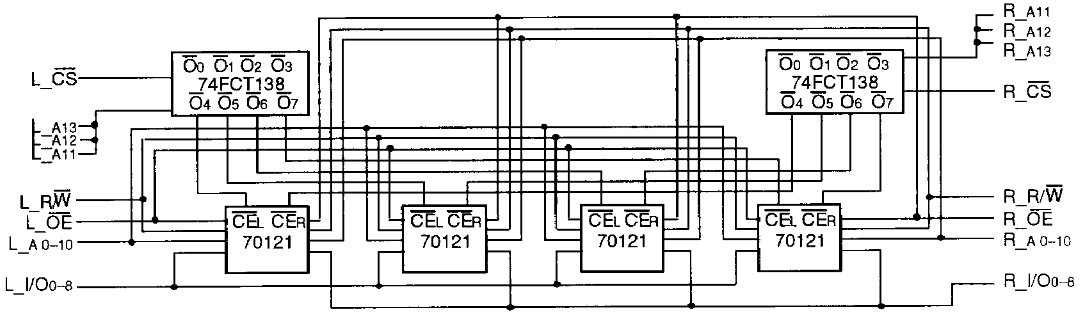
IDT7M1004 (8K x 9)



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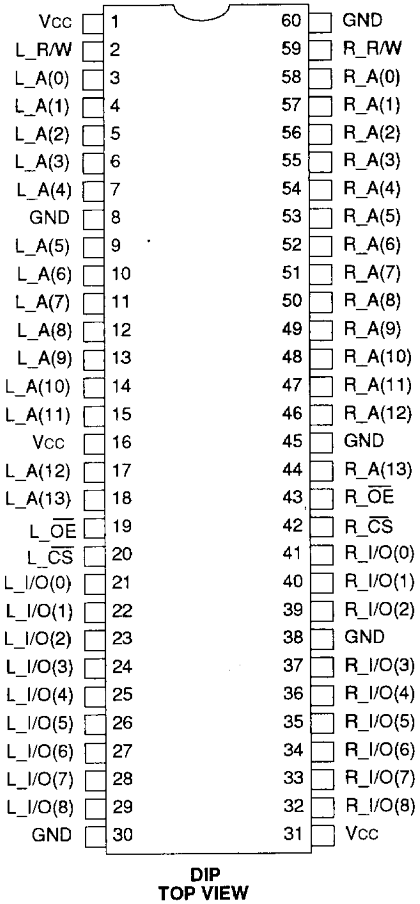
PIN CONFIGURATION



DIP
TOP VIEW

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PIN NAMES[1]

Left Port	Right Port	Names
L_$\overline{CS}$	R_$\overline{CS}$	Chip Selects
L_R/$\overline{W}$	R_R/$\overline{W}$	Read/Write Enables
L_$\overline{OE}$	R_$\overline{OE}$	Output Enables
L_A (0–13)	R_A (0–13)	Address Inputs
L_I/O (0–8)	R_I/O (0–8)	Data Input/Outputs
Vcc		Power
GND		Ground

2797 tbl 01

NOTE:

1. On the IDT7M1004 option (8K x 9) L_A_{13} and R_A_{13} need to be connected to GND for proper operation of the module.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

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NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE:

2797 tbl 03

1. $V_{IL} \geq -3.0V$ for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

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CAPACITANCE TABLE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	IDT7M1004 Max.	IDT7M1005 Max.	Unit
C_IN(1)	Input Capacitance (A0–10, $\overline{OE}$, R/$\overline{W}$)	V_IN = 0V	100	55	pF
C_IN(2)	Input Capacitance (Data)	V_IN = 0V	100	55	pF
C_IN(3)	Input Capacitance (A11–13, $\overline{CS}$)	V_IN = 0V	15	15	pF
COUT	Output Capacitance (Data)	V_OUT = 0V	100	55	pF

NOTE:

2797 tbl 05

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M1004		IDT7M1005		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	40	—	80	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	40	—	80	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	2.4	—	V

2797 tbl 06

Symbol	Parameter	Test Conditions	Commercial			Military			Unit
			Min.	Max.(1)	Max.(2)	Min.	Max.(1)	Max.(2)	
I_{CC2}	Dynamic Operating Current (Both Ports Active)	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, Outputs Open, f = f_{MAX}	—	500	870	—	560	860	mA
I_{CC1}	Standby Supply Current (One Port Inactive)	V_{CC} = Max., $\overline{CS}$_L or $\overline{CS}$_R ≥ V_{IH} Outputs Open, f = f_{MAX}	—	370	650	—	430	750	mA
I_{SB1}	Standby Supply Current (Both Ports Inactive)	V_{CC} = Max., $\overline{CS}$_L and $\overline{CS}$ ≥ V_{IH} Outputs Open, f = f_{MAX}	—	280	560	—	280	560	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	$\overline{CS}$_L and $\overline{CS}$_R ≥ V_{CC} –0.2V $V_{IN} > V_{CC}$ 0.2V or < 0.2V, f=0	—	60	120	—	120	240	mA

NOTES:

2797 tbl 07

1. IDT7M1004 (8K x 9) version only.
2. IDT7M1005 (16K x 9) version only.

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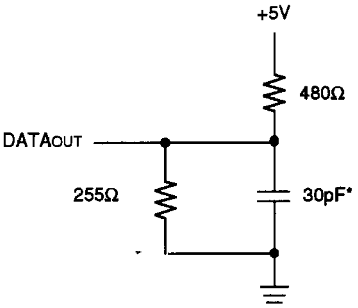
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2797 tbl 08



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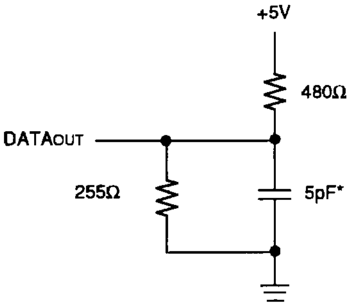

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*Including scope and jig.

Figure 1. Output Load

Figure 2. Output Load (For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)

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AC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = –55°C to +125°C or 0°C to +70°C)

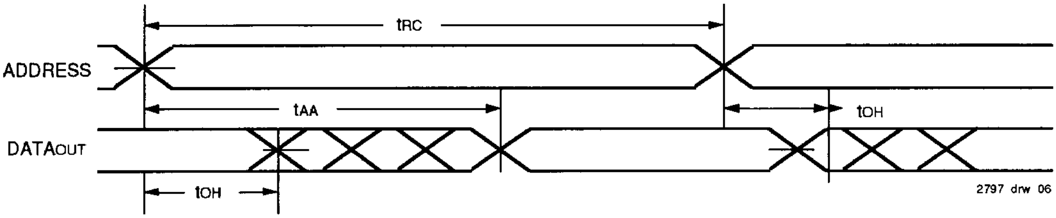
Symbol	Parameter	-30(9)		-35(9)		-40		-45		-55		-65		-80(10)		-100(10)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle																		
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{ACS}(2)	Chip Select Access Time	—	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	ns
t_{OE}	Output Enable Access Time	—	15	—	20	—	20	—	25	—	30	—	35	—	40	—	45	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	3	—	3	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	3	—	3	—	3	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Up Time	—	50	—	50	—	50	—	50	—	50	—	50	—	50	—	50	ns
Write Cycle																		
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	55	—	65	—	80	—	100	—	ns
t_{CW}(2)	Chip Select to End of Write	25	—	30	—	35	—	40	—	45	—	50	—	55	—	60	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	35	—	40	—	45	—	50	—	55	—	60	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	35	—	40	—	50	—	55	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	20	—	25	—	25	—	25	—	30	—	40	—	45	—	50	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	15	—	15	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{OW}(1)	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns

2797 tbl 09

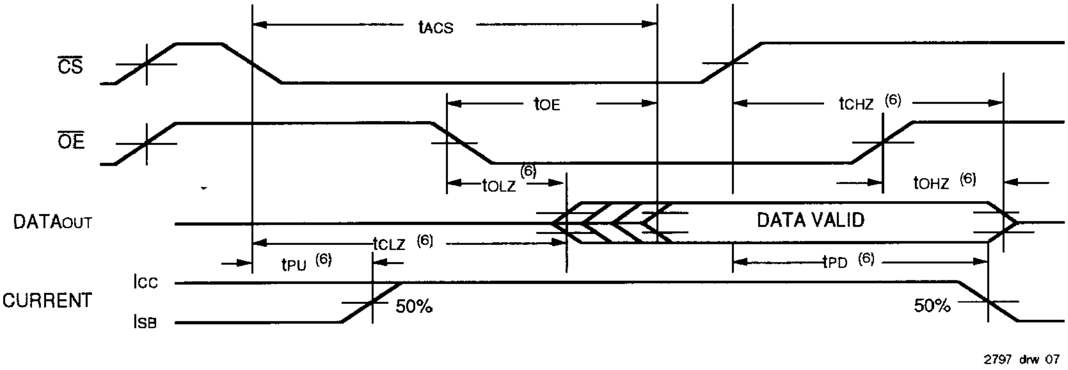
NOTES:

1. This parameter is guaranteed by design but not tested.
2. To access RAM array, $\overline{CS} \le V_{IL}$.
3. Master mode is not available on this module.
4. The module is always in the Slave Mode.
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. This speed is currently available in commercial versions only.
10. This speed is currently available in military versions only.

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) (1, 2, 4)



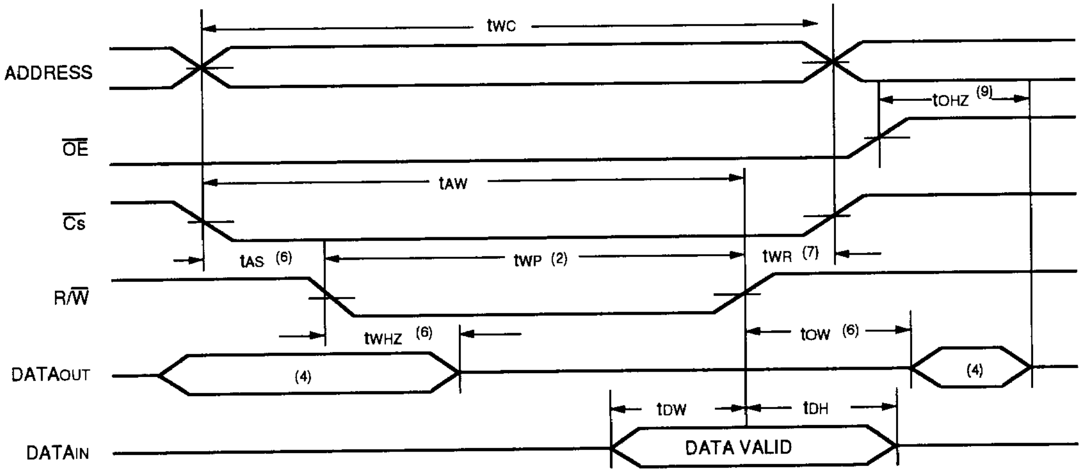
TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE) (1, 3, 5)



NOTES:

1. R/$\overline{W}$ is high for Read Cycles
2. Device is continuously enabled, $\overline{CS}$ = L. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low
4. $\overline{OE}$ = L
5. To access RAM, $\overline{CS}$ = L. To access semaphore, $\overline{CS}$ = H.
6. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{\text{W}}$ CONTROLLED TIMING) (1, 3, 5, 8)



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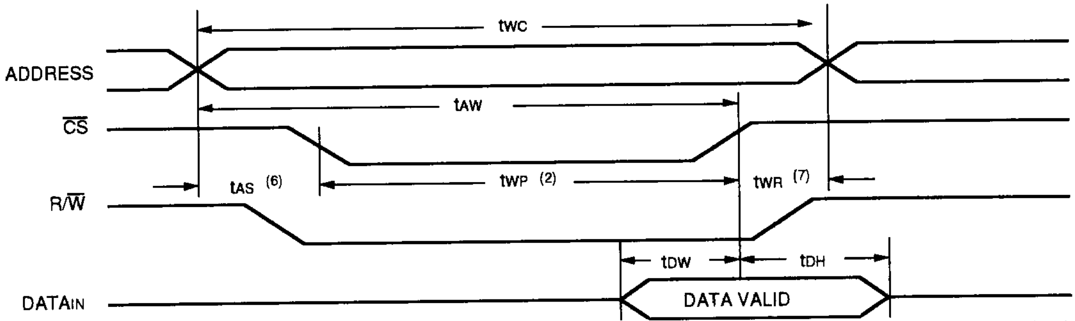
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING) (1, 3, 5, 8)



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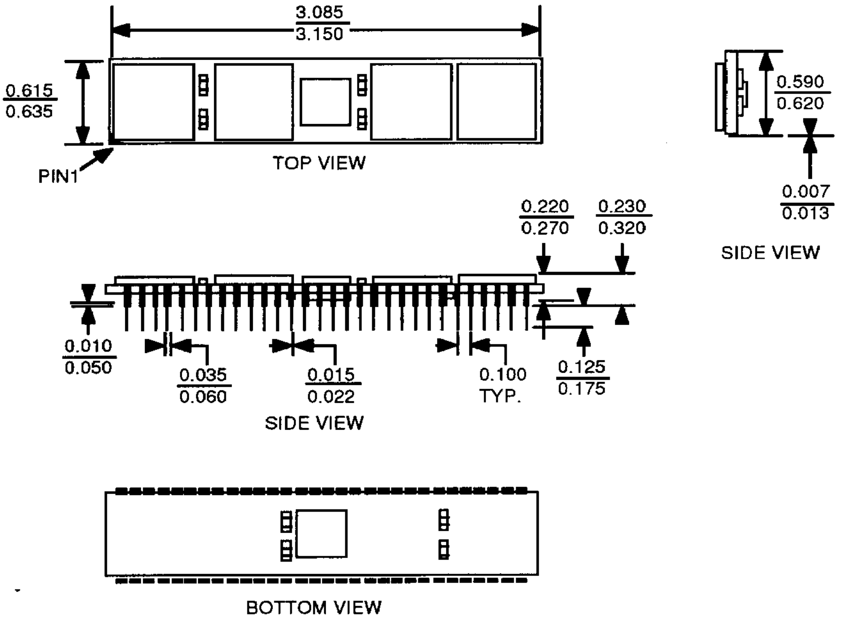
NOTES:

1. R/$\overline{\text{W}}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}$ and a low R/$\overline{\text{W}}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or R/$\overline{\text{W}}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{\text{CS}}$ low transition occurs simultaneously with or after the R/$\overline{\text{W}}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{\text{OE}}$ is low during a R/$\overline{\text{W}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is high during an R/$\overline{\text{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. This parameter is guaranteed by design but not tested.

PACKAGE DIMENSIONS

7M1004



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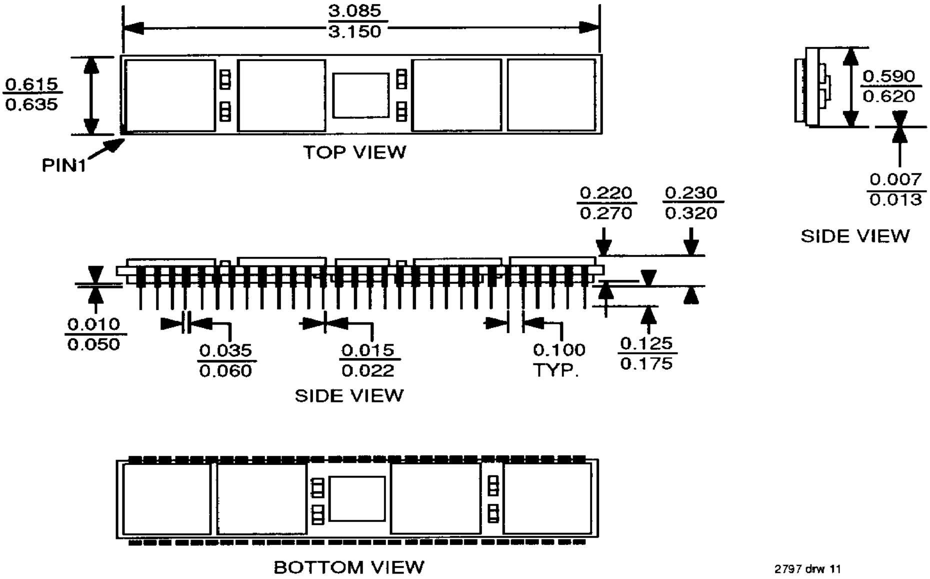

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