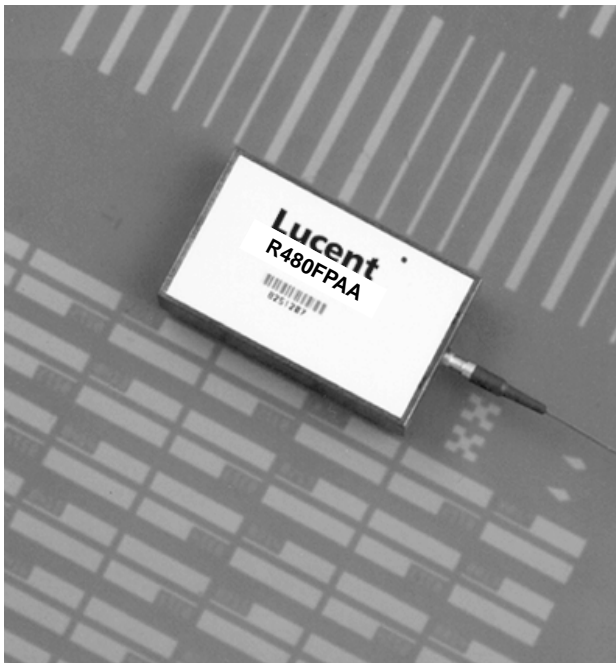




R480-Type Lightwave Receiver with CML Data Output for 2.488 Gbits/s Applications



Manufactured in a low-profile, 24-pin package, the R480-Type receiver features either an avalanche or PIN photodetector, a transimpedance amplifier, and a limiting amplifier IC.

Features

- Multisourced footprint
- Internal APD bias supply
- Differential CML data output
- APD and PIN versions
- Typical sensitivity:
 - APD, -32 dBm
 - PIN, -23 dBm
- Operation at 1.3 μm or 1.55 μm
- TTL link status flag
- Wide operating case temperature range:
 - APD, 0 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$
 - PIN, -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$

- Space-saving, self-contained, 24-pin DIP
- Lucent Technologies' Reliability and Qualification Program for built-in quality
- SONET/SDH compatible for OC-48/STM-16 data rate

Applications

- Telecommunications:
 - Inter- and intraoffice SONET/SDH
 - Subscriber loop
 - Metropolitan area networks
- High-speed data communications

Description

The R480-Type 2.5 Gbits/s lightwave receiver is designed for use in SONET OC-48 and synchronous digital hierarchy (SDH) STM-16 telecommunications applications and high-speed data communications applications. The receiver converts received optical signals in the range of 1.2 μm to 1.6 μm wavelength into differential CML data outputs. The receiver consists of either an InGaAs APD or PIN photodetector (depending on model selected), a transimpedance amplifier, and a limiting amplifier that provides differential CML data output. A TTL compatible link status flag signal indicates when there is a loss of optical signal.

The receiver is manufactured in a low-profile, pig-tailed, 24-pin plastic DIP package. It requires a single, 5.0 V power supply. The APD version has the added benefit of containing the high-voltage supply internal to the receiver. This internal supply also provides the necessary temperature compensation for the APD. An analog photodetector monitor provides a voltage proportional to the optical input level voltage (OILV).

Flag Output

When the incoming optical signal falls below the link-status switching threshold, the FLAG output is asserted and the FLAG output logic level changes from a TTL low to a TTL high.

Pin Information

Table 1. Pin Information

Pin	Name	Pin	Name
1	NIC*	24	NUC†
2	NUC†	23	OILV
3	LOS Flag‡	22	Vcc
4	Ground	21	NUC†
5	NIC*	20	Ground
6	NIC*	19	Ground
7	Ground	18	NIC*
8	Vcc	17	Ground
9	Ground	16	Ground
10	DATA	15	Ground
11	$\overline{\text{DATA}}$	14	Ground
12	Ground	13	NIC*

* Pins labeled NIC have no internal connection.

† Pins designated as no user connect (NUC) are connected internally. The user should not make any connections to these pins.

‡ The loss of signal (LOS) FLAG output is a logic level that indicates the presence or absence of a minimum acceptable level of optical input. A TTL logic HIGH indicates the absence of a valid optical input signal.

§ Analog optical input level voltage (OILV) is proportional to the optical input power.

Handling Precautions

The R480-Type receiver is manufactured with a 39 in. \pm 4 in. (100 cm \pm 10 cm) single-mode fiber pigtail with a 900 μ m OD PVC outer jacket. Both SC and FC-PC connectors are offered on standard versions. Other optical connector options are available on special order. Please contact a Lucent Technologies Microelectronics Group Account Manager for availability and ordering information.

The minimum fiber bending radius is 1.5 inches (38 mm).

Receiver Processing

The R480-Type receiver devices can withstand normal wave-soldering processes. The complete receiver module is not hermetically sealed; therefore, it should not be immersed in, or sprayed with, any solutions. The optical connector process cap deformation temperature is 85 °C. The receiver pins can be wave soldered at 250 °C for 10 seconds.

Electrostatic Discharge

CAUTION: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Lucent Technologies employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 k Ω , capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.

Installation Considerations

Although the receiver has been designed with ruggedness in mind, care should be used during handling. The optical connector should be kept free from dust. The optical connector process cap should be kept in place as a dust cover when the device is not connected to a cable. If contamination is present on the optical connector, the use of canned air with an extension tube should remove any loose debris. Other cleaning procedures are outlined in the *Cleaning Fiber Optic Assemblies* Technical Note (TN95-010LWP).

The cable should be handled conservatively, with no excessive axial pulling or lateral tugging.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature Range:				
APD	T _C	0	70	°C
PIN	T _C	-40	85	°C
Storage Temperature	T _{stg}	-40	85	°C
Optical Input Power—Biased:				
APD	P _{IN}	—	3	dBm
PIN	P _{IN}	—	8	dBm
Supply Voltages	V _{CC}	0	6.5	V
Lead Soldering Temperature/Time	—	—	250/10	°C/s

Characteristics

Table 2. Optical Characteristics

At 1.3 μm wavelength and 1 x 10⁻¹⁰ BER with 2²³ - 1 NRZ pseudorandom data.

Parameter	Symbol	Min*	Typ [†]	Max*	Unit
Measured Average Sensitivity:					
APD	P _{MIN}	—	-32	-30	dBm
PIN	P _{MIN}	—	-23	-21	dBm
Maximum Input Power:					
APD	P _{MAX}	-8	—	—	dBm
PIN	P _{MAX}	-3	—	—	dBm
Link Status Switching Threshold Decreasing Light Input:					
APD	LSTD	-45	-40	-35	dBm
PIN	LSTD	-38	-31	-27	dBm
Flag Response Time	t _{FLAG}	3	—	1000	μs
Signal-Detect Hysteresis	—	0.5	—	—	dB
Optical Input Level Voltage: [‡]					
PIN at 0 dBm	OILV	—	2.0	—	V
APD at -10 dBm	OILV	—	2.0	—	V
Reflectance	—	—	—	-27	dB

* Over operating temperature range and at end of life.

† Typical values at room temperature and beginning of life.

‡ OILV measured with respect to ground.

Characteristics (continued)

Table 3. Electrical Characteristics

Parameter	Symbol	Min	Typ*	Max	Unit
Bit Rate	—	2488.07	2488.32	2488.57	Mbits/s
dc Power Supply Voltages	V _{CC}	4.75	5.0	5.25	V
Power Consumption	—	—	1.0	1.5	W
Output Data Voltage:†					
Single Output	SV	0.3	—	0.5	Vp-p
Differential Output	DV	0.6	—	1.0	Vp-p
Output Flag Voltage:‡					
High	V _{FOH}	4.0	5.0	V _{CC}	V
Low	V _{FOL}	0	0.2	0.4	V

* Typical values measured at room temperature and beginning of life.

† Measured with a 50 Ω to ground. Outputs must be ac-coupled (see Figure 2).

‡ TTL output.

Qualification and Reliability

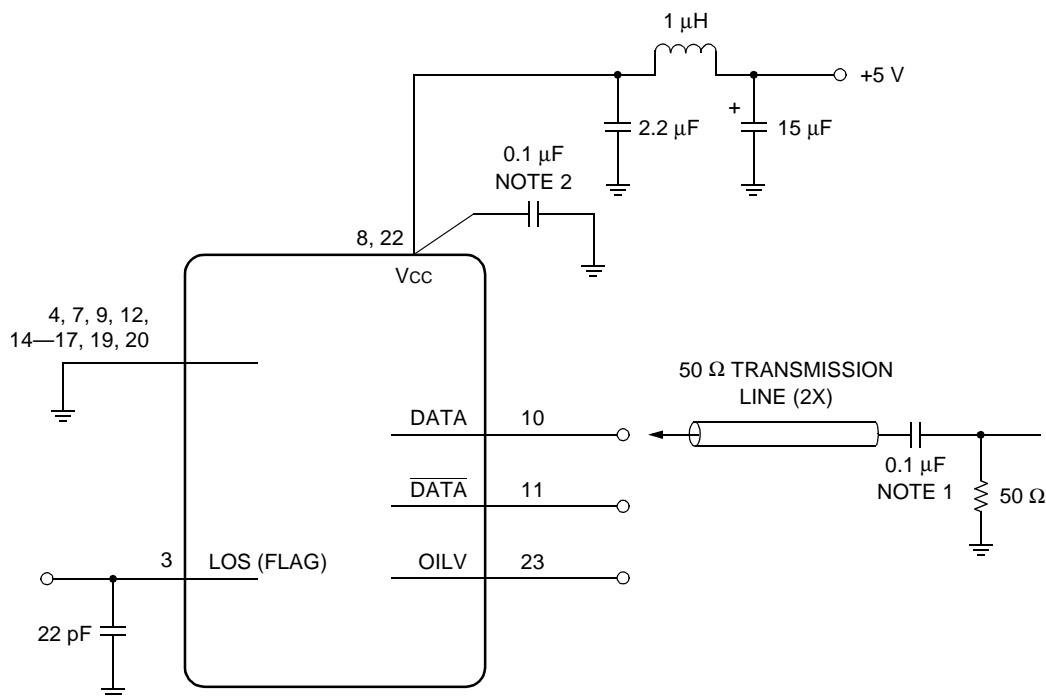
To help ensure high product reliability and customer satisfaction, Lucent is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronics modules are qualified to Lucent internal standards using MIL-STD-883 test methods and procedures, and using sampling techniques consistent with *Telcordia Technologies** requirements. This qualification program fully meets the intent of *Telcordia Technologies* reliability practices TR-NWT-000468 and TA-TSY-000983. In addition, the Optoelectronics design, development, and manufacturing facility of Lucent Technologies Microelectronics Group has been certified to be in full compliance with the latest ISO†-9001 Quality System Standards.

* *Telcordia Technologies* is a trademark of Bell Communications Research, Inc.

† ISO is a registered trademark of the International Organization for Standardization.

PWB Layout Guidelines

- The data outputs are designed to drive 50 Ω loads.
- Data output traces must be controlled-impedance lines and the termination impedance must match the line impedance. Avoid 90° bends in the traces. Paired lines (i.e., DATA and $\overline{\text{DATA}}$) must be equal in length.
- Data output lines should be as short and straight as possible and should be shielded from noise sources to prevent noise from feeding back into the receiver.
- Use high-quality multilayer printed-wiring boards. A ground plane should occupy the area directly beneath the receiver.



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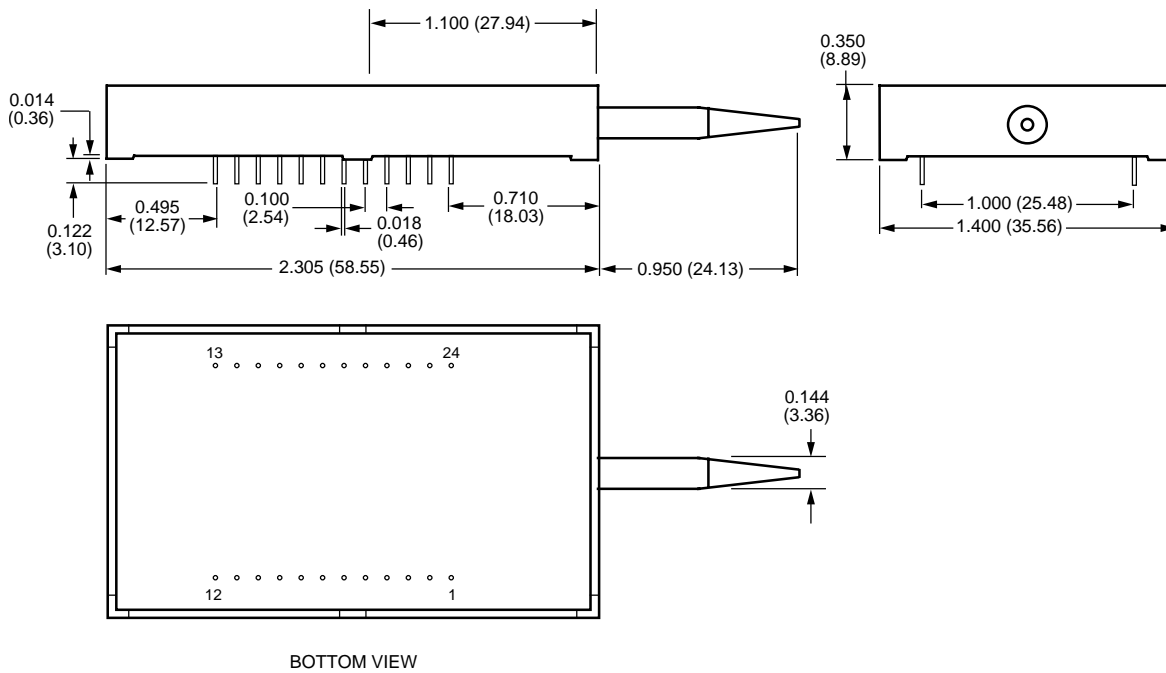
Note 1: Data outputs must be ac-coupled on customer board. Use a 0.1 μF chip capacitor with a low ESR. For optimum receiver performance, both data outputs must be terminated in equivalent loads, even if one of the outputs is not being used.

Note 2: The 0.1 μF Vcc power supply bypass capacitors should be high-quality, low ESR chip capacitors that are located as close as possible to the appropriate power supply leads and should provide a low-inductance path to the ground plane.

Figure 1. Biasing and Interfacing to the R480-Type 2.5 Gbits/s Receiver

Outline Diagrams

Dimensions are in inches and (millimeters).



1-999(C)

Ordering Information

Table 4. Ordering Information for the R480-Type Receiver

Product Code	Detector	Connector	Comcode
R480CPAA	PIN	SC	TBD
R480FPAA	PIN	FC/PC	TBD
R480CMAA	APD	SC	TBD
R480FMAA	APD	FC/PC	TBD
R480WPAA	PIN	LC	TBD
R480WMAA	APD	LC	TBD

Table 5. Related Product Information

Product Code	Description	Document Number
T48 Transmitter	2.5 Gbits/s Uncooled Laser Transmitter	DS00-088OPTO
R485-Type Receiver	2.5 Gbits/s Receiver with Clock Recovery	DS01-005OPTO

For additional information, contact your Microelectronics Group Account Manager or the following:

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