

Sil 0680A PCI to IDE/ATA Chip



Data Sheet

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Revision History:

Version	Comment	Date
Rev. 0.1	First draft (from Engineering Design Specification)	08/07/00
Rev. 0.2	Additional register definitions added	10/09/00
Rev. 0.3	Changed package type to TQFP	10/10/00
Rev. 0.4	Changed TQFP drawing: minor changes to pinout and PLL external component values	10/13/00
Rev. 0.5	Completely re-written from technical standpoint	01/23/01
Rev. 0.5A	PRELIMINARY markings removed: submitted for review/comment	01/26/01
Rev 0.90	Major Content Changes	07/05/01
Rev. 0.91	More content changes	08/08/01
Rev. 0.92	Content corrections	08/09/01
Rev. 0.93	Made Minor corrections	08/10/01
Rev. 0.99	Corrections made in preparation of releasing Rev 1.0 version including adding references to ATA/133	
Rev. 1.0	Final corrections made, errata added	09/24/01
Rev. 1.05	Errata for chip Revision 00, marked "680 CES", removed	11/15/01
Rev. 1.1	Changed Register defaults and Resistor Values consistent with chip Revision 01. Clarified OS support.	11/29/01
Rev. 1.2	Changed Document Number	01/09/02
Rev. 1.3	Made minor corrections and change the document name from 680 to 680A	5/16/02

1. Overview

The Silicon Image Sil 0680A is a single-chip solution for a PCI to ATA controller. It accepts host commands through the PCI bus, processes them and transfers data between the host and ATA devices. It can be used to control two independent ATA channels: primary and secondary. Each channel has its own ATA bus and will support up to two ATA/ATAPI devices for a maximum of four devices. The Sil 0680A supports up to a 133 MB/sec transfer rate exceeding that which is specified in ATA/ATAPI-6.

This controller provides OEMs with an enabling solution for interfacing to storage media such as hard disk drives. For personal computer manufacturers, using the Sil 0680A will differentiate them from the competition by allowing for the addition of more drives and incorporating the newest drive standards, all at a lower cost. For embedded applications, the Sil 0680A provides a high performance and cost effective interface for storage and ATAPI device support.

1.1 Key Benefits

The Silicon Image Sil 0680A stand-alone Ultra ATA/133 PCI to ATA host controller is the perfect single-chip solution for designs based on chipsets without an integrated ATA host controller, or designs which need to expand the number of ATA channels to accommodate the growing number of storage peripherals with ATA interface.

The Sil 0680A comes complete with drivers for Windows 98, Windows Millennium, Windows NT 4.0, Windows 2000, Windows XP and Linux. It is also fully operational and compatible with default IDE drivers from Microsoft.

Comprehensive RAID (0, 1, 0+1) software support is also provided for Windows 98, NT 4.0, Windows Me, Windows 2000 and Windows XP.

1.2 Features

1.2.1 Overall Features

- Standalone PCI to ATA host controller chip
- Compliant with PCI Specification, revision 2.2.
- Compliant with PCI IDE Controller Specification, revision 1.0.
- Compliant with Programming Interface for Bus Master IDE Controller, revision 1.0.
- Compliant with ATA/ATAPI-6 specifications.
- Compliant with UDMA6 ATA/133 Specification
- Driver support for Win98, WinME, NT4, Win2K and XP.(IDE and RAID including Linux IDE support)
- Supports up to 4Mbit external FLASH or EPROM for BIOS expansion.
- Supports an external EEPROM, FLASH or serial EPROM for programmable subsystem vendor ID and subsystem product ID.
- Supports all necessary test requirements for WHQL.
- Supports the Microsoft driver protocols for PIO and bus master DMA operations.
- Fabricated in a 0.35 μ CMOS process with a 3.3 volt core and 5 volt tolerant I/Os.
- Available in a 144-pin LQFP package.

1.2.2 PCI Features

- Supports PCI 33 MHz with 32-bit data.
- Supports PCI PERR and SERR reporting.
- Supports PCI bus master operations: Memory Read, Memory Read Multiple, and Memory Write.
- Supports PCI bus target operations: Configuration Read, Configuration Write, I/O Read, I/O Write, Memory Read, Memory Write, Memory Read Line (Memory Read), Memory Read Multiple (Memory Read), Memory Write and Invalidate (Memory Write).
- Supports byte alignment for odd-byte PCI address access.
- Supports jumper configurable PCI class code.
- Supports programmable and EEPROM, FLASH and EPROM loadable PCI class code.
- Supports IDE native mode (non-legacy) functions only. memory space

1.2.3 ATA Features

- Supports two independent ATA channels.
- Supports ATA 133.
- Supports full speed burst transfers on the ATA bus.
- Supports software-controlled ATA bus tri-state.
- Supports device specific timing registers.
- Supports device read-ahead and write-ahead capability under Virtual DMA.

1.2.4 Other Features

- Features one 256-byte FIFO (32-bit x 64 deep) per IDE channel for host reads and writes.
- Features ATA to PCI interrupt masking.
- Features command buffering from the PCI to ATA.
- Features Virtual DMA: Bus master transfer on the PCI bus and PIO transfer on the ATA bus.
- Features Watch Dog Timer for fault resiliency.

1.3 Sil 0680A Technical Description

The Sil 0680AA is available in a 144-pin LQFP (Thin Quad Flat Package) including more ground pins in order to accommodate the new higher data transfer rate specified in the ATA/ATAPI-6 specification. The chip has an internal phase lock loop that will provide the 100/133MHz (selectable) internal clock, allowing a data transfer rate of 100/133MB/sec (selectable) on ATA interface. A built-in 80-pin cable detector provides users the ability to determine whether a cable can support the latest Ultra ATA/100/133 (selectable) transfer rate. The Sil 0680A is capable of supporting Native mode, external BIOS, Enhanced IDE mode (ultra DMA and multiword DMA mode) and PIO mode.

1.4 References

For more details about the ATA technology, the reader is referred to the following industry specifications:

- ATA/ATAPI-6 (at time of publication, ATA/ATAPI-6 has not been formally approved)
- PCI Local Bus Specification Revision 2.2
- Advanced Power Management Specification Revision 1.0
- PCI IDE Controller Specification Revision 1.0
- Programming Interface for Bus Master IDE Controller, Revision 1.0

1.5 Functional Description

Sil 0680A is more than a PCI-to-ATA bridge chip that transfers data between the PCI bus and storage media (e.g hard disk drive, etc) over the ATA bus. As a host controller, it also performs functions associated with the host, such as storing configuration information, and processing data for errors. The Sil 0680A680A can be described in the following functional blocks:

- PCI Interface. Provides the interface to any system that has a PCI bus. Instructions and system clocks are based on this interface.
- ATA Interface. Two separate channels (Primary and Secondary) to access storage media such as hard disk drives, CD-ROM's etc.
- Controller Interface. Additional hardware interface for controlling and configuring the Host Controller.

1.6 Functional Block Diagram

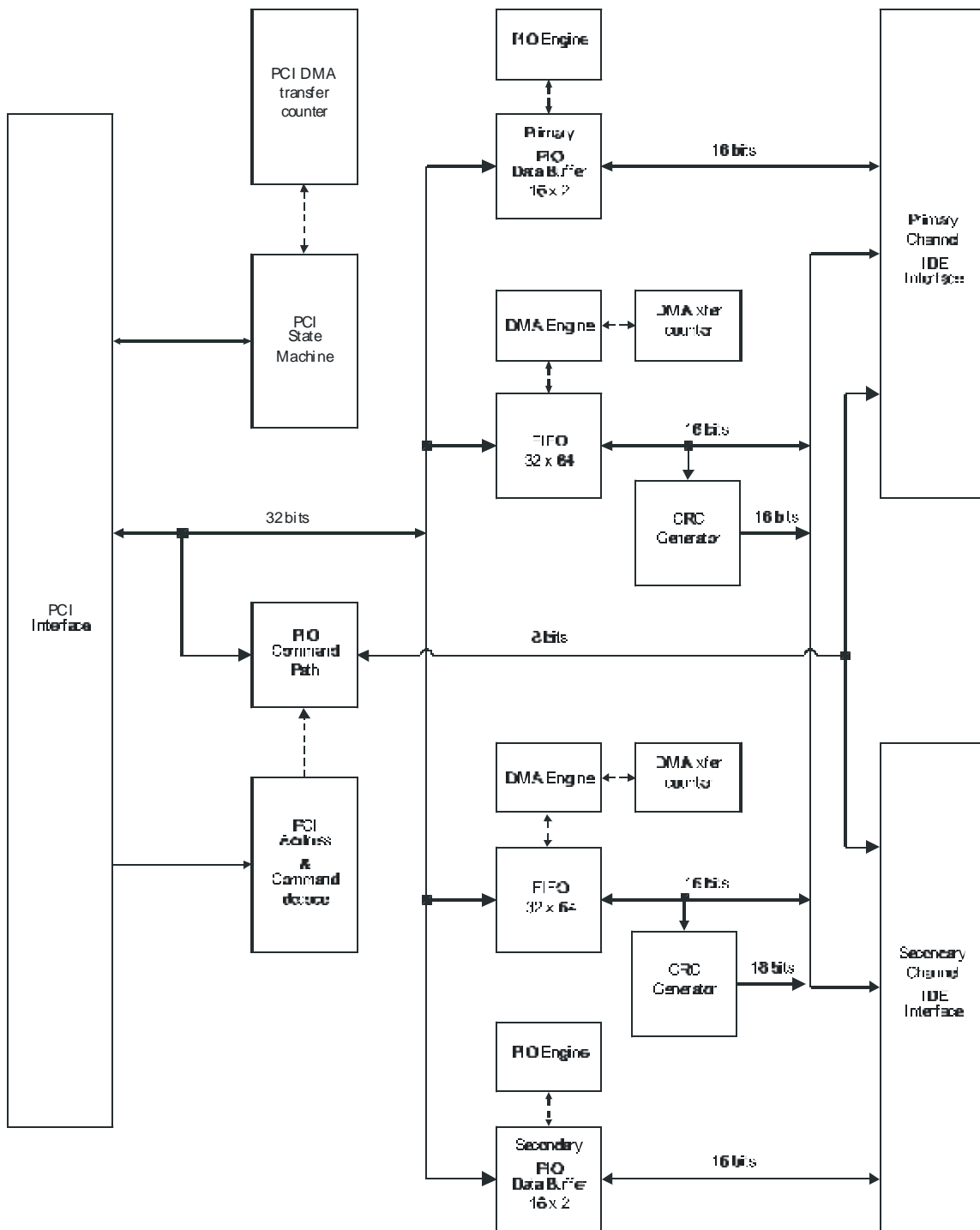


Figure 1-1: Sil 0680A Functional Block Diagram

1.7 PCI Interface

The Sil 0680A PCI interface is compliant with the PCI Local Bus Specification (Revision 2.2). PCI stands for Peripheral Component Interconnect, a high-performance and robust interconnect bus that provides a processor-independent data path between the CPU and high-speed peripherals. The PCI Specification is monitored by the PCI Special Interest Group (PCI-SIG). The PCI-SIG is an unincorporated association of members of the microcomputer industry created to monitor and enhance the development of PCI architecture and is governed by PCI-SIG bylaws ([HTTP://www.pcisig.com/](http://www.pcisig.com/)).

The Sil 0680A can act as a PCI master and a PCI slave, and contains the Sil 0680A PCI configuration space and internal registers. When the Sil 0680A needs to access shared memory, it becomes the bus master of the PCI bus and completes the memory cycle without external intervention. In the mode when it acts as a bridge between the PCI bus and the IDE/ATA bus it will behave as a PCI slave.

1.8 PCI Initialization

Generally, when a system initializes a module containing a PCI device, the configuration manager reads the configuration space of each PCI device on the PCI bus. Hardware signals select a specific PCI device based on a bus number, a slot number, and a function number. If a device that is addressed (via signal lines) responds to the configuration cycle by claiming the bus, then that function's configuration space is read out from the device during the cycle. Since any PCI device can be a multifunction device, every supported function's configuration space needs to be read from the device. Based on the information read, the configuration manager will assign system resources to each supported function within the device. Sometimes new information needs to be written into the function's configuration space. This is accomplished with a configuration write cycle.

1.9 PCI Bus Operations

Sil 0680A behaves either as a PCI master or a PCI slave device at any time and switches between these modes as required during device operation.

As a PCI slave, the Sil 0680A responds to the following PCI bus operations:

- I/O Read
- I/O Write
- Configuration Read
- Configuration Write
- Memory Read
- Memory Write

All other PCI cycles are ignored by the Sil 0680A.

As a PCI master, the Sil 0680A generates the following PCI bus operations:

- Memory Read Multiple
- Memory Read Line
- Memory Read
- Memory Write

1.10 PCI Configuration Space

This section describes how the SiI 0680A implements the required PCI configuration register space. The intent is to provide an appropriate set of configuration registers that satisfy the needs of current and anticipated system configuration mechanisms, without specifying those mechanisms or otherwise placing constraints on their use. These registers allow for:

- Full device relocation (including interrupt binding)
- Installation, configuration, and booting without user interventions
- System address map construction by device-independent software

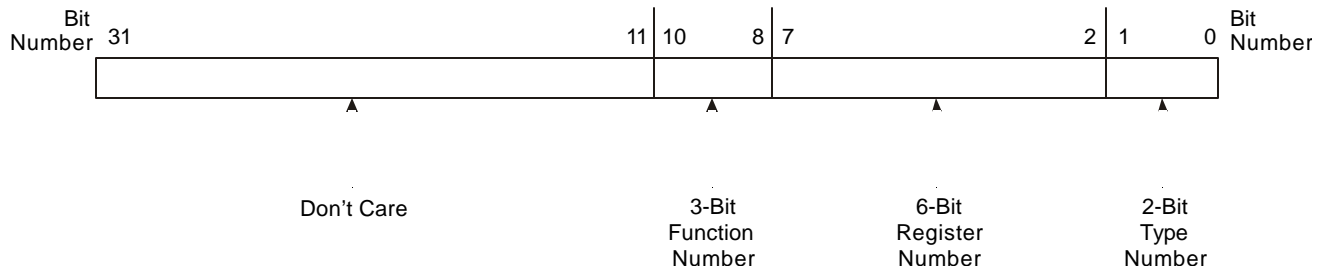


Figure 1-2: Address Lines During Configuration Cycle

SiI 0680A only responds to Type 0 configuration cycles. Type 1 cycles, which pass a configuration request on to another PCI bus, are ignored.

The address phase during a SiI 0680A configuration cycle indicates the function number and register number being addressed which can be decoded by observing the status of the address lines AD[31:0].

The value of the signal lines AD[7:2] during the address phase of configuration cycles selects the register of the configuration space to access. Valid values are between 0 and 15, inclusive. Accessing registers outside this range results in an all-0s value being returned on reads, and no action being taken on writes.

The Class Code register contains the Class Code, Sub-Class Code, and Register-Level Programming Interface registers.

All writable bits in the configuration space are reset to 0 by the hardware reset, PCI RESET (RST#) asserted. After reset, SiI 0680A is disabled and will only respond to PCI configuration write and PCI configuration read cycles.

1.11 Deviations from the Specification

The SiI 0680A product has been developed and tested to the specification listed in this document. As a result of testing and customer feedback, we may become aware of deviations to the specification that could affect the component's operation. To ensure awareness of these deviations by anyone considering the use of the SiI 0680A, we will include them in this document.

2. Electrical Characteristics

2.1 Device Electrical Characteristics

Specifications are for temperature range, 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	Ratings	Unit
VDD _H	Supply Voltage	3.6	V
V _{IN}	Input Voltage	-0.3 ~ 6.0	V
I _{OUT}	DC Output Current	16	mA

T _{STG}	Storage Temperature	-65 ~ 150	°C
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Table 2-1: Absolute Maximum Ratings

Symbol	Parameter	Condition	Type	Limits			Unit
				Min	Typ	Max	
VDD	Supply Voltage	-	-	3.0	3.3	3.6	V
IDD	Supply Current (See Sec. 2.5)	Quiescent	-	-	250	-	mA
		Operating	-	-	350	-	
V _{IH}	Input High Voltage	-	3.3V PCI	0.5xVDD	-	-	V
		-	Non-PCI	2.0	-	-	
V _{IL}	Input Low Voltage	-	3.3V PCI	-	-	0.3xVDD	V
		-	Non-PCI	-	-	0.8	
V+	Input High Voltage	-	Schmitt	-	1.8	2.3	V
V-	Input Low Voltage	-	Schmitt	0.5	0.9	-	V
V _H	Hysteresis Voltage	-	Schmitt	0.4	-	-	V
I _{IH}	Input High Current	V _{IN} = VDD	-	-10	-	10	μA
I _{IL}	Input Low Current	V _{IN} = VSS	-	-10	-	10	μA
V _{OH}	Output High Voltage	-	-	2.4	-	-	V
V _{OL}	Output Low Voltage	-	-	-	-	0.4	V
I _{oz}	3-State Leakage Current	-	-	-10	-	10	μA

Table 2-2: DC Specifications

2.2 PCI 33 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T _{VAL}	CLK to Signal Valid – Bussed Signals	2.0	11.0	ns
T _{VAL (PTP)}	CLK to Signal Valid – Point to Point	2.0	11.0	ns
T _{ON}	Float to Active Delay	2.0	-	ns
T _{OFF}	Active to Float Delay	-	28.0	ns
T _{SU}	Input Setup Time – Bussed Signals	7.0	-	ns
T _{SU (PTP)}	Input Setup Time – Point to Point	10.0	-	ns
T _H	Input Hold Time	0.0	-	ns

Table 2-3: PCI 33 MHz Timing Specifications

2.3 ATA/ATAPI-6 Slew Rate Specifications

Symbol	Parameter	Condition	Limits		Unit
			Min	Max	
S _{RISE}	Output Slew Rate – Rising	Refer to ATA Specification for specific test condition requirements	0.4	1	V/ns
S _{FALL}	Output Slew Rate – Falling	Refer to ATA Specification for specific test condition requirements	0.4	1	V/ns

Table 2-4: ATA /ATAPI-6 Slew Rate Specifications

2.4 ATA/ATAPI-6 AC/DC Specifications

Symbol	Parameter	Condition	Limits		Unit
			Min	Max	
I _{OL}	Output Sink Current	-	4	-	mA
I _{OH}	Output Source Current	-	400	-	μA
V ₊	Low-to-High Input Threshold	-	1.5	2.0	V
V ₋	High-to-Low Input Threshold	-	1.0	1.5	V
V _{OH}	Output Voltage High	-6 mA < I _{OUT} < 3 mA	VDD - 0.51	VDD+ 0.3	V
V _{OL}	Output Voltage Low	I _{OUT} = 6 mA	-	0.51	V

Table 2-5: ATA/ATAPI-6 DC Specifications

2.5 Power Supply Bypass Considerations

It is recommended that a 4-layer board (minimum) with internal Power and Ground Planes be used when integrating the SiI 0680A. Good high-speed layout techniques should be used and proper power supply bypassing is essential. Both bulk and local (high frequency) bypass capacitors should be used.

Bulk bypassing is intended to reduce the voltage noise (droop) induced by changes in load current and the inductance in the power distribution system (wires and/or etch). Since the currents vary greatly from no activity to worst case data patterns, a significant amount of capacitance is required.

All bypass capacitors should be connected to the power and ground plane with a low inductance connection (short, wide traces connecting component pad to plane).

The bulk bypass capacitor(s) should have good high frequency characteristics. A capacitor with low ESR (Equivalent Series Resistance) should be used. It should be located close to the source of +3.3V (output pin of regulator or connector pin for off board regulators). The following minimum values are recommended:

Low ESR Tantalum – 100μF

Low ESR Aluminum Electrolytic – 600μF

Local high frequency bypass should also be implemented. Capacitors should be located on all four sides of the chip close to the VDD/VSS pins. Three caps per side are recommended (12 total). Additional capacitors (x6) should be distributed evenly around the board area.

The following capacitor is recommended for local bypass:

Ceramic X7R Dielectric - 0.01μF

For a slight improvement in high frequency impedance of the bypass capacitors, two capacitors in parallel can be used for Local Bypass. The paired caps must be located as close as possible to each other. The following values are recommended for the capacitor pairs:

Ceramic X7R Dielectric - 0.1μF

Ceramic X7R Dielectric – 1000pF

3. Pin Definition

3.1 Sil 0680A Pin Listing

This section describes the pin-out of the Sil 0680A PCI-to-ATA host controller ASIC.

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
1	VSS	GND	-	-	Ground
2	PLL_VDD	PWR	-	-	PLL 3.3 Volt Power
3	PLL_CPBIAS	Analog	-	-	PLL Charge Pump Bias
4	PLL_VCOBIAS	Analog	-	-	PLL VCO Bias
5	PLL_LOOPFLT	Analog	-	-	PLL Loop Filter
6	PLL_GND	GND	-	-	PLL Ground
7	TEST_MODE	I	-	PD – 20k	ASIC Test Mode Enable
8	IDE0_DD00	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 0 / FLASH memory address bit 18
9	IDE0_DD01	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 1 / FLASH memory address bit 17
10	IDE0_DD02	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 2 / FLASH memory address bit 16
11	IDE0_DD03	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 3 / FLASH memory address bit 15
12	IDE0_DD04	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 4 / FLASH memory address bit 14
13	IDE0_DD05	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 5 / FLASH memory address bit 13
14	IDE0_DD06	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 6 / FLASH memory address bit 12
15	IDE0_DD07	I/O	ATA Buffer	PD – 100k	IDE #0 Data Bus bit 7 / FLASH memory address bit 11
16	VDD	PWR	-	-	3.3 Volt Power
17	VSS	GND	-	-	Ground
18	IDE0_DD08	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 8 / FLASH memory address bit 10
19	IDE0_DD09	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 9 / FLASH memory address bit 9

Table 3-1: Sil 0680A Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
20	IDE0_DD10	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 10 / FLASH memory address bit 8
21	IDE0_DD11	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 11 / FLASH memory address bit 7
22	IDE0_DD12	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 12 / FLASH memory address bit 6
23	IDE0_DD13	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 13 / FLASH memory address bit 5
24	IDE0_DD14	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 14 / FLASH memory address bit 4
25	IDE0_DD15	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 15 / FLASH memory address bit 3
26	VDD	PWR	-	-	3.3 Volt Power
27	VSS	GND	-	-	Ground
28	IDE0_CS0_N	I/O	12 mA	-	IDE #0 Chip Select / FLASH memory read strobe
29	IDE0_CS1_N	I/O	12 mA	-	IDE #0 Chip Select / FLASH memory write strobe
30	IDE0_DA0	I/O	12 mA	-	IDE #0 Device Address / FLASH memory address bit 2
31	IDE0_DA1	I/O	12 mA	-	IDE #0 Device Address / FLASH memory address bit 1
32	IDE0_DA2	I/O	12 mA	-	IDE #0 Device Address / FLASH memory address bit 0
33	IDE0_DIOR_N	I/O	ATA Buffer	-	IDE #0 Device I/O Read
34	IDE0_DIOW_N	I/O	ATA Buffer	-	IDE #0 Device I/O Write
35	IDE0_DMACK_N	I/O	ATA Buffer	-	IDE #0 DMA Acknowledge
36	VDD	PWR	-	-	3.3 Volt Power
37	VSS	GND	-	-	Ground
38	IDE0_CBLID_N	I-Schmitt	-	PU – 100k	IDE #0 Cable ID
39	IDE0_INTRQ	I-Schmitt	-	PD – 100k	IDE #0 Interrupt Request
40	IDE0_IORDY	I-Schmitt	-	PU – 100k	IDE #0 I/O Ready
41	IDE0_AT_REXT	Analog	-	-	IDE #0 External Bias Circuit
42	IDE0_DMARQ	I-Schmitt	-	PD – 100k	IDE #0 DMA Request
43	IDE0_RST_N	I/O	12 mA	-	IDE #0 Reset

Table 3-1: Sil 0680A Pin Listing (continued)

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
44	IDE1_DD00	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 0 / FLASH memory data bit 0
45	IDE1_DD01	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 1 / FLASH memory data bit 1
46	IDE1_DD02	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 2 / FLASH memory data bit 2
47	IDE1_DD03	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 3 / FLASH memory data bit 3
48	IDE1_DD04	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 4 / FLASH memory data bit 4
49	IDE1_DD05	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 5 / FLASH memory data bit 5
50	IDE1_DD06	I/O	ATA Buffer	PU – 100k	IDE #0 Data Bus bit 6 / FLASH memory data bit 6
51	VDD	PWR	-	-	3.3 Volt Power
52	VSS	GND	-	-	Ground
53	IDE1_DD07	I/O	ATA Buffer	PD – 100k	IDE #0 Data Bus bit 7 / FLASH memory data bit 7
54	IDE1_DD08	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
55	IDE1_DD09	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
56	IDE1_DD10	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
57	IDE1_DD11	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
58	IDE1_DD12	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
59	IDE1_DD13	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
60	IDE1_DD14	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
61	VDD	PWR	-	-	3.3 Volt Power
62	VSS	GND	-	-	Ground
63	IDE1_DD15	I/O	ATA Buffer	PU – 100k	IDE #1 Data Bus
64	IDE1_CS0_N	I/O	12 mA	-	IDE #1 Chip Select / EEPROM SCLK
65	IDE1_CS1_N	I/O	12 mA	-	IDE #1 Chip Select / EEPROM SDAT
66	IDE1_DA0	I/O	12 mA	-	IDE #1 Device Address
67	IDE1_DA1	I/O	12 mA	-	IDE #1 Device Address
68	IDE1_DA2	I/O	12 mA	-	IDE #1 Device Address

Table 3-1: Sil 0680A Pin Listing (continued)

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
69	IDE1_DIOR_N	I/O	ATA Buffer	-	IDE #1 Device I/O Read
70	IDE1_DIOW_N	I/O	ATA Buffer	-	IDE #1 Device I/O Write
71	IDE1_CBLID_N	I-Schmitt	-	PU – 100k	IDE #1 Cable ID
72	VDD	PWR	-	-	3.3 Volt Power
73	VSS	GND	-	-	Ground
74	IDE1_DMACK_N	I/O	ATA Buffer	-	IDE #1 DMA Acknowledge
75	IDE1_INTRQ	I-Schmitt	-	PD – 100k	IDE #1 Interrupt Request
76	IDE1_IORDY	I-Schmitt	-	PU – 100k	IDE #1 I/O Ready
77	IDE1_AT_REXT	Analog	-	-	IDE #1 External Bias Circuit
78	IDE1_DMARQ	I-Schmitt	-	PD – 100k	IDE #1 DMA Request
79	IDE1_RST_N	I/O	12 mA	-	IDE #1 Reset
80	JP	I	-	PU – 20k	IDE Configuration Jumper
81	PCI_AD31	I/O	PCI	-	PCI Address/Data
82	PCI_AD30	I/O	PCI	-	PCI Address/Data
83	PCI_AD29	I/O	PCI	-	PCI Address/Data
84	PCI_AD28	I/O	PCI	-	PCI Address/Data
85	PCI_AD27	I/O	PCI	-	PCI Address/Data
86	PCI_AD26	I/O	PCI	-	PCI Address/Data
87	VDD	PWR	-	-	3.3 Volt Power
88	VSS	GND	-	-	Ground
89	PCI_AD25	I/O	PCI	-	PCI Address/Data
90	PCI_AD24	I/O	PCI	-	PCI Address/Data
91	PCI_CBE3	I/O	PCI	-	PCI Command/Byte Enable
92	PCI_IDSEL	I	-	-	PCI ID Select
93	PCI_AD23	I/O	PCI	-	PCI Address/Data
94	PCI_AD22	I/O	PCI	-	PCI Address/Data
95	PCI_AD21	I/O	PCI	-	PCI Address/Data
96	PCI_AD20	I/O	PCI	-	PCI Address/Data
97	PCI_AD19	I/O	PCI	-	PCI Address/Data
98	VDD	PWR	-	-	3.3 Volt Power
99	VSS	GND	-	-	Ground

Table 3-1: Sil 0680A Pin Listing (continued)

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
100	PCI_AD18	I/O	PCI	-	PCI Address/Data
101	PCI_AD17	I/O	PCI	-	PCI Address/Data
102	PCI_AD16	I/O	PCI	-	PCI Address/Data
103	PCI_CBE2	I/O	PCI	-	PCI Command/Byte Enable
104	PCI_FRAME_N	I/O	PCI	-	PCI Frame
105	PCI_IRDY_N	I/O	PCI	-	PCI Initiator Ready
106	PCI_TRDY_N	I/O	PCI	-	PCI Target Ready
107	PCI_DEVSEL_N	I/O	PCI	-	PCI Device Select
108	VDD	PWR	-	-	3.3 Volt Power
109	VSS	GND	-	-	Ground
110	PCI_STOP_N	I/O	PCI	-	PCI Stop
111	PCI_PERR_N	I/O	PCI	-	PCI Parity Error
112	PCI_SERR_N	OD	PCI	-	PCI System Error
113	PCI_PAR	I/O	PCI	-	PCI Parity
114	PCI_CBE1	I/O	PCI	-	PCI Command/Byte Enable
115	PCI_AD15	I/O	PCI	-	PCI Address/Data
116	PCI_AD14	I/O	PCI	-	PCI Address/Data
117	PCI_AD13	I/O	PCI	-	PCI Address/Data
118	VDD	PWR	-	-	3.3 Volt Power
119	VSS	GND	-	-	Ground
120	PCI_AD12	I/O	PCI	-	PCI Address/Data
121	PCI_AD11	I/O	PCI	-	PCI Address/Data
122	PCI_AD10	I/O	PCI	-	PCI Address/Data
123	PCI_AD09	I/O	PCI	-	PCI Address/Data
124	PCI_AD08	I/O	PCI	-	PCI Address/Data
125	PCI_CBE0	I/O	PCI	-	PCI Command/Byte Enable
126	PCI_AD07	I/O	PCI	-	PCI Address/Data
127	PCI_AD06	I/O	PCI	-	PCI Address/Data
128	VDD	PWR	-	-	3.3 Volt Power
129	VSS	GND	-	-	Ground
130	PCI_AD05	I/O	PCI	-	PCI Command/Byte Enable

Table 3-1: Sil 0680A Pin Listing (continued)

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
131	PCI_AD04	I/O	PCI	-	PCI Command/Byte Enable
132	PCI_AD03	I/O	PCI	-	PCI Command/Byte Enable
133	PCI_AD02	I/O	PCI	-	PCI Command/Byte Enable
133	PCI_AD02	I/O	PCI	-	PCI Command/Byte Enable
134	PCI_AD01	I/O	PCI	-	PCI Command/Byte Enable
135	PCI_AD00	I/O	PCI	-	PCI Command/Byte Enable
136	PCI_REQ_N	T	PCI	-	PCI Bus Request
137	PCI_GNT_N	I	-	-	PCI Bus Grant
138	PCI_INTA_N	OD	PCI	-	PCI Interrupt
139	BA5_EN	I	-	-	Base Address 5 Enable Jumper
140	PCI_CLK	I	-	-	PCI Clock
141	PCI_RST_N	I-Schmitt	-	-	PCI Reset
142	SCAN_EN	I	-	PD – 20k	Internal Scan Enable
143	MEM_CS_N	I/O	4 mA	-	Memory Chip Select
144	VDD	PWR	-	-	3.3 Volt Power

Table 3-1: Sil 0680A Pin Listing (continued)

Pin Type	Pin Description
I	Input Pin with LVTTTL Thresholds
I-Schmitt	Input Pin with Schmitt Trigger
O	Output Pin
T	Tri-state Output Pin
I/O	Bidirect Pin
OD	Open Drain Output Pin

3.2 Sil 0680A Pin Diagram

The Sil 0680A pin diagram is shown in Figure 3-1.

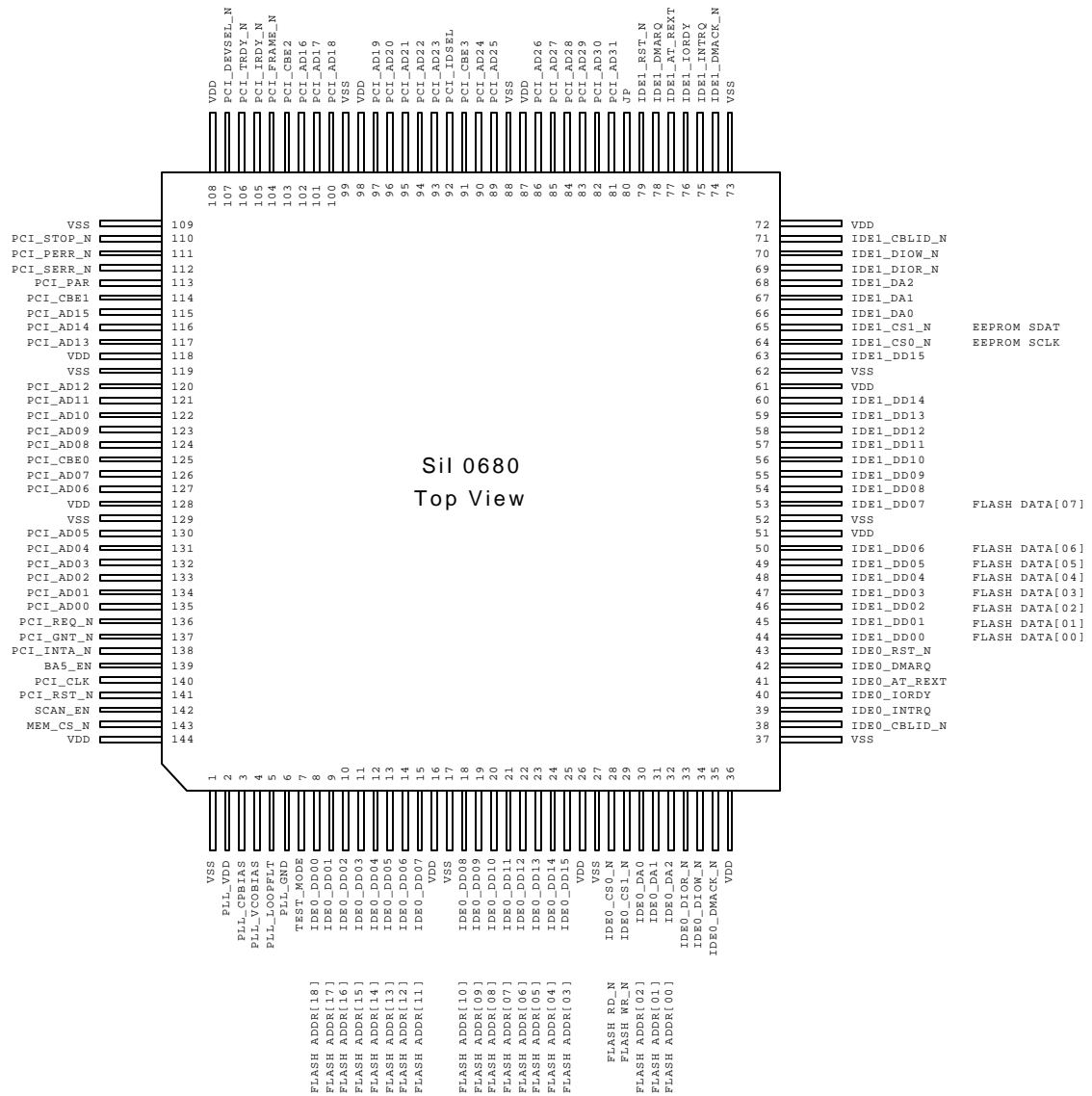


Figure 3-1: Sil 0680A Pin Diagram

3.3 Sil 0680A Pin Descriptions

3.3.1 IDE/ATA Primary Channel

IDE0 Disk Data Bus

Pin Names: IDE0_DD[15..0]

Pin Numbers: 25, 24, 23, 22, 21, 20, 19, 18, 15, 14, 13, 12, 11, 10, 9, 8

Disk Data bits 0 through 15 are the 16-bit bi-directional data bus which connects to the ATA device(s). IDE0_DD[15:0] are data signals to the primary Channel. IDE0_DD[7:0] defines the low byte while IDE0_DD[15:8] defines the high byte of this 16-bit data register. The data bus is normally in a high impedance state and is driven by the Sil 0680A during the IDE0_DIOW_N command pulse in either single/multi-word DMA mode, or valid at every edge of IDE0_DIOR_N (HSTROBE) or IDE0_IORDY (DSTROBE) in Ultra DMA mode. IDE0_DD[7] is a multifunction pin which allows a host to recognize the absence of an ATA/ATAPI device at power- I-down resistor be connected to this pin.

IDE0 Chip Select

Pin Names: IDE0_CS0_N; IDE0_CS1_N

Pin Numbers: 28, 29

These are the chip select signals from the host used to select the Command Block or Control Block registers. When IDE0_DMACK_N is asserted, IDE0_CS0_N and IDE0_CS1_N shall be negated and transfers shall be 16 bits wide.

IDE0 Disk Address

Pin Names: IDE0_DA[2..0]

Pin Numbers: 32, 31, 30

Disk Address bits 0 through 2 are normally outputs to the ATA connector selecting the register in the drive's Command Block register. IDE0_DA[2:0] sends address signals to the primary channel. These address signals are decoded from the PCI_AD[2:0] and PCI_CBE[3:0] inputs.

IDE0 Disk I/O Read

Pin Name: IDE0_DIOR_N

Pin Number: 33

Primary Channel Disk I/O Read is an active low output which enables data to be read from the drive. The duration and repetition rate of IDE0_DIOR_N cycles is determined by Sil 0680A programming. IDE0_DIOR_N to the primary channel is driven high when inactive. This signal is defined as HSTROBE in Ultra DMA write mode to write data to the primary channel drive. This signal is also defined as primary channel HDMARDY_N in Ultra DMA read mode.

IDE0 Disk I/O Write

Pin Name: IDE0_DIOW_N

Pin Number: 34

Primary Channel Disk I/O Write is an active low output that enables data to be written to the drive. The duration and repetition of IDE0_DIOW_N cycles is determined by Sil 0680A Programming. IDE0_DIOW_N to the primary channel is driven high when inactive. This signal is defined as primary channel STOP in ultra DMA mode.

IDE0 DMA Acknowledge

Pin Name: IDE0_DMACK_N

Pin Number: 35

This signal is normally used by the Sil 0680A in response to IDE0_DMARQ to either acknowledge that the primary channel is ready to accept data, or that data is available. This signal is also used to write CRC code to the primary channel drive at the end of each Ultra DMA burst transfer.

IDE0 Cable Detect

-up resistor is recommended. This signal is defined as DSTROBE in Ultra DMA read mode to read data from the currently selected drive to the primary channel. This signal is also defined as DDMARDY_N in Ultra DMA write mode.

IDE0 External Bias Circuit

Pin Name: IDE0_AT_REXT

Pin Number: 41

IDE0_AT_REXT is an analog pin for connection to an external bias circuit. This pin is sensitive to noise and must be routed carefully. Keep the trace length on this pin as short as possible and away from any sources of noise.

IDE0 DMA Request

Pin Name: IDE0_DMARQ

Pin Number: 42

This signal is used in a handshake manner with IDE0_DMACK_N, and shall be asserted high by the currently selected drive attached to the primary IDE/ATA Channel when it is ready to transfer data to or from the host. This pin should have a 5.6 KΩ pull-down resistor connected to it.

IDE0 Disk Reset

Pin Name: IDE0_RST_N

Pin Number: 43

IDE0 Disk Reset is an active low output which signals the IDE/ATA drive to initialize its control register. IDE0_RST_N is a buffered version of the PCI_RST_N input. It can also be generated by programming the Si1 0680A register and connects directly to the ATA connector. IDE0_RST_N asserts reset to the primary IDE/ATA channel.

3.3.2 IDE/ATA Secondary Channel

IDE1 Disk Data Bus

Pin Names: IDE1_DD[15..0]

Pin Numbers: 63, 60, 59, 58, 57, 56, 55, 54, 53, 50, 49, 48, 47, 46, 45, 44

Disk Data bits 0 through 15 are the 16-bit bi-directional data bus, which connects to the IDE/ATA device(s). IDE1_DD[15:0] are data signals to the secondary channel. IDE1_DD[7:0] defines the low data byte while IDE1_DD[15:8] defines the high data byte of this 16-bits data register. The data bus is normally in a high impedance state and is driven by the Si1 0680A during the IDE1_DIOW_N command pulse in either single/multi-word DMA mode, or valid at every edge of IDE1_DIOR_N (HSTROBE) or IDE1_IORDY (DSTROBE) in Ultra DMA mode. IDE1_DD07 is a multifunction pin, which allows a host to recognize the absence of an ATA/ATAPI device at power-up. A pull-down resistor is recommended to be connected to this pin.

IDE1 Chip Select

Pin Names: IDE1_CS0_N; IDE1_CS1_N

Pin Numbers: 64, 65

These are the chip select signals from the host used to select the Command Block or Control Block registers. When IDE1_DMACK_N is asserted, IDE1_CS0_N and IDE1_CS1_N shall be negated and transfers shall be 16 bits wide.

IDE1 Disk Address

Pin Names: IDE1_DA[2..0]

Pin Numbers: 68, 67, 66

Disk Address bits 0 through 2 are normally outputs to the ATA connector to select the register in the drive's Command Block register. IDE1_DA [2:0] sends address signals to the secondary channel. These address signals are decoded from the PCI_AD[2:0] and PCI_CBE[3:0] inputs.

IDE1 Disk I/O Read

Pin Name: IDE1_DIOR_N

Pin Number: 69

This is an active low output which enables data to be read from the drive. The duration and repetition rate of IDE1_DIOR_N cycles is determined by programming the Sil 0680A PIO timing registers. IDE1_DIOR_N to the secondary channel is driven high when inactive. This signal is defined as HSTROBE in Ultra DMA write mode to write data to the secondary channel drive. This signal is also defined as secondary channel HDMARDY_N in Ultra DMA read mode.

IDE1 Disk I/O Write

Pin Name: IDE1_DIOW_N

Pin Number: 70

This is an active low output that enables data to be written to the drive. The duration and repetition rate of IDE1_DIOW_N cycles is determined by programming the Sil 0680A PIO timing registers. IDE1_DIOW_N to the Secondary channel is driven high when inactive. This signal is also defined as secondary channel STOP in Ultra DMA mode.

IDE1 Cable Detect

Pin Names: IDE1_CBLID_N

Pin Number: 71

IDE1_CBLID_N (Cable Detect) determines the type of cable attached to the primary channel. In general, a low on this pin indicates that a 40 conductor cable is attached. A high indicates that an 80 conductor cable is attached. Refer to the ATA/ATAPI-6 Specification for complete details.

IDE1 DMA Acknowledge

Pin Name: IDE1_DMACK_N

Pin Number: 74

This signal is normally used by the Sil 0680A in response to IDE1_DMARQ to either acknowledge that the secondary channel is ready to accept data, or that data is available. This signal is also used to write CRC code to the secondary channel drive at the end of each Ultra DMA burst transfer.

IDE1 Interrupt Request

Pin Name: IDE1_INTRQ

Pin Number: 75

Primary channel interrupt request is an input signal used to generate the PCI_INTA_N output. This input should have a 10k Ω pull-down resistor connected to it.

IDE1 I/O Ready

Pin Name: IDE1_IORDY

Pin Number: 76

The Secondary Channel Drive Channel's Initiator Ready is an active high input. It indicates that the ATA disk drive has -up resistor is recommended. This signal is defined as DSTROBE in Ultra DMA read mode to read data from the currently selected drive attached to the secondary channel. This signal is also defined as DDMARDY_N in Ultra DMA write mode.

IDE1 External Bias Circuit

Pin Name: IDE1_AT_REXT

Pin Number: 77

IDE1_AT_REXT is an analog pin for connection to an external bias circuit. This pin is sensitive to noise and must be routed carefully. Keep the trace length on this pin as short as possible and away from any sources of noise.

IDE1 DMA Request

Pin Name: IDE1_DMARQ

Pin Number: 78

This signal is used in a handshake manner with IDE1_DMACK_N and shall be asserted high by the currently selected drive attached to the secondary IDE/ATA channel when it is ready to transfer data to or from the host. . This pin should have a 5.6 K Ω pull-down resistor connected to it.

IDE1 Disk Reset

Pin Name: IDE1_RST_N

Pin Number: 79

Disk Reset is an active low output which signals the IDE/ATA drive to initialize its control register. IDE1_RST_N is a buffered version of the PCI_RST_N input. It can also be generated by programming the Sil 0680A register, and connects directly to the ATA connector. IDE1_RST_N asserts reset to the secondary ATA channel.

3.3.3 PCI 33MHz 32-bit Section

PCI Address and Data

Pin Names: PCI_AD[31..0]

Pin Numbers: 81~86, 89, 90, 93~97, 100~102, 115~117, 120~124, 126, 127, 130~135

Address and Data buses are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the first clock cycle in which PCI_FRAME_N signal is asserted. During the address phase, PCI_AD[31:0] contain a physical address (32 bits). For I/O, this can be a byte address. For configuration and memory it is a DWORD address. During data phases, PCI_AD[7:0] contain the least significant byte (LSB) and PCI_AD[31:24] contain the most significant byte (MSB). Write data is stable and valid when PCI_IRDY_N is asserted; read data is stable and valid when PCI_TRDY_N is asserted. Data is transferred during those clocks where both PCI_IRDY_N and PCI_TRDY_N are asserted.

PCI Command and Byte Enables

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Pin Names: PCI_CBE[3..0]

Pin Numbers: 91, 103, 114, 125

Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, PCI_CBE[3:0]_N define the bus command. During the data phase, PCI_CBE[3:0]_N are used as Byte Enables. Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.

PCI ID Select

Pin Name: PCI_IDSEL

Pin Number: 92

This signal is used as a chip select during configuration read and write transactions.

PCI Frame Cycle

Pin Name: PCI_FRAME_N

Pin Number: 104

Cycle Frame is driven by the current master to indicate the beginning and duration of an access. PCI_FRAME_N is asserted to indicate that a bus transaction is beginning. While PCI_FRAME_N is asserted, data transfers continue. When PCI_FRAME_N is de-asserted, the transaction is in the final data phase or has completed.

PCI Initiator Ready

Pin Name: PCI_IRDY_N

Pin Number: 105

Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with PCI_TRDY_N. A data phase is completed on any clock when both PCI_IRDY_N and PCI_TRDY_N are sampled as asserted. Wait cycles are inserted until both PCI_IRDY_N and PCI_TRDY_N are asserted together.

PCI Target Ready

Pin Name: PCI_TRDY_N

Pin Number: 106

Target Ready indicates the target agent's ability to complete the current data phase of the transaction. PCI_TRDY_N is used with PCI_IRDY_N. A data phase is completed on any clock when both PCI_TRDY_N and PCI_IRDY_N are sampled asserted. During a read, PCI_TRDY_N indicates that valid data is present on PCI_AD[31:0]. During a write, it indicates the target is prepared to accept data.

PCI Device Select

Pin Name: PCI_DEVSEL_N

Pin Number: 107

Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, PCI_DEVSEL_N indicates to a master whether any device on the bus has been selected.

PCI Stop

Pin Name: PCI_STOP_N

Pin Number: 110

PCI_STOP_N indicates the current target is requesting that the master stop the current transaction.

PCI Parity Error

Pin Name: PCI_PERR_N

Pin Number: 111

PCI_PERR_N indicates a data parity error between the current master and target on PCI. On a write transaction, the target always signals data parity errors back to the master on PCI_PERR_N. On a read transaction, the master asserts PCI_PERR_N to indicate to the system that an error was detected.

PCI System Error

Pin Name: PCI_SERR_N

Pin Number: 112

System Error is for reporting address parity errors, data parity errors on Special Cycle Command, or any other system error where the result will be catastrophic. The PCI_SERR_N is a pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of PCI_SERR_N is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of PCI_SERR_N to the de-asserted state is accomplished by a weak pull-up. Note that if an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

PCI Parity

Pin Name: PCI_PAR

Pin Number: 113

PCI_PAR is even parity across PCI_AD[31:0] and PCI_CBE[3:0]_N. Parity generation is required by all PCI agents. PCI_PAR is stable and valid one clock after the address phase. For data phases PCI_PAR is stable and valid one clock after either PCI_IRDY_N is asserted on a write transaction or PCI_TRDY_N is asserted on a read transaction. Once PCI_PAR is valid, it remains valid until one clock after the completion of the current data phase. (PCI_PAR has the same timing as PCI_AD[31:0] but delayed by one clock.)

PCI Request

Pin Name: PCI_REQ_N

Pin Number: 136

This signal indicates to the arbiter that this agent desires use of the PCI bus.

PCI Grant

Pin Name: PCI_GNT_N

Pin Number: 137

This signal indicates to the agent that access to the PCI bus has been granted. In response to a PCI request, this is a point-to-point signal. Every master has its own PCI_GNT_N, which must be ignored while PCI_RST_N is asserted.

PCI Interrupt A

Pin Name: PCI_INTA_N

Pin Number: 138

Interrupt A is used to request an interrupt on the PCI bus. PCI_INTA_N is open collector and is an open drain output.

PCI Clock Signal

Pin Names: PCI_CLK

Pin Number: 140

Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals (except PCI_RST_N, and PCI_INTA_N) are sampled on the rising edge of PCI_CLK. All other timing parameters are defined with respect to this edge.

PCI Reset

Pin Name: PCI_RST_N

Pin Number: 141

PCI_RST_N is an active low input that is used to set the internal registers to their initial state. PCI_RST_N is typically the system power-on reset signal as distributed on the PCI bus.

3.3.4 Miscellaneous I/O

Ground

Pin Name: VSS

Pin Number: 1, 17, 27, 37, 52, 62, 73, 88, 99, 109, 119, 129

Ground reference point to power supply.

PLL VDD

Pin Name: PLL_VDD

Pin Number: 2

Dedicated PLL Power supply (3.3 Volts +/- 10%). Refer to section 7.1 for PLL connections.

PLL Charge Pump Bias

Pin Name: PLL_CPBIAS

Pin Number: 3

Dedicated PLL analog pin for charge pump bias. Refer to section 7.1 for PLL connections.

PLL VCO Bias

Pin Name: PLL_VCOBIAS

Pin Number: 4

Dedicated PLL analog pin for VCO bias. Refer to section 7.1 for PLL connections.

PLL Loop Filter

Pin Name: PLL_LOOPFLT

Pin Number: 5

Dedicated PLL analog input for off-chip loop filter. Refer to section 7.1 for PLL connections.

PLL Ground

Pin Name: PLL_GND

Pin Number: 6

Dedicated PLL Ground (Power supply reference). Refer to section 7.1 for PLL connections.

Test Mode

Pin Name: TEST_MODE

Pin Number: 7

This pin, in conjunction with other pins, enables various test functions within the device. This pin should be tied to ground for normal operation.

Power Supply

Pin Name(s): VDD
Pin Number(s): 16, 26, 36, 51, 61, 72, 87, 98, 108, 118, 128 and 144
Power Supply Input (3.3 volts +/- 10%)

IDE Configuration

Pin Names: JP
Pin Numbers: 80
IDE Configuration Jumper Pin.

JP Pin	CONFIGURATION
0	RAID Class, PCI Class Code = 010400h
1	IDE Class, PCI Class Code = 010185h

Table 3-2: ATA Configuration

This pin has an internal pull-up resistor, and if left unconnected, will default to '1'. Otherwise, tie this pin high (1,) or low (0) to select the desired mode.

It is recommended that this pin to be tied to low (RAID Class) when Silicon Image drivers (RAID or Non-RAID) are used.

Base Address 5 Enable

Pin Name: BA5_EN
Pin Number: 139
Base Address 5 Enable Jumper Pin.

BA5_EN Pin	CONFIGURATION
0	Base Address 5 Disabled (Note 1)
1	Base Address 5 Enabled

Table 3-3: Base Address 5 Configuration

Note 1: Reading Base Address 5 returns all zeroes.

This pin does not have an internal resistor and therefore must be tied high (1) or low (0) to select the desired mode.

It is recommended that this pin is enabled (tied high)() for all configurations.

Internal Scan Enable

Pin Name: SCAN_EN
Pin Number: 142
This pin when active (high) will place all scan flip-flops into a scan mode. This pin should be tied to ground for normal operation.

Memory Chip Select

Pin Name: MEM_CS_N
Pin Number: 143
This pin is used to select and enable the external memory. It is active low.

4. Package Drawing

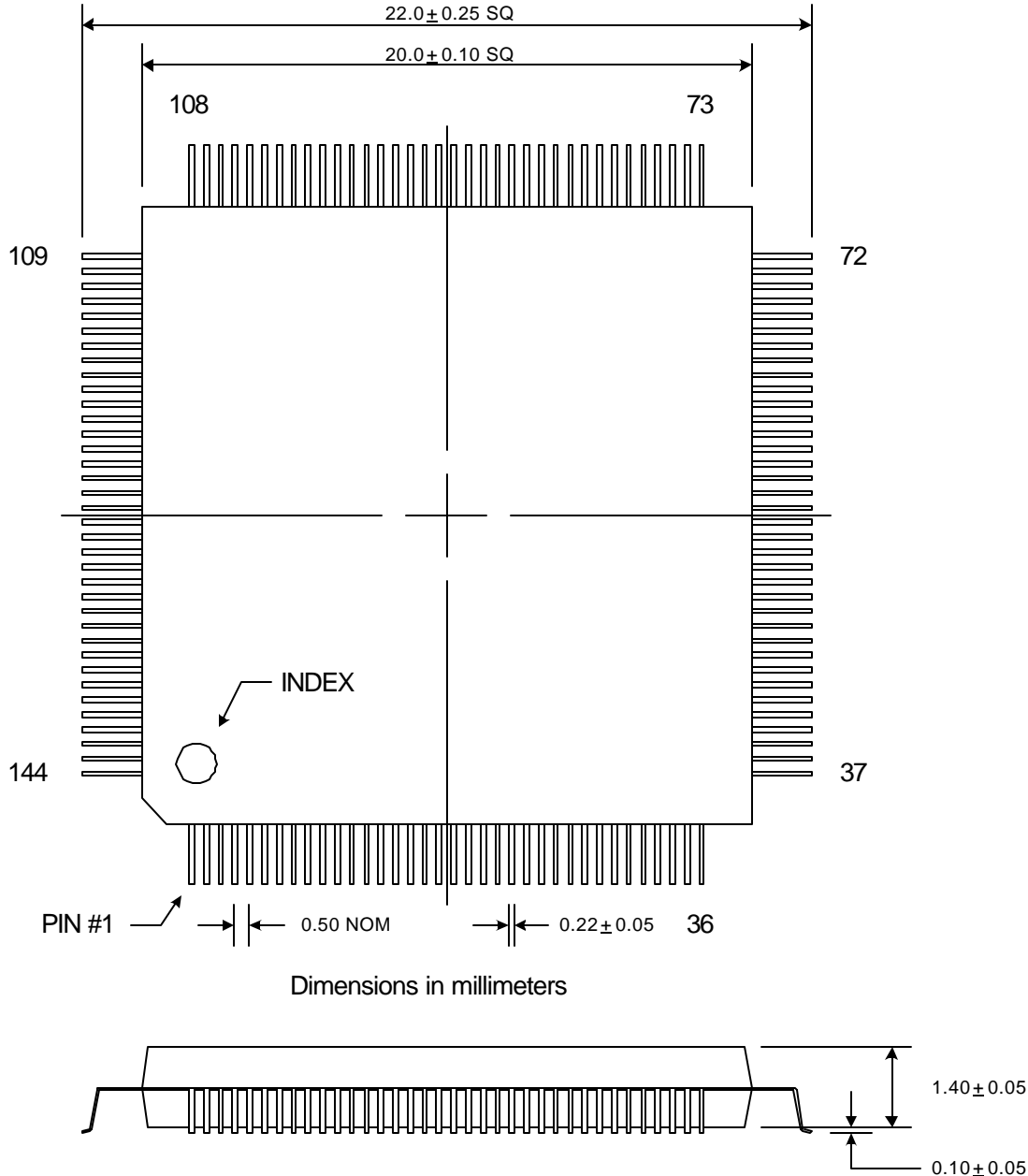


Figure 4-1: Package Drawing – 144 LQFP

5. ASIC Block Diagram

The Sil 0680A ASIC contains the major logic modules shown in Figure 5-1.

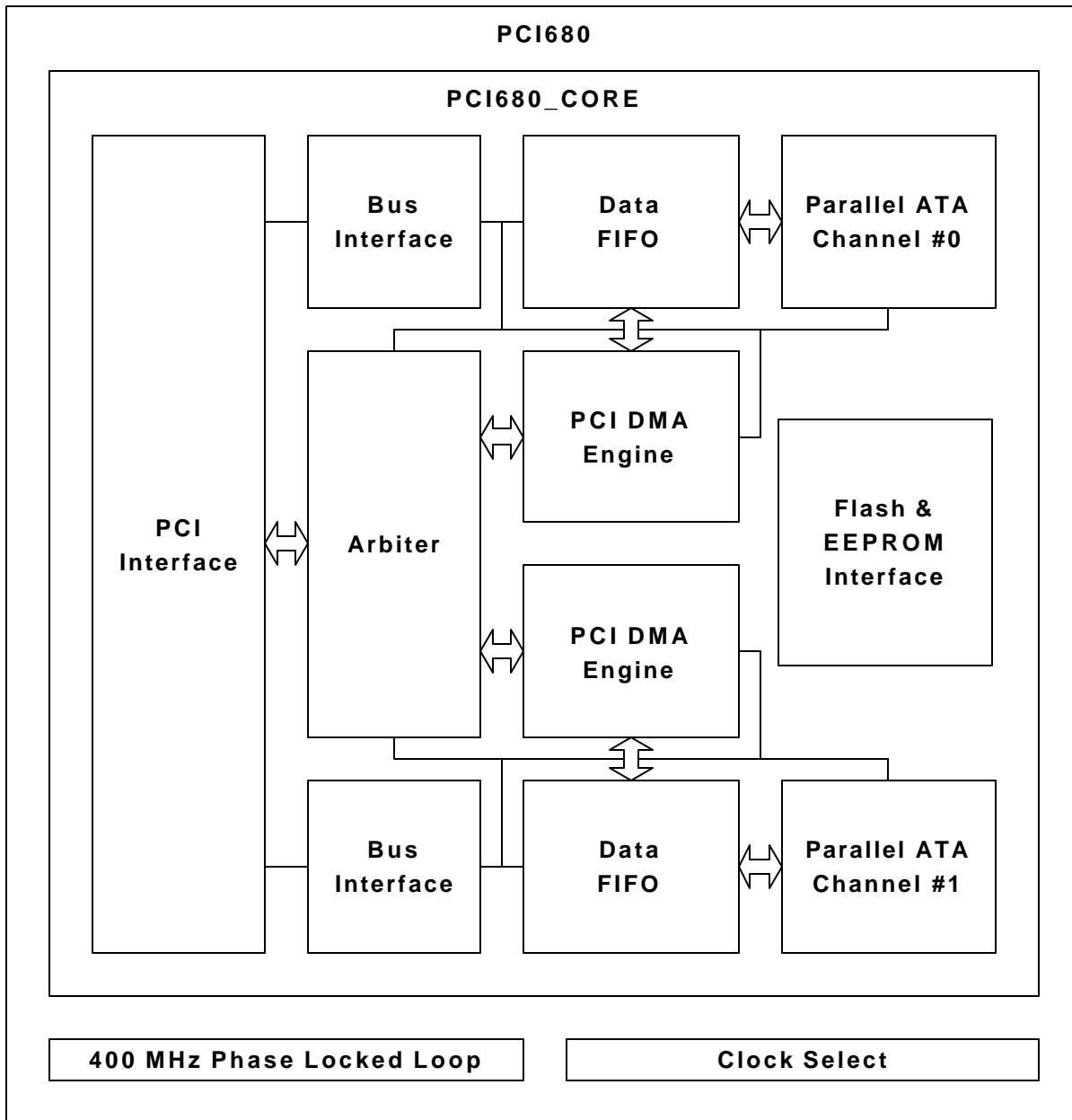


Figure 5-1: Sil 0680A ASIC Block Diagram

PCI Bus	Bits	Type	Description
PCI_AD[31:00]	32	I/O	PCI address/data bus
PCI_CBE[3:0]	4	I/O	PCI command/byte enables
PCI_IDSEL	1	I	PCI ID select
PCI_FRAME_N	1	I/O	PCI FRAME# signal
PCI_IRDY_N	1	I/O	PCI IRDY# signal
PCI_TRDY_N	1	I/O	PCI TRDY# signal
PCI_STOP_N	1	I/O	PCI STOP# signal
PCI_DEVSEL_N	1	I/O	PCI DEVSEL# signal
PCI_PAR	1	I/O	PCI parity bit
PCI_PERR_N	1	I/O	PCI parity error signal
PCI_SERR_N	1	OD	PCI system error signal
PCI_REQ_N	1	T	PCI bus request
PCI_GNT_N	1	I	PCI bus grant
PCI_M66EN	1	I	PCI 66 MHz enable
PCI_CLK	1	I	PCI clock
PCI_RST_N	1	I	PCI bus reset

Table 5-1: PCI Bus Signals Group

IDE Channel #0	Bits	Type	Description
IDE0_DD[15:00]	16	I/O	IDE data bus
IDE0_CS0_N	1	I/O	IDE chip select
IDE0_CS1_N	1	I/O	IDE chip select
IDE0_DA0	1	I/O	IDE device address
IDE0_DA1	1	I/O	IDE device address
IDE0_DA2	1	I/O	IDE device address
IDE0_DIOR_N	1	I/O	IDE device IO read
IDE0_DIOW_N	1	I/O	IDE device IO write
IDE0_DMACK_N	1	I/O	IDE DMA acknowledge
IDE0_CBLID_N	1	I	IDE cable ID
IDE0_INTRQ	1	I	IDE interrupt request
IDE0_IORDY	1	I	IDE IO channel ready
IDE0_AT_REXT	1	I/O	IDE external bias circuit
IDE0_DMARQ	1	I	IDE DMA request
IDE0_RST_N	1	I/O	IDE reset

Table 5-2: IDE Channel #0 Signals Group

IDE Channel #1	Bits	Type	Description
IDE1_DD[15:00]	16	I/O	IDE data bus
IDE1_CS0_N	1	I/O	IDE chip select
IDE1_CS1_N	1	I/O	IDE chip select
IDE1_DA0	1	I/O	IDE device address
IDE1_DA1	1	I/O	IDE device address
IDE1_DA2	1	I/O	IDE device address
IDE1_DIOR_N	1	I/O	IDE device IO read
IDE1_DIOW_N	1	I/O	IDE device IO write
IDE1_DMACK_N	1	I/O	IDE DMA acknowledge
IDE1_CBLID_N	1	I	IDE cable ID
IDE1_INTRQ	1	I	IDE interrupt request
IDE1_IORDY	1	I	IDE IO channel ready
IDE1_AT_REXT	1	I/O	IDE external bias circuit

IDE1_DMARQ	1	I	IDE DMA request
IDE1_RST_N	1	I/O	IDE reset

Table 5-3: IDE Channel #1 Signals Group

FLASH Interface	Bits	Type	Description
IDE0_DD[07]	1	O	FLASH memory address bit 18
IDE0_DD[05]	1	O	FLASH memory address bit 17
IDE0_DD[08]	1	O	FLASH memory address bit 16
IDE0_DD[09]	1	O	FLASH memory address bit 15
IDE0_DD[04]	1	O	FLASH memory address bit 14
IDE0_DD[03]	1	O	FLASH memory address bit 13
IDE0_DD[10]	1	O	FLASH memory address bit 12
IDE0_DD[00]	1	O	FLASH memory address bit 11
IDE0_DA2	1	O	FLASH memory address bit 10
IDE0_DD[01]	1	O	FLASH memory address bit 09
IDE0_DD[02]	1	O	FLASH memory address bit 08
IDE0_DD[11]	1	O	FLASH memory address bit 07
IDE0_DD[12]	1	O	FLASH memory address bit 06
IDE0_DD[13]	1	O	FLASH memory address bit 05
IDE0_DD[14]	1	O	FLASH memory address bit 04
IDE0_DD[15]	1	O	FLASH memory address bit 03
IDE0_DA0	1	O	FLASH memory address bit 02
IDE0_CS0_N	1	O	FLASH memory address bit 01
IDE0_CS1_N	1	O	FLASH memory address bit 00
IDE1_DD[07]	1	I/O	FLASH memory data bit 07
IDE1_DD[06]	1	I/O	FLASH memory data bit 06
IDE1_DD[05]	1	I/O	FLASH memory data bit 05
IDE1_DD[04]	1	I/O	FLASH memory data bit 04
IDE1_DD[11]	1	I/O	FLASH memory data bit 03
IDE1_DD[10]	1	I/O	FLASH memory data bit 02
IDE1_DD[09]	1	I/O	FLASH memory data bit 01
IDE1_DD[08]	1	I/O	FLASH memory data bit 00
IDE0_DA1	1	O	FLASH memory read strobe
IDE0_DD[06]	1	O	FLASH memory write strobe
MEM_CS_N	1	O	FLASH memory chip select

Table 5-4: SiI 0680A FLASH Memory Signals Group – Shared Signals

EEPROM Interface	Bits	Type	Description
IDE1_CS1_N	1	O	EEPROM serial data
IDE1_CS0_N	1	O	EEPROM serial clock

Table 5-5: SiI 0680A EEPROM Memory Signals Group – Shared Signals

Test Mode Signals	Bits	Type	Description
SCAN_EN	1	I	ASIC internal scan mode enable
TEST_MODE	1	I	ASIC test mode enable

Table 5-6: Sil 0680A Test Signals Group