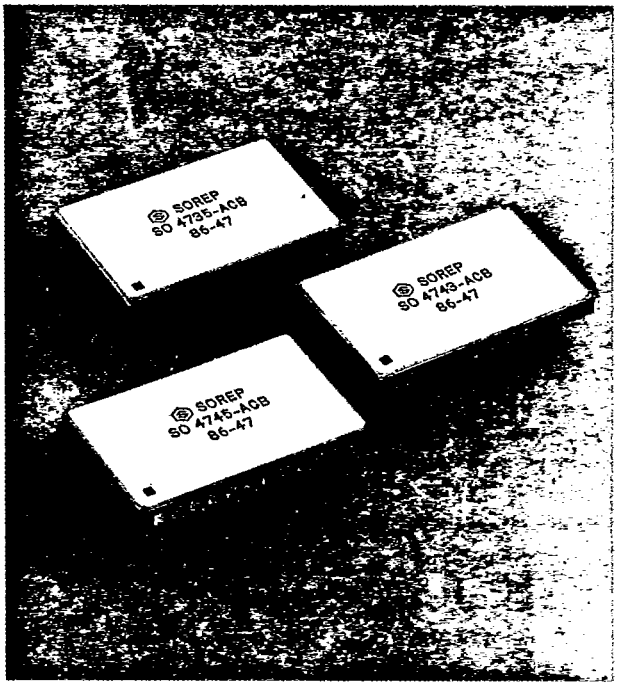
SO 4735 A/4743 A/4745 A

VOLTAGE TO FREQUENCY CONVERTERS

T-73-13-03

FEATURES

- 1 MHz (4735 A), 10 MHz (4743 A), 15 MHz (4745 A) Full-scale outputs.
- Full differential input.
- 0.006% (4735 A), 0.024% (4743 A), 0.048% (4745 A) non-linearity.
- 100 dB Dynamic range.
- 24 pin hermetic DIL.
- TTL and open collector output.



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APPLICATIONS

- Two-wire digital data transmission.
- Ratiometric data conversion.
- Fiber optic data links.
- Telemetry.
- Data recording.
- Instrumentation.

DESCRIPTION

The SO 4735 A / 4743 A / 4745 A is a family of voltage to frequency converters which offer high accuracy (0.006%, 0.024%, 0.048% respectively) and high full-scale capability (1 MHz, 10 MHz, 15 MHz respectively). They have full differential input capabilities and can be driven with positive and negative voltages, and positive currents. The output stage of the units contains an open collector transistor, with internal pull-up resistors for TTL compatibility (Fan-out = 10 TTL loads). Short response time (15 μS), coupled with wide input range (+ 100 μV to 10 V) makes the units suitable for applications where high resolution over a wide dynamic range is required. Full scale error and offset error are externally trimmable. These very accurate voltage to frequency converters are convenient for applications like modulation-demodulation, data links, isolation coupling, data conversion, instrumentation, radars and sonars.
The SO 4735 A, 4743 A and 4745 A are available in the commercial range, military range,

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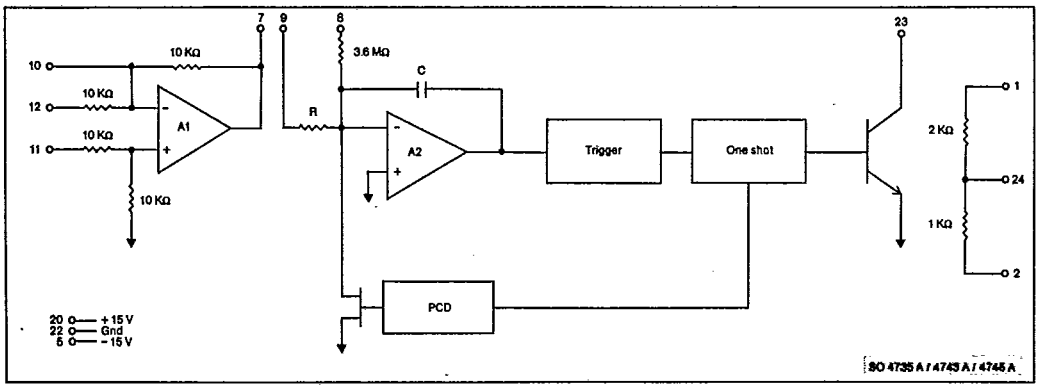
ABSOLUTE MAXIMUM RATINGS T_A = 25°C

PARAMETER	MIN	MAX	UNIT
Positive supply voltage V_{DD}		+18	V
Negative supply voltage V_{EE}	−18		V
Analog input voltage	−15	+15	V
Differential input voltage	−30	+30	V

PARAMETER	MIN	MAX	UNIT
Analog input current	−1.5	1.5	mA
Open collector output V_{CEO} (Ic = 10 mA) Ic max	0	 15 100	 V mA
Storage temperature range	−65	+150	°C

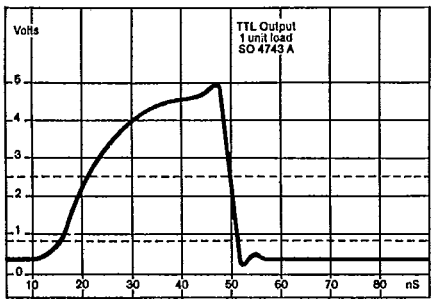
- For supply voltages less than ± 15 V, the input voltage must not exceed the supply voltage.
- Indefinite short to ground of pin 23 does not cause any damage or degradation to performance. However, both units will fail if shorted to the V_{DD} or V_{EE} supply voltages.
- Soldering temperature : 10 sec @ 300 °C max.

FUNCTIONAL DIAGRAM

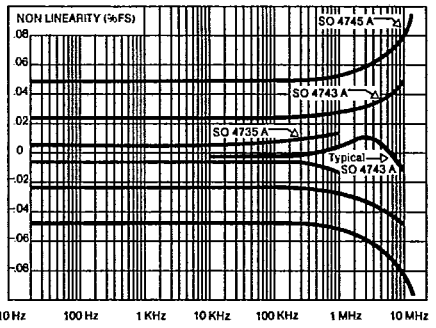


TYPICAL CURVES

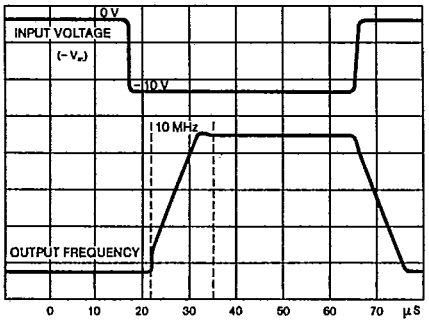
Output pulse



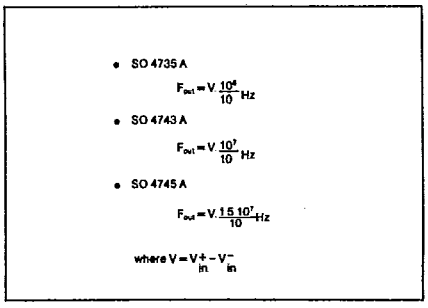
Linearity error



Settling time



Transfer function



ELECTRICAL CHARACTERISTICS

T = 25°C, V_{DD} = + 15.0 V, V_{EE} = −15.0 V, after 2 minutes warm-up, unless otherwise specified.

	SO 4735 A			SO 4743 A			SO 4745 A				
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	LEVEL
Full-scale	1			10			15			MHz	II
Input range : $+V_{in}$	$+10^{-4}$		+10	*		*	*		*	V	II
$-V_{in}$	−10		-10^{-4}	*		*	*		*	V	II
$+V_{in} - (-V_{in})$	$\pm 10^{-4}$		±10	*		*	*		*	V	II
$+I_{in}$	$+10^{-4}$		+1	*		*	*		*	mA	IV
Input impedance : $+V_{in}$	+9.9		+10.1	*		*	*		*	KΩ	IV
$-V_{in}$	+19.9		+20.1	*		*	*		*	KΩ	IV
$+I_{in}$	Virtual ground			Virtual ground			Virtual ground				IV
Overrange			10			*			*	%	III
Common mode rejection ratio	60			*			*			dB	IV
TTL output : High level	2.4			*			*			V	II
Low level			0.8			*			*	V	II
Fan-out			10			*			*	TTL u.l	IV
Pulse width	20		40	*		*	15		30	nS	II
Output impedance		600			*			*		Ω	IV
Maximum non-linearity (1)	±0.006%			±0.024%			±0.048%				II
$+V_{in}$, $-V_{in}$, $+I_{in}$	±0.006% f_{out} / FS			±0.024% f_{out} / FS			±0.048% f_{out} / FS				
Offset error (2)	−1		+1	−10		+10	−15		+15	KHz	II
Full scale error	0		+5	0		+50	0		+50	KHz	II
Offset drift	−50		+50	−100		+100	−100		+100	µV/°C	I
Full scale drift	−75		+75	−100		+100	−100		+100	ppm.FS/°C	I
Power supply sensitivity											
Offset		± 15			*			*		µV/%ΔV_{cc}	V
Full-scale		± 100			*			*		µV/%ΔV_{cc}	V
Response time (3)			15			*			*	µS	IV
Power supply range	±14		±18	*		*	*		*	V	IV
Quiescent current : I_{DD}			+75			*			*	mA	II
I_{EE}	−25			*			*			mA	II
Specified temperature range											
CC suffix	0		70	0		70	0		70	°C	
CZ suffix	−55		+125	−55		+125	−55		+125	°C	
CB suffix	−55		+125	−55		+125	−55		+125	°C	

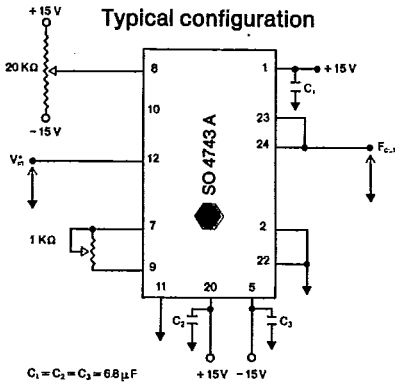
Notes : 1) Non linearity is defined as the deviation from the best straight line. Not specified under overrange conditions.
2) Offset-error is the deviation of the measured point for V_{in}^{+} = + 10 mV from the ideal point. Adjustable to zero.
3) For + 10 V input step, to ± 0.01 % output.
* Means "same specification as SO 4735".

TEST LEVEL

I 100% production tested and QA tested per QA test plan QA 200.
II 100% production tested at T = 25°C and QA sample tested at 25°C and T_{min} and T_{max} per QA test plan QA 200.
III QA sample tested per QA test plan QA 200.
IV Parameter guaranteed by design and characterization.
V Typical value for information.

APPLICATION INFORMATION

Typical configuration



OFFSET AND FULL SCALE TRIM

Offset calibration should be performed prior to full-scale calibration. Offset is adjusted with a 20 kΩ, 10 turn, 100 ppm/°C potentiometer connected as in typical circuit configuration. Because it is difficult to measure $f_{out} = 0$, the best method is to input + 1 mV at pin 12, and adjust :

$f_{out} = 100$ Hz (SO 4735 A)
$f_{out} = 1$ KHz (SO 4743 A)
$f_{out} = 1.5$ KHz (SO 4745 A).

The full-scale trim is adjusted with a 1 kΩ, 10 turn, 100 ppm/°C potentiometer connected as in typical circuit configuration. As the procedure can only lower the full-scale output frequency, the units are laser-trimmed at the factory to have initial full-scale error that is always positive. Full-scale values as low as 0.25 x FS are achievable. If external full-scale adjustment is not used, pins 7 and 9 must be tied together.

OUTPUT CIRCUIT

The units output a pulse train (see "typical curves"). When configured with TTL output, the fan-out is 10 TTL loads. The output circuit is a single transistor connected as a saturated switch with an uncommitted 2 kΩ pull up resistor. Care should be taken to avoid shorting of pin 23 to V_{DD} or V_{EE}. Either condition would cause catastrophic failure of the output transistor.

LAYOUT AND GROUNDING

Due to the high linearity of the units, certain precautions must be observed during initial system design. Layout must be clean, with output pulses routed as far as possible away from the input signals. For maximum performance, by-pass capacitors should be used (see typical circuit configuration). Analog and digital grounds are internally separated (pin 22 : Analog Ground, pin 2 : Digital Ground). The use of a ground plane is recommended. Any amplifiers used in front of the voltage to frequency converter should be decoupled.

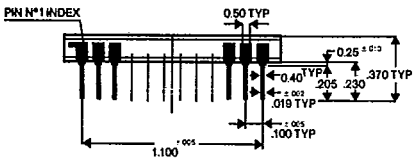
NON LINEARITY SPECIFICATION

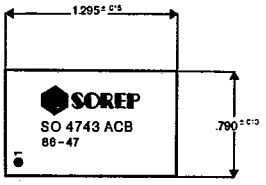
The non-linearity is the deviation of the measured point from the "best straight line". The deviation is expressed as a percent of the full-scale plus a percent of the signal (10 mV < V_{in} < 10 V). To recover the maximum linearity error (or non-linearity) for the desired point, calculate :

SO 4735 A
Max.N.L. = ±0.006% ±0.006% f_{out}/1
SO 4743 A
Max.N.L. = ±0.024% ±0.024% f_{out}/10
SO 4745 A
Max.N.L. = ±0.048% ±0.048% f_{out}/15

} where f_{out} in MHz, Max.N.L. in % FS

PACKAGE OUTLINE





All dimensions are in inches.

PIN ASSIGNMENT

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	+ 15 V supply (VDD)	9	Full scale adjust	17	N/C
2	Digital ground	10	+ Iin	18	N/C
3	N/C	11	$\overline{V_{in}}$	19	N/C
4	N/C	12	V_{in}	20	+ 15 V supply
5	− 15 V supply (VEE)	13	N/C	21	N/C
6	N/C	14	N/C	22	Analog Ground
7	Full-scale adjust	15	N/C	23	Output
8	Offset adjust	16	N/C	24	TTL

ORDERING INFORMATION

MODEL	SPECIFIED
SO 4735 A CC	0°C; 70°C
SO 4735 A CZ	−55; 125°C
SO 4735 A CB	*

MODEL	SPECIFIED
SO 4743 A CC	0°C; 70°C
SO 4743 A CZ	−55; 125°C
SO 4743 A CB	*

MODEL	SPECIFIED
SO 4745 A CC	0°C; 70°C
SO 4745 A CZ	−55; 125°C
SO 4745 A CB	*

* Please refer to pages 1 / 1-1 / 2-1 / 3-1