1GB – 2x64Mx72 DDR SDRAM, UNBUFFERED, PLL, FBGA

FEATURES

- Unbuffered 200-pin (SO-DIMM), small-outline, dual-in-line module
- Fast data transfer rate: PC-2100, and PC-2700
- Clock speeds of 133MHz, and 166MHz
- Supports ECC error detection and correction
- $V_{CC} = V_{CCQ} = +2.5V \pm 0.2V$(133 and 166MHz)
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency: DDR 266 (2, 2.5 clock), DDR333 (2.5 clock)
- Programmable Burst Length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh, 7.8µs refresh interval (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Dual Rank
- Leaded & lead-free/RoHS compliant
- Gold edge contacts
- JEDEC standard 200 pin, small-outline, SO-DIMM package
  - PCB height option: 31.75 mm (1.25")

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The WV3EG265M72EFSU is a 2x64Mx72 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM components. The module consists of eighteen 64Mx8 DDR SDRAMs in FBGA packages mounted on a 200 pin FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

OPERATING FREQUENCIES

	DDR333@CL=2.5	DDR266@CL=2	DDR266@CL=2.5
Clock Speed	166MHz	133MHz	133MHz
CL-t_{RCD}-t_{RP}	2.5-3-3	2-2-2	2.5-3-3

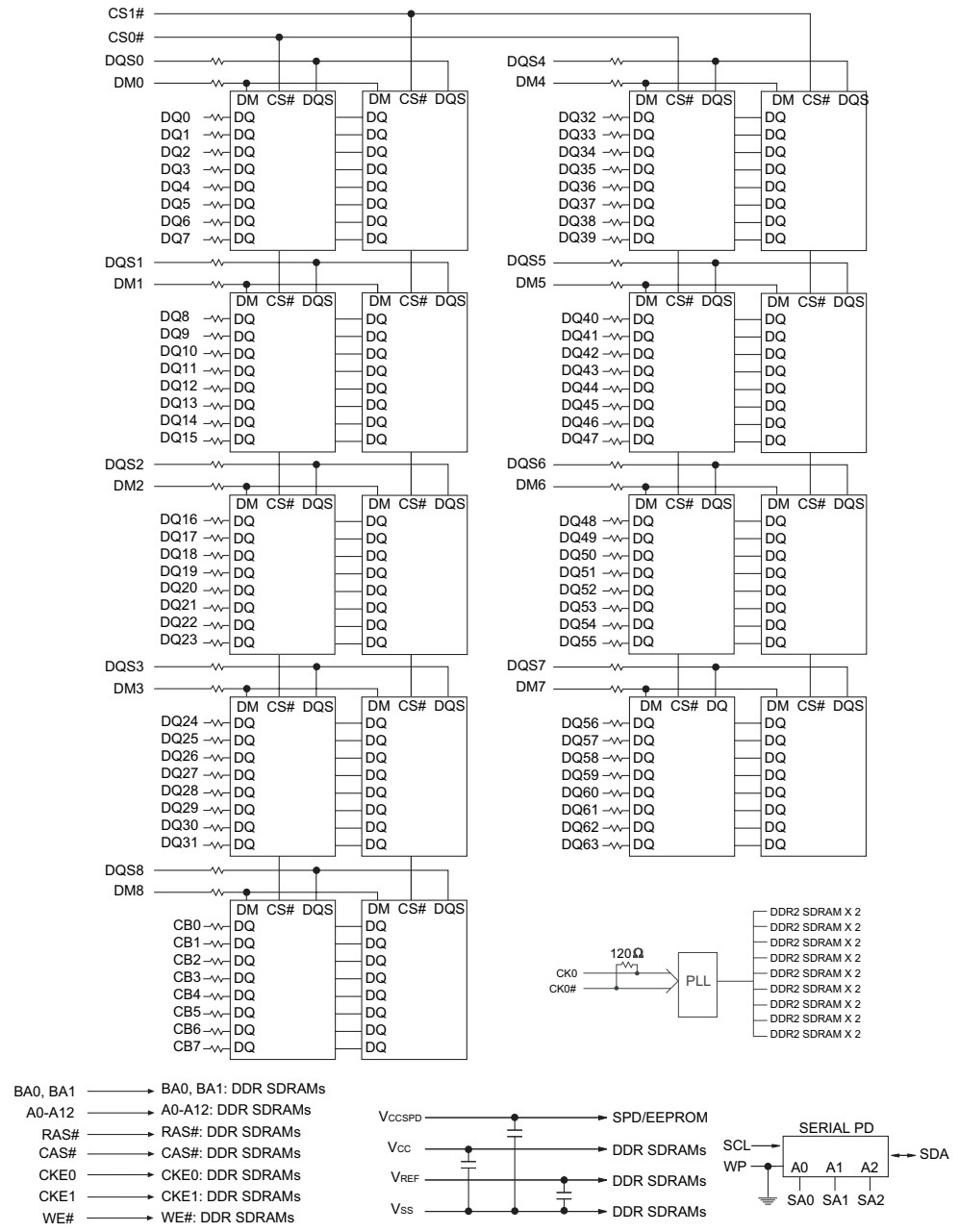
PIN CONFIGURATION

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V_{REF}	51	V_{SS}	101	A9	151	DQ42
2	V_{REF}	52	V_{SS}	102	A8	152	DQ46
3	V_{SS}	53	DQ19	103	V_{SS}	153	DQ43
4	V_{SS}	54	DQ23	104	V_{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V_{CC}
6	DQ4	56	DQ28	106	A6	156	V_{CC}
7	DQ1	57	V_{CC}	107	A5	157	V_{CC}
8	DQ5	58	V_{CC}	108	A4	158	NC
9	V_{CC}	59	DQ25	109	A3	159	V_{SS}
10	V_{CC}	60	DQ29	110	A2	160	NC
11	DQS0	61	DQS3	111	A1	161	V_{SS}
12	DM0	62	DM3	112	A0	162	V_{SS}
13	DQ2	63	V_{SS}	113	V_{CC}	163	DQ48
14	DQ6	64	V_{SS}	114	V_{CC}	164	DQ52
15	V_{SS}	65	DQ26	115	A10	165	DQ49
16	V_{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V_{CC}
18	DQ7	68	DQ31	118	RAS#	168	V_{CC}
19	DQ8	69	V_{CC}	119	WE#	169	DQS6
20	DQ12	70	V_{CC}	120	CAS#	170	DM6
21	V_{CC}	71	CB0	121	CS0#	171	DQ50
22	V_{CC}	72	CB4	122	CS1#	172	DQ54
23	DQ9	73	CB1	123	NC	173	V_{SS}
24	DQ13	74	CB5	124	NC	174	V_{SS}
25	DQS1	75	V_{SS}	125	V_{SS}	175	DQ51
26	DM1	76	V_{SS}	126	V_{SS}	176	DQ55
27	V_{SS}	77	DQS8	127	DQ32	177	DQ56
28	V_{SS}	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	CB2	129	DQ33	179	V_{CC}
30	DQ14	80	CB6	130	DQ37	180	V_{CC}
31	DQ11	81	V_{CC}	131	V_{CC}	181	DQ57
32	DQ15	82	V_{CC}	132	V_{CC}	182	DQ61
33	V_{CC}	83	CB3	133	DQS4	183	DQS7
34	V_{CC}	84	CB7	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V_{SS}
36	V_{CC}	86	NC	136	DQ38	186	V_{SS}
37	CK0#	87	V_{SS}	137	V_{SS}	187	DQ58
38	V_{SS}	88	V_{SS}	138	V_{SS}	188	DQ62
39	V_{SS}	89	NC	139	DQ35	189	DQ59
40	V_{SS}	90	V_{SS}	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	V_{CC}
42	DQ20	92	V_{CC}	142	DQ44	192	V_{CC}
43	DQ17	93	V_{CC}	143	V_{CC}	193	SDA
44	DQ21	94	V_{CC}	144	V_{CC}	194	SA0
45	V_{CC}	95	CKE1	145	DQ41	195	SCL
46	V_{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V_{CCSPD}
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	V_{SS}	199	NC
50	DQ22	100	A11	150	V_{SS}	200	NC

PIN NAMES

Symbol	Description
A0-A12	Address input
BA0, BA1	Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data Strobe
CK0, CK0#	Clock Input
CKE0-CKE1	Clock Enable Input
CS0#-CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Input
WE#	Write Enable
DM0-DM8	Data Write Mask
V_{CC}	Power Supply
V_{SS}	Ground
V_{REF}	SSTL_2 reference voltage
V_{CCSPD}	Serial EEPROM Positive Power Supply
SDA	Input/Output: Serial Presence-Detect Data
SCL	Serial Clock
SA0-SA2	Presence Detect Address Input
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 Ω ±5% unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	Notes
Supply Voltage DRR266/DDR333 (nominal V_{CC} 2.5V)		V_{CC}	2.3	2.7	V	
I/O Supply Voltage DRR266/DDR333 (nominal V_{CC} 2.5V		V_{CCQ}	2.3	2.7	V	
I/O Reference Voltage		V_{REF}	0.49 × V_{CC}	0.51 × V_{CC}	V	1
I/O Termination Voltage		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	2
Input Logic High Voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{CC} + 0.30	V	
Input Logic Low Voltage		$V_{IL(DC)}$	-0.3	V_{REF} - 0.15	V	
Input voltage level, CK and CK#		$V_{IN(DC)}$	-0.3	V_{REF} + 0.30	V	
Input differential voltage, CK and CK#		$V_{ID(DC)}$	0.3	V_{REF} + 0.60	V	3
Input crossing point voltage, CK and CK#		$V_{IX(DC)}$	0.3	V_{REF} - 0.60	V	
Input leakage current	Addr CAS#, RAS#, WE#	I_I	-36	36	µA	
	CS#, CKE		-18	18	µA	
	CK, CK#		-10	10	µA	
	DM		-4	4	µA	
Output leakage current		I_{OZ}	-10	10	µA	
Output high current (normal strength) V_{OUT} = v +0.84V		I_{OH}	-16.8		mA	
Output high current (normal strength) V_{OUT} = V_{TT} - 0.84V		I_{OL}	16.8		mA	
Output high current (half strength) V_{OUT} = V_{TT} - 0.45V		I_{OH}	-9		mA	
Output high current (half strength) V_{OUT} = V_{TT} - 0.45V		I_{OL}	9		mA	

Notes:

1 V_{REF} is expected to equal to 0.5*V_{CCQ} of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-2 percent of the DC value.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level of CK#.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{IN}, V_{OUT}	Voltage on V_{CC} pin relative to V_{SS}	-0.5 ~ 3.6	V
V_{CC}, V_{CCQ}	Voltage on V_{CC} & V_{CCQ} supply relative to V_{SS}	-1.0 ~ 3.6	V
V_{REF}	Voltage of V_{REF} supply relative to V_{SS}	-1.0 ~ 3.6	V
T_{STG}	Storage Temperature	-55 ~ +150	°C
T_A	Operating temperature	0 ~ 70	°C
P_D	Power dissipation	18	W
I_{OS}	Short circuit output current	50	mA

Notes:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceed.

Functional ioeration should be restricted to recommended operation conditions.

Exposing to higher than recommended voltage for extended periods of time could affect device reliability.

AC OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.31	-	V
AC Input High (Logic 0) Voltage	V_{IL}(AC)	-	V_{REF} - 0.31	V
Input Differential Voltafe, CK and CK# inputs	V_{ID}(AC)	0.7	V_{CC} + 0.6	V
Input Crossing Point Voltage, CK and CK# input	VIX(AC)	0.5*V_{CC} - 0.2	0.5*V_{CC} + 0.2	V

INPUT/OUTPUT CAPACITANCE

TA=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#)	$C_{IN}1$	31	49	pF
Input capacitance (CKE0, CKE1)	$C_{IN}2$	17.5	26.5	pF
Input capacitance (CS0# - CS1#)	$C_{IN}3$	17.5	26.5	pF
Input capacitance (CLK0, CLK0#)	$C_{IN}4$	6	7.5	pF
Input capacitance (DM0~DM8)	$C_{IN}5$	11	13	pF
Input capacitance (DQ0~DQ63), (CB0~CB7)	$C_{OUT}1$	11	13	pF

I_{CC} SPECIFICATIONS AND CONDITIONS

V_{CC}, V_{CCQ} = +2.5V ±0.2V

SYM	PARAMETER/CONDITION	MAX			UNITS
		DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5	
I_{CC0}*	OPERATING CURRENT: One device bank; Active-Precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	1,270	1,180	1,180	mA
I_{CC1}*	OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle	1,540	1,450	1,450	mA
I_{CC2P}**	PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (MIN); CKE = (LOW)	370	370	370	mA
I_{CC2F}**	IDLE STANDBY CURRENT: CS# = HIGH; All device banks are idle; t_{CK} = t_{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM	820	820	820	mA
I_{CC3P}**	ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; t_{CK} = t_{CK} (MIN); CKE = LOW	820	820	820	mA
I_{CC3N}**	ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank active; t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	1,090	1,090	1,090	mA
I_{CC4R}*	OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	1,585	1,450	1,450	mA
I_{CC4W}*	OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	1,675	1,495	1,495	mA
I_{CC5}**	AUTO REFRESH BURST CURRENT: t_{REFC} = t_{RFC} (MIN)	3,970	3,790	3,790	mA
I_{CC6}**	SELF REFRESH CURRENT: CKE ≤ 0.2V	370	370	370	mA
I_{CC7}*	OPERATING CURRENT: Four device bank interleaving READs (Burst = 4) with auto precharge, t_{RC} = minimum t_{RC} allowed; t_{CK} = t_{CK} (MIN); Address and control inputs change only during Active READ, or WRITE commands	3,565	3,250	3,250	mA

Note: I_{CC} specification is based on **SAMSUNG** components. Other DRAM Manufacturers specification may be different.

*: Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

**: Value calculated reflects all module ranks in this operating condition.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

V_{CC} = V_{CCQ} = +2.5V ±0.2V

AC CHARACTERISTICS			335		262		265		UNITS
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	
Row cycle time		tRC	60		65		65		t_{CK}
Refresh row cycle time		tRFC	72		75		75		ps
Row active		tRAS	42	70K	45	120K	45	120K	ps
RAS# to CAS# delay		tRCD	18		20		20		t_{CK}
Row precharge time		tRP	18		20		20		ns
Row active to row active delay		tRRD	12		15		15		ns
Write recovery time		tWR	15		15		15		ns
Last data in to READ command		tWTR	1		1		1		ns
Clock cycle time	CL = 2.5	$t_{CK\ (2.5)}$	6	12	7.5	12	7.5	12	ns
	CL =2	$t_{CK\ (2)}$	7.5	12	7.5	12	10	12	ns
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DQS-out access time from CK/CK#		t_{DQSCK}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns
Output data access time from CK/CK#		tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns
Data stobe edge to output data edge		t_{DQSQ}		0.45		0.5		0.5	ns
Read preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
Read postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
CK to vaild DQS-in		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}
DQS-in setup time		tWPRES	0		0		0		ns
DQS-in hold time		tWPRE	0.25		0.25		0.25		t_{CK}
DQS falling edge to CK rising-setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}
DQS falling edge to CK rising-hold time		tDHS	0.2		0.2		0.2		t_{CK}
DQS-in high level width		tDQHS	0.35		0.35		0.35		t_{CK}
DQS-in low level width		TDQSL	0.35		0.35		0.35		t_{CK}
Address and control input setup time (fast)		tISF	0.75		0.9		0.9		ns
Address and control input hold time (fast)		tIHF	0.75		0.9		0.9		ns
Address and control input setup time (slow)		tISS	0.8		1.0		1.0		ns
Address and control input hold time (slow)		tIHS	0.8		1.0		1.0		ns
Data-out high impedance time from CK/CK#		tHZ	-0.70	+0.70	-0.75	+0.75	-0.75	+0.75	ns
Data-out low impedance time to CK/CK#		tLZ	-0.70	+0.70	-0.75	+0.75	-0.75	+0.75	ns
Mode register set cycle		tMRD	12		15		15		ns
DQ & DM setup time to DQS		tDS	0.45		0.5		0.5		ns
DQ & DM hold time to DQS		tDH	0.45		0.5		0.5		ns
Control & address input pulse width		tIPW	2.2		2.2		2.2		ns
DQ & DM input pulse width		tDIPW	1.75		1.75		1.75		ns
Exit self refresh to non-read command		tXSNR	75		75		75		ns

* AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Continued on next page

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

V_{CC} = V_{CCQ} = +2.5V ±0.2V

AC CHARACTERISTICS		335		262		265		UNITS
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	
Exit self regresh to read command	t_{XSRD}	200		200		200		t_{CK}
Refresh interval time	t_{REFI}		7.8		7.8		7.8	µs
Output DQS vaild window	t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns
Clock half period	t_{HP}	t_{CLmin} or t_{CHmin}		t_{CLmin} or t_{CHmin}		t_{CLmin} or t_{CHmin}		ns
Data hold skew factor	t_{QHS}		0.55		0.75		0.75	ns
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	ns
Active Read with auto precharge command	t_{RAP}	18		20		20		ns
Auto precharge Write recovery + Precharge time	t_{RAL}	t_{WR}/t_{CK} + t_{RP}/t_{CK}		t_{WR}/t_{CK} + t_{RP}/t_{CK}		t_{WR}/t_{CK} + t_{RP}/t_{CK}		t_{CK}

* AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

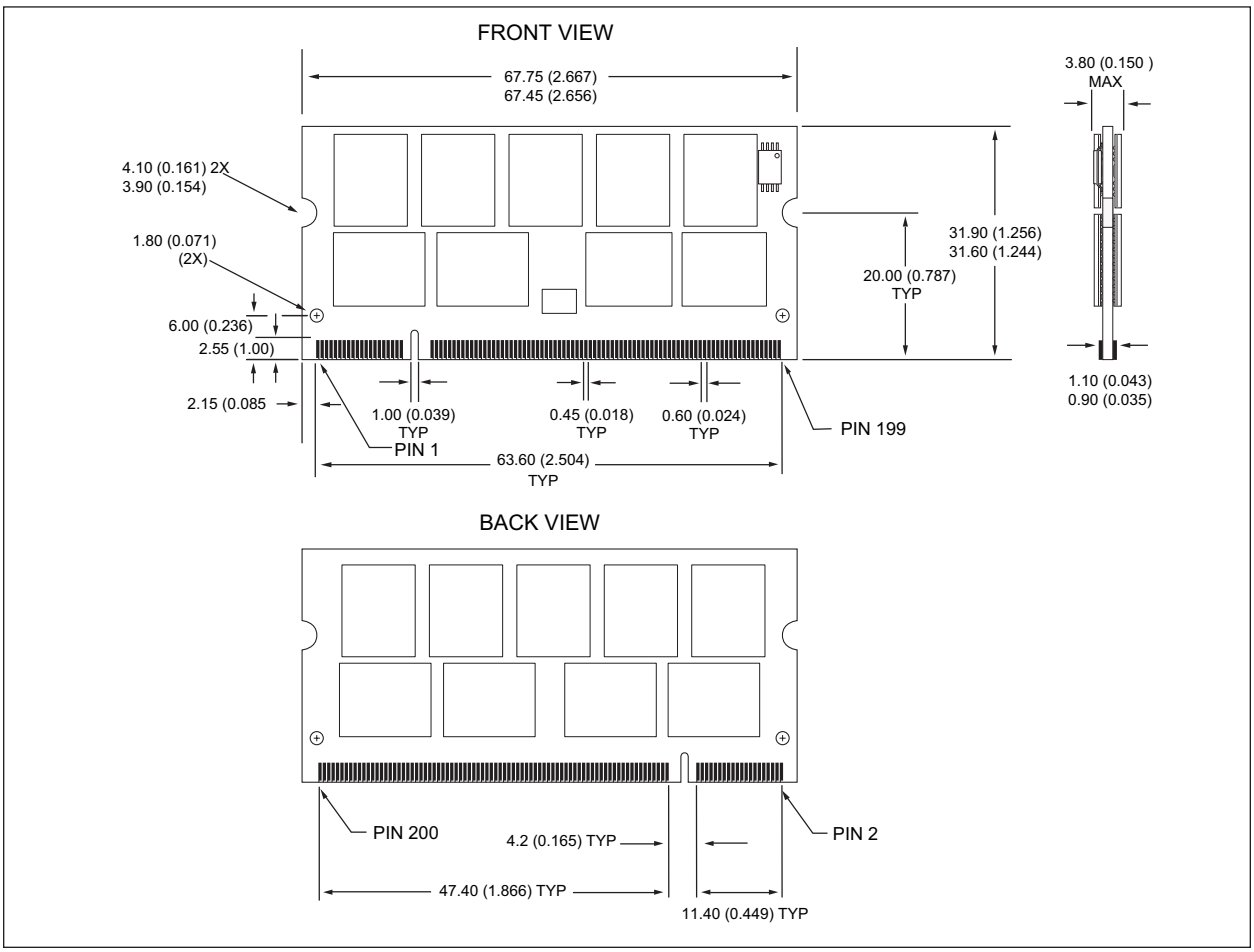
ORDERING INFORMATION FOR D4

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
WV3EG265M72EFSU335D4xxx	166MHz/333Mbps	2.5	3	3	31.75 (1.25") MAX
WV3EG265M72EFSU262D4xxx	133MHz/266Mbps	2	2	2	31.75 (1.25") MAX
WV3EG265M72EFSU265D4xxx	133MHz/266Mbps	2.5	3	3	31.75 (1.25") MAX

NOTES:

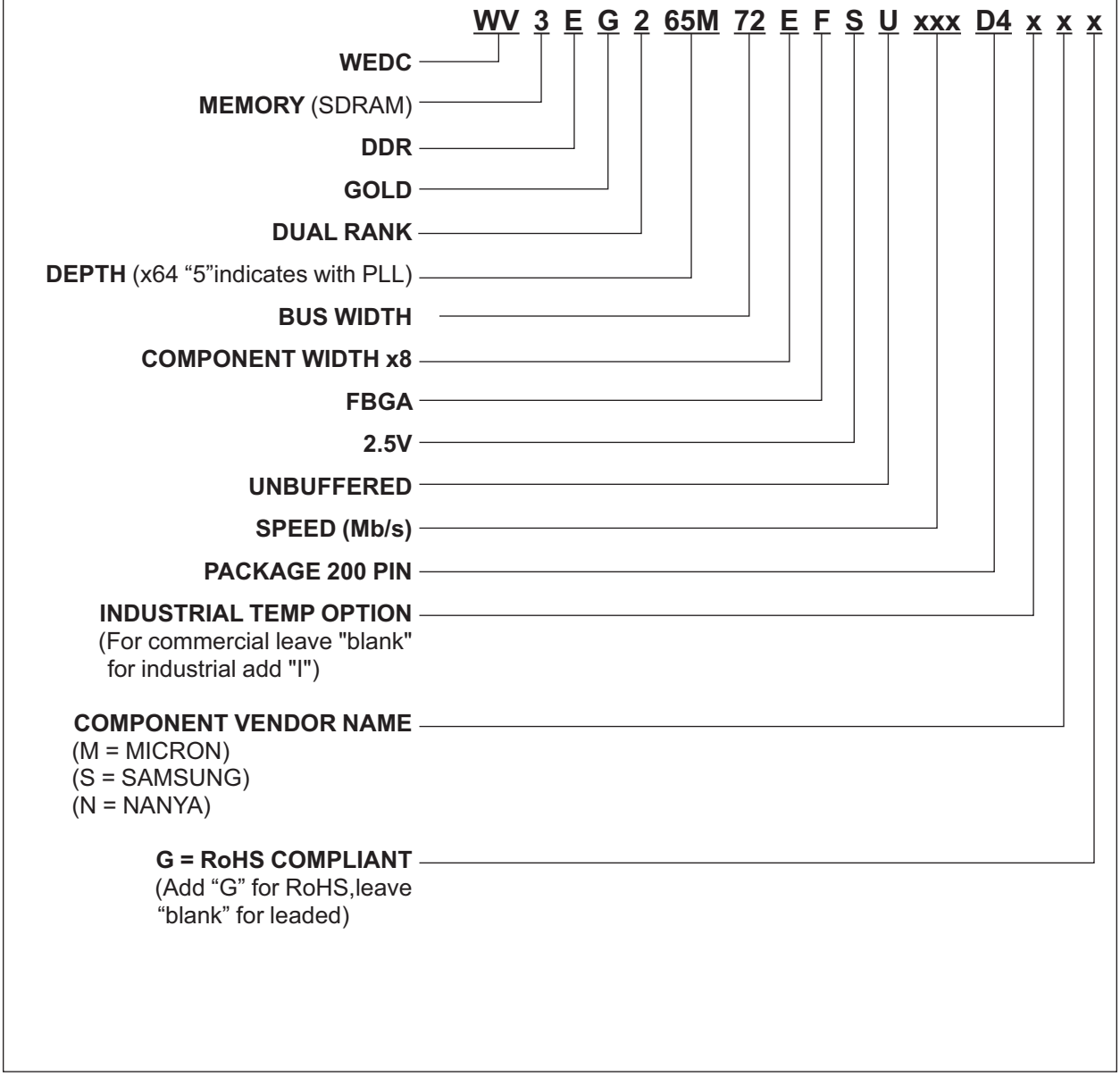
- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

200-PIN DDR SO-DIMM DIMENSIONS



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

1GB – 2x64Mx72 DDR SDRAM, UNBUFFERED, with PLL, FBGA

DRAM DIE OPTIONS:

- SAMSUNG: C-Die
- MICRON: T27Z: D-Die, will move to T37Z:F Q2'06
- NANYA: B-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	May 2006	Advanced