HD66137T

Dec. 01 , 1998 Rev. 1.1

High - Voltage 240 - Channel Common Driver for Dot - Matrix STN LCD

HITACHI

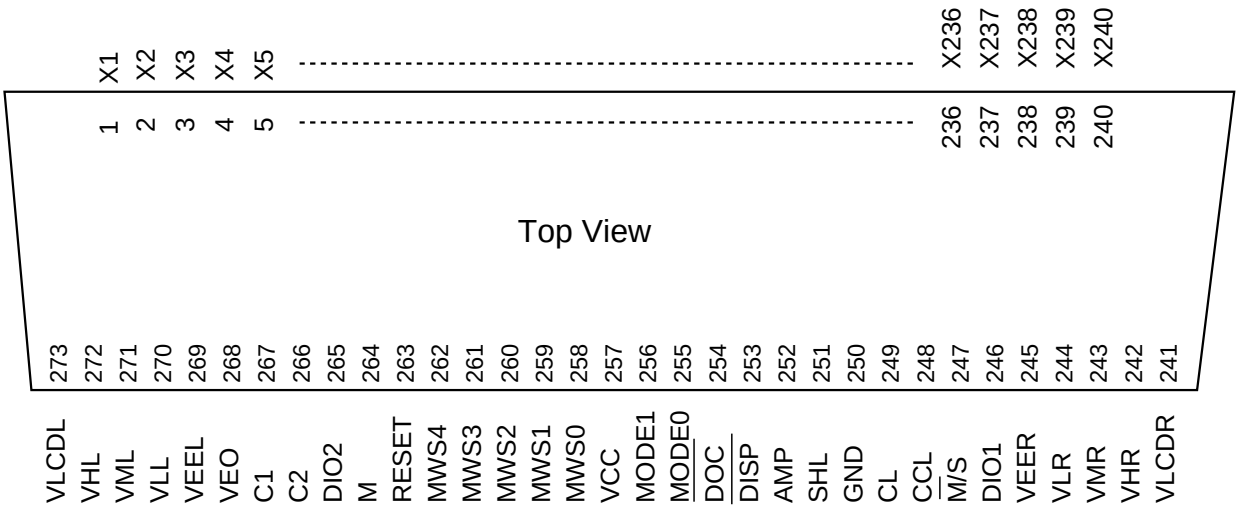
Description

The HD66137T is a 240-channel common driver which drives a dot matrix STN liquid - crystal panel. By changing the mode, this can be applied to 240- and 200- and 160- channel output. Through the use of a 43V high-voltage CMOS process technology, a high-voltage drive of +21.5 V and -21.5 V, centering on VM is possible. -21.5V is generated from max +21.5V with built-in switching circuit and external capacity. 3 V is used for logic drive. This device is used together with the segment driver HD66130 , HD66134S or HD66136.

Features

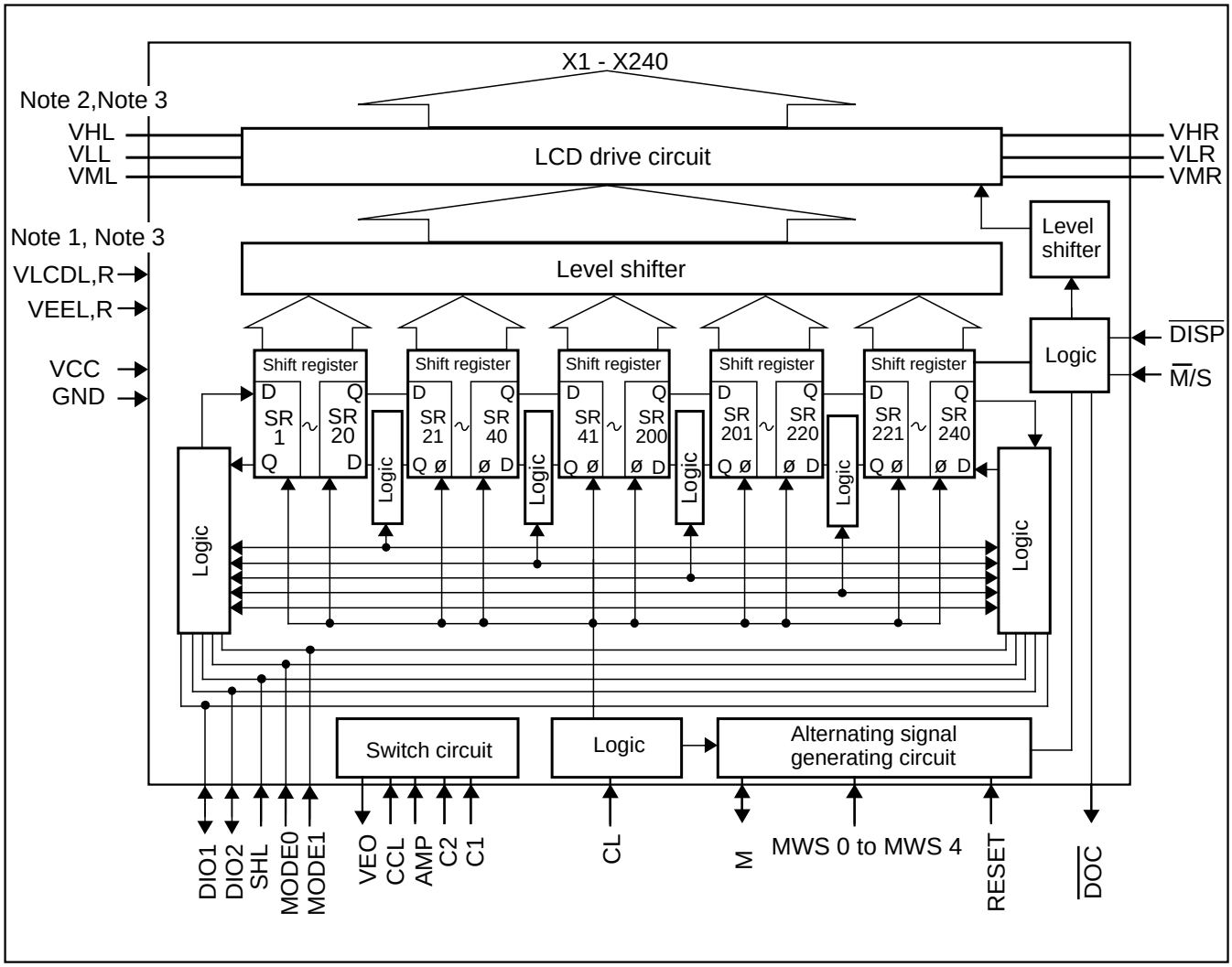
- Display duty: Up to 1 / 240
- LCD drive voltage: 43 V max
- Built-in switching circuit (to generate -21.5V)
- Number of LCD drive circuit: 240
- Operating voltage: 2.5 to 5.5 V
- Intermediate voltage I/F
- Built-in alternating signal generation circuit Pin programmable
- Output mode change: 240-output mode
  200-output mode
  160-output mode
- Built-in display-off function
- Flex TCP

Pin Arrangement



Note: The shape above does not indicate the actual outline.

*** This products still under development. So, the specification may be changed without preannouncement**



* 1 VLCDL and VLCDR, and VEEL and VEER are internally connected.
* 2 VHL and VHR, VLL and VLR, and VML and VMR are internally connected.

Internal Block Diagram

1. LCD drive circuit

This circuit selects and outputs the three level signals for the LCD drive. By a combination of the data in the shift register and M, either VH, VL, or VM is selected and transmitted to the output circuit.

2. Level shifter

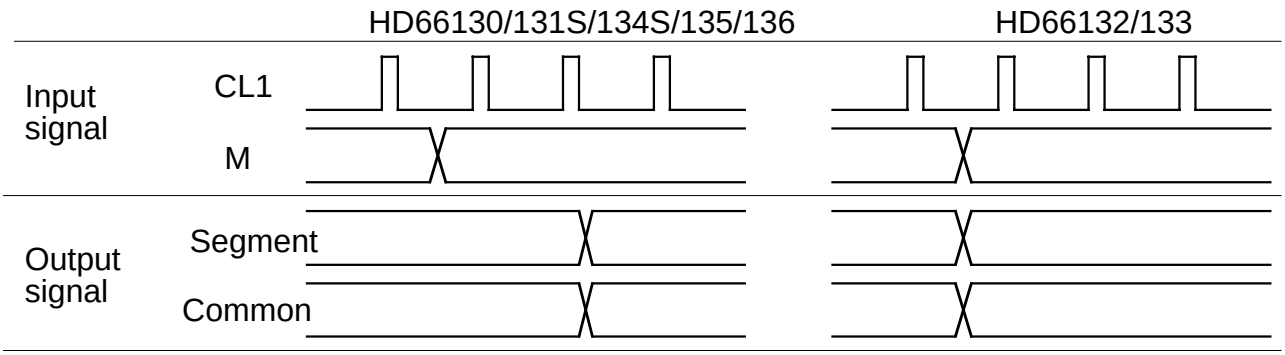
This boosts a 5V signal to a high-voltage signal for LCD drive.

3. Shift register

This is a 240-bit bidirectional shift register circuit. The first line marker signal output from the DIO1 pin and DIO2 pin is sequentially shifted by shift clock CL. The shift direction is determined by the SHL pin. 4. Alternating signal generating circuit

This circuit generates an alternating signal , M signal for LCD display. To suppress cross-talk, the signal is alternated in a unit from several lines to several tens of lines. By connecting MWS0 to MWS4 pins to Vcc or GND, the desired number of signals can be alternated. When alternating signals are externally input, all pins , MWS0 to MWS4 are connected to GND.

HIFAS driver family timing comparison



Pin Functions

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Classification	Symbol	Pin No.	Connected to	I/O	Functions
Power supply	VLCDL,R VEEL,R VCC GND	273,241 269,245 257 250	Power supply	—	VLCDL,R - VEEL,R : Power supply for LCD drive VLCDL,R : Power supply for switch circuit VCC - GND : Power supply for logic circuit
	VHL, R VLL, R VML, R	272,242 270,244 271,243	Power supply	Input	Power supply for LCD drive level VHL,R : Selected level ; Set to the same voltage as VLCDL, R. VLL,R : Selected level ; Set to the same voltage as VEEL, R. VML,R : Non-selected level and Power supply for switch circuit
	VEO	268	VEEL,R	output	When using built-in switching circuit and generate VEE, VEO pin should be connect to VEEL,R pins. VM voltage is point of reference. VLCD - VM voltage is reversed and output as VEE. If built-in switching circuit is not used, don't connect any lines to this pin.
	C1,C2	267,266	Capacitance	—	External capacitance should be connected when using the switch circuit for generate VEE . If built-in switching circuit is not used, don't connect any lines to this pin.
Control signal	CL	249	MPU	Input	Shift clock input data is shifted at the falling edge of shift clock, CL of the shift register.
	M	264	Extension driver or MPU	I/O	Inputs or outputs the alternating current for LCD drive output.
	MWS0 MWS1 MWS2 MWS3 MWS4	258 259 260 261 262	—	Input	This pin specifies the cycle of the alternating signal , M signal in the unit of the number of lines. The number of lines, which is an integer from 2 to 31, is specified as follows. Usually, specify the number of lines within a range from 10 to 31. When the HD66131T is driven by an external alternating signal, specify the number of lines as zero.

Number of lines	MWS4	MWS3	MWS2	MWS1	MWS0	Line alternating waveform	M-pin status
0	0	0	0	0	0	—	Input
1	0	0	0	0	1	Prohibited	Output
2	0	0	0	1	0	2 lines alternated	
3	0	0	0	1	1	3 lines alternated	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	
31	1	1	1	1	1	31 lines alternated	

1 ="Vcc", 0 ="GND"

	MODE0 MODE1	255 256	—	Input	Switch terminals for the number of LCD drive output pins

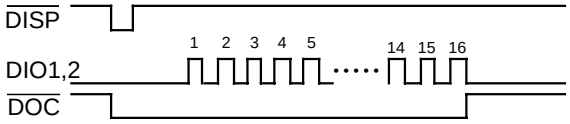
MODE0	MODE1	Shift direction
" H "	" H "	240 - output (X1,X2,X3.....X238,X239,X240)
" H "	" L "	200 - output (X21,X22,X23.....X218,X219,X220)
" L "	" H "	160 - output (X41,X42,X43.....X198,X199,X200)
" L "	" L "	Prohibited

	DIO1 DIO2	246 265	Extension driver or MPU	I/O	Serial data input / output pin; input / output pins for sift register

SHL	DIO1	DIO2
" H " level	serial output pin	serial input pin
" L " level	serial input pin	serial output pin

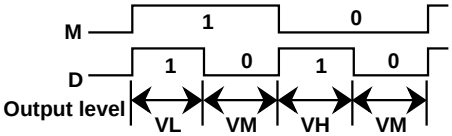
	CCL	248	MPU	Input	Built-in switching circuit clock input. When using built-in switching circuit and generating VEE, this pin connect CL pin. If built-in switching circuit is not used, CCL must be fixed to GND
	AMP	252	VCC or GND	Input	Built-in switching circuit on-off control When using built-in switching circuit, this pin must be fixed to VCC. If built-in switching circuit is not used, this pin must be fixed to GND

Pin Functions

Classifi-cation	Symbol	Pin No.	Connected to	I/O	Functions
Control signal	RESET	263	MPU or VCC	Input	Setting this pin to GND initializes the alternating signal (M signal) circuit. A VCC level RESET is normally used.
	$\overline{DISP}$	253	MPU	Input	Setting this pin to GND sets LCD drive output X1 to X240 to the VM level. Internal resister is not cleared.
	$\overline{M}$/S	247	—	Input	Controls the display-off function. and display-off signal output from $\overline{DOC}$ pin $\overline{M}$/S: "H"level — When $\overline{DISP}$ is low level, X1-240 set VM level $\overline{M}$/S: "L"level — Until 16 times serial data is input into DIO, X1-X240 set VM level
	$\overline{DOC}$	254	—	Output	$\overline{M}$/S: "H"level — When $\overline{DISP}$ is low level,output low level; When $\overline{DISP}$ is high level,output high level $\overline{M}$/S: "L"level — Until 16 times serial data is input, output low level  When using M/S is low level ,$\overline{DOC}$ pin should be connected to SEG LSI Dispoff control pin.
	SHL	251	—	Input	This pin switches shift resister directions.

SHL	MODE0	MODE1	Shift direction
			Right shift
" H " level	" H "	" H "	DIO2→SR1→••••••→SR240→DIO1
	" H "	" L "	DIO2→SR21→••••••→SR220→DIO1
	" L "	" H "	DIO2→SR21→••••••→SR220→DIO1
			Left shift
" L " level	" H "	" H "	DIO1→SR240→••••••→SR1→DIO2
	" H "	" L "	DIO1→SR220→••••••→SR21→DIO2
	" L "	" H "	DIO1→SR200→••••••→SR41→DIO2

SR1, SR2 ••• SR240 correspond to X1, X2 ••• X240.
Note: The 40 or 80 pins invalidated at the 200-output or 160-output mode output the non- selected level synchronized with M signal; These pins should be used open.

LCD drive output	X1 to X240	1 to 240	LCD	Output	LCD drive output By a combination of the display data and the M signal, when $\overline{DISP}$ is set to Vcc, either VH, VL, or VM is selected and transmitted to the output circuit. 

Note : Configuring the LCD panel using the HD66137 when using the select SEGMENT driver.

The select SEGMENT driver.

SEGMENT driver	Select
HD66130(320OUT)	○
HD66132(240OUT)	×
HD66134S(240OUT)	○

Segment driver	Select
HD66136(400OUT)	○

Application Example (1)

Figure 1 shows an application example of 640 x 3 (color) x 240 dot Half VGA Size STN color panel. This panel consist on HD66137 x 1 piece and HD66136 x 5 pieces.
HD66137 generate M signal and DOC signal . M signal pin is connected M signal pin of HD66136 and DOC signal pin is connected DISP signal pin of HD66136.
HD66137 is able to generates minus voltage by external capacitor, CO.
VEO pin is connected VEE pin and VL pin.

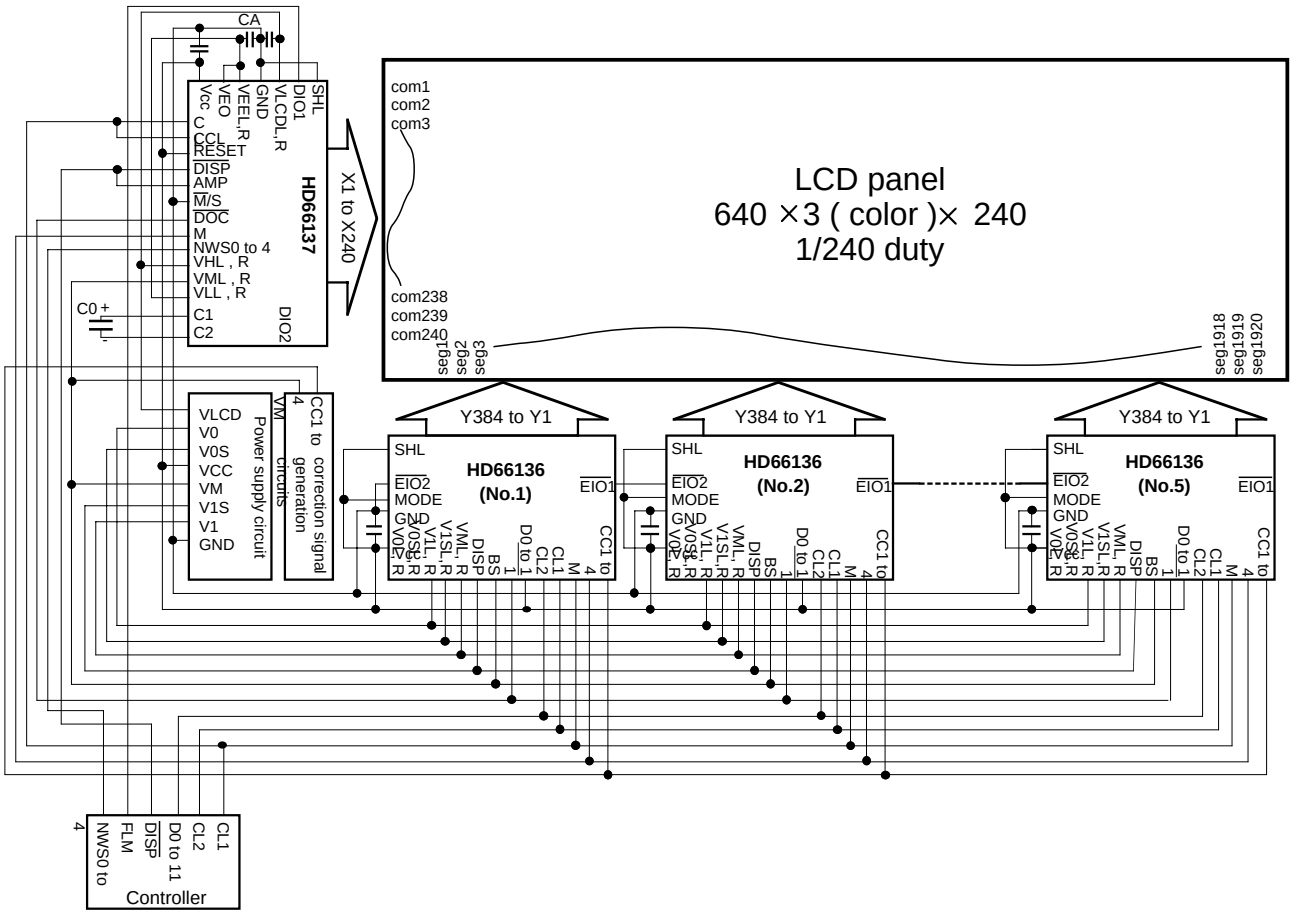


Figure1 Application Example (1)

Notes:
1. When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1 µF for each IC , between Vcc and GND, V0 and GND, VLCD and GND, and VEE and GND.
2. In addition, for the power supply circuit, connect a capacitor of several µF or several tens of µF between the liquid-crystal power supply and GND. For evaluation, confirm that there is no inversion between liquid-crystal drive power supply and level power supply in the period between when the liquid-crystal drive power supply is turned on and when it is turned off.
3. when using external capacitor, CO to generate VEE, connect a capacitor of several µF or several tens of µF between the VEE and GND.

Application Example (2)

Figure 2 shows an application example of 320 3 x (color) x 240 dot Quarter VGA size STN color panel. This panel consist of HD66137 x 1 piece and HD66130 x 3 pieces.
HD66137 generate M signal and DOC signal . M signal pin is connected M signal pin of HD66130 and DOC signal pin is connected DISP signal pin of HD66136.
HD66137 is able to generates minus voltage by external capacitor, CO.
VEO pin is connected VEE pin and VL pin.

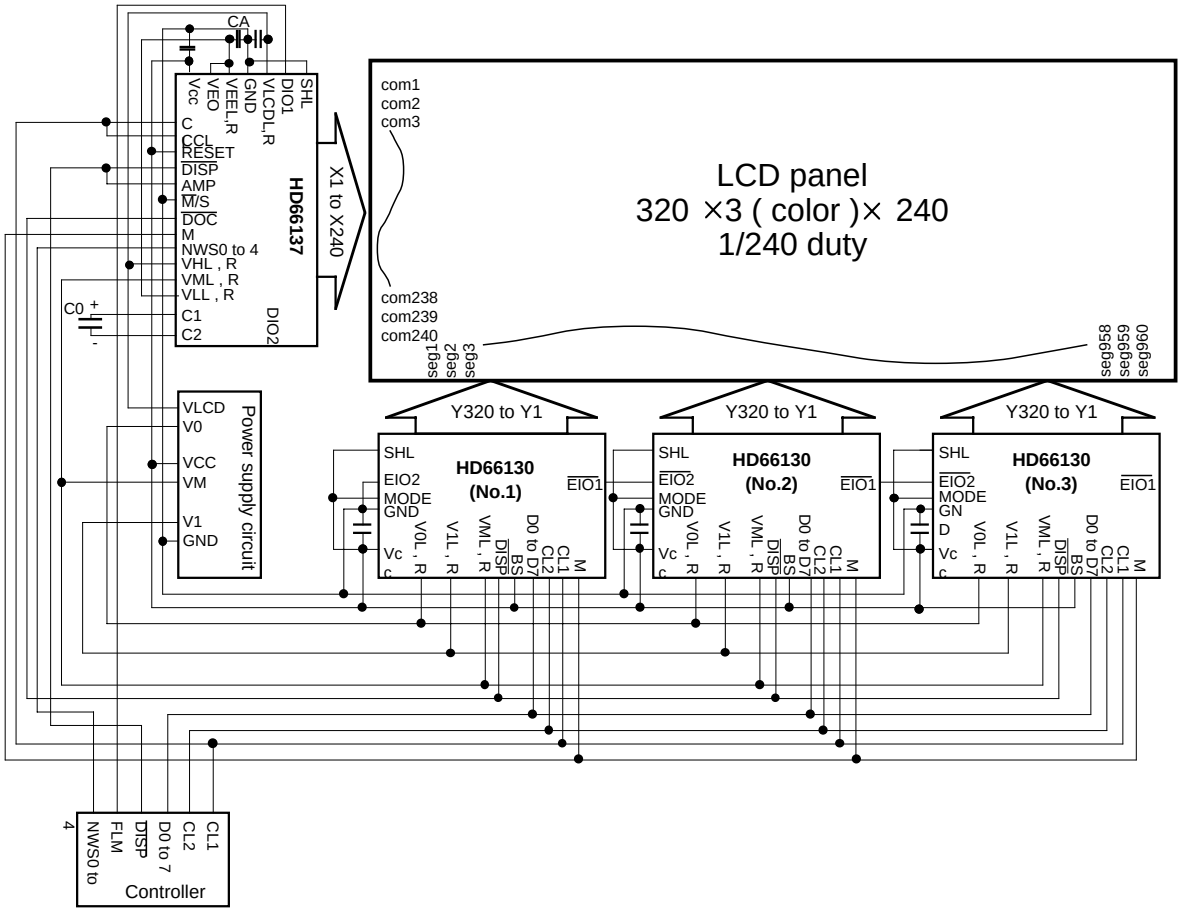


Figure2 Application Example (2)

Notes:
1. When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1 µF for each IC , between Vcc and GND, V0 and GND, VLCD and GND, and VEE and GND.
2. In addition, for the power supply circuit, connect a capacitor of several µF or several tens of µF between the liquid-crystal power supply and GND. For evaluation, confirm that there is no inversion between liquid-crystal drive power supply and level power supply in the period between when the liquid-crystal drive power supply is turned on and when it is turned off.
3. when using external capacitor, CO to generate VEE, connect a capacitor of several µF or several tens of µF between the VEE and GND.

Power Supply Circuit Example

Figure 3 Shows power supply circuits example

By using 3 level power supply output DC - DC converter,LCD power supply circuit is established without minus voltage power supply.

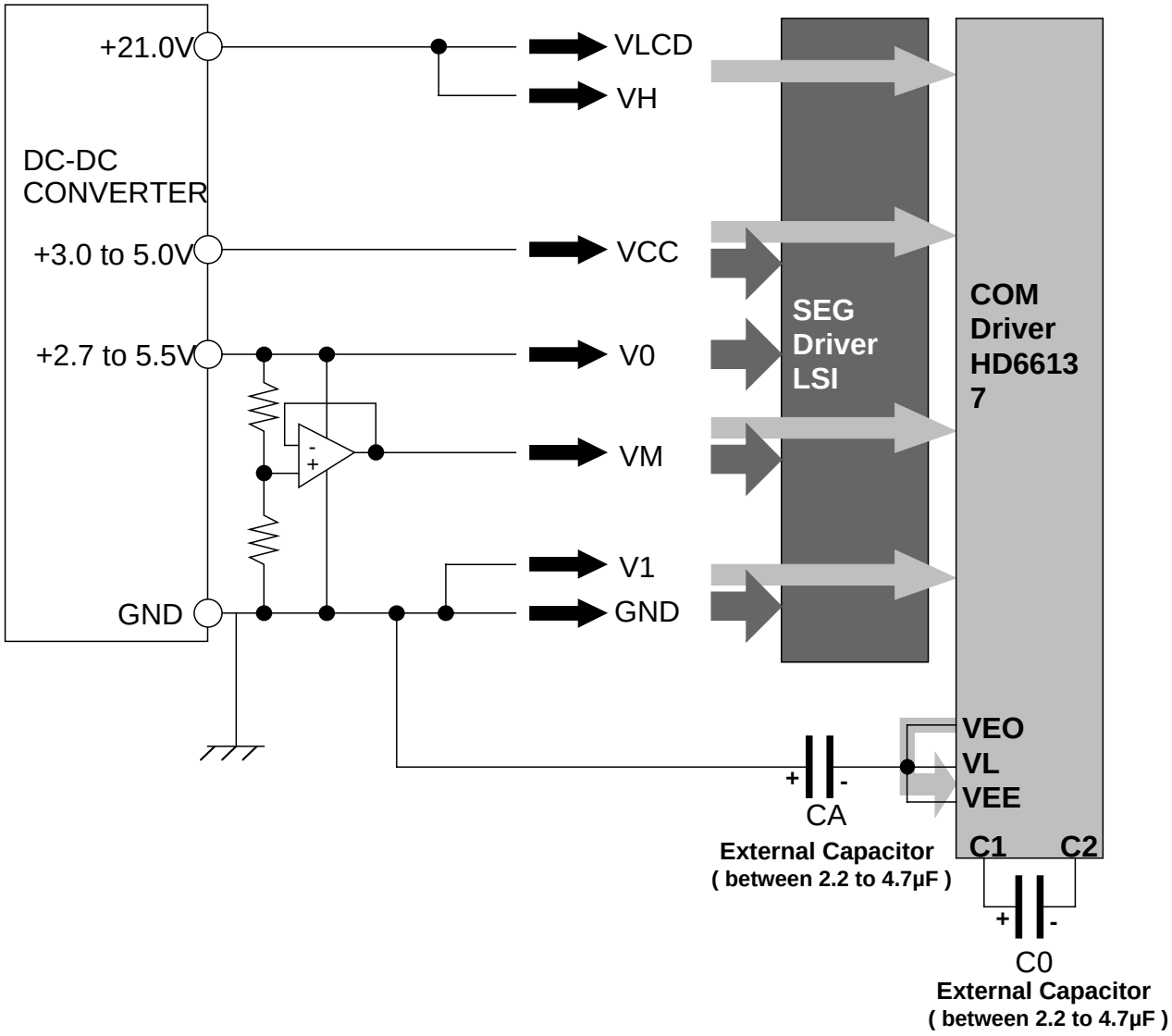


Figure 3 Power Supply Circuit Example

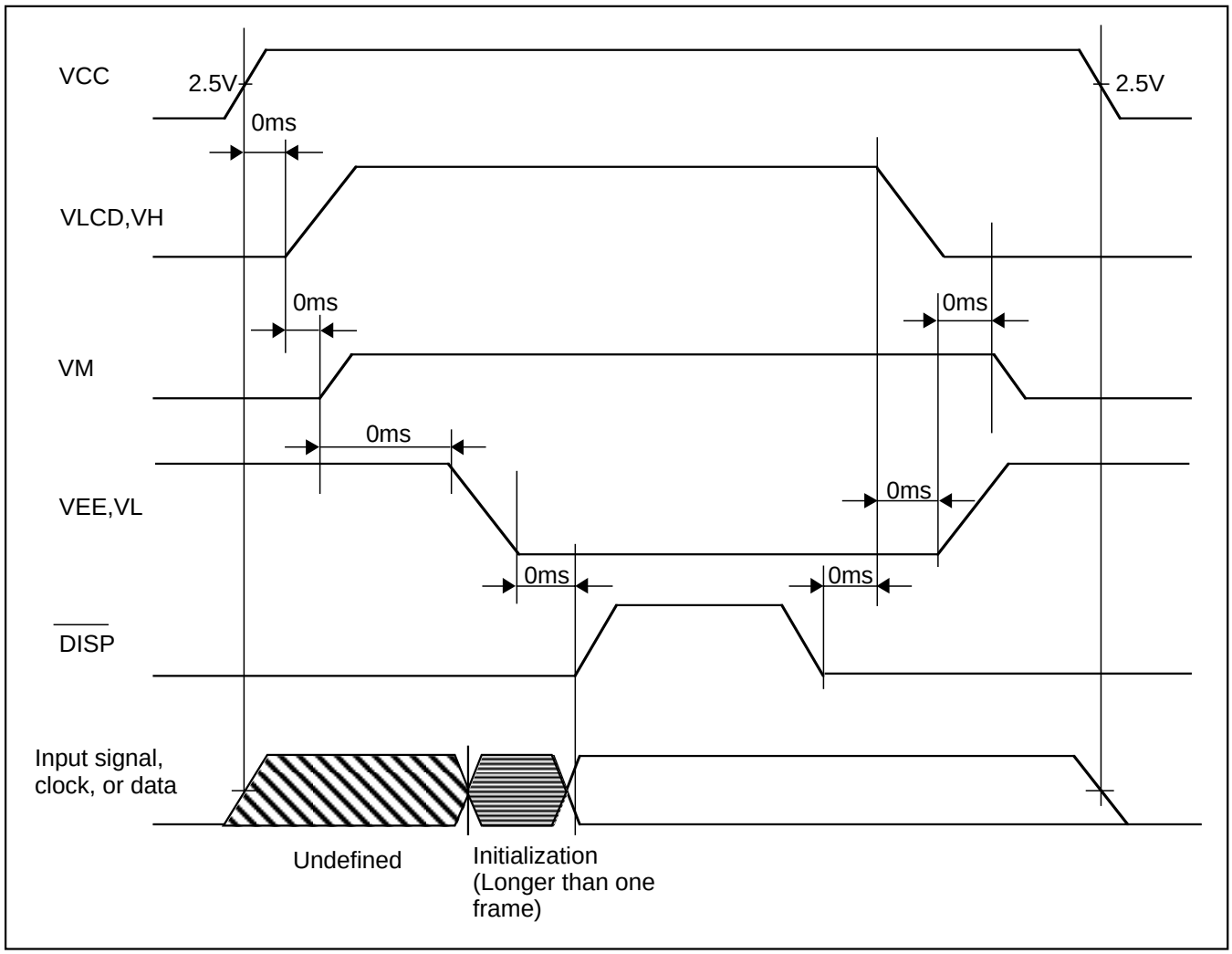
Absolute Maximum Ratings

Items		Symbol	Ratings	Unit	Note
Power supply voltage	Logic circuit	VCC	- 0.3 to + 7.0	V	* 1 , * 8
	LCD drive circuit	VLCD	- 0.3 to + 25.0	V	*1 , * 3 , * 8
		VEE	- 20.0 to + 0.3	V	* 1 , * 4 , * 8
Input voltage (1)		VT1	- 0.3 to VCC + 0.3	V	* 1 , * 2
Input voltage (2)		VH	- 0.3 to VLCD	V	* 1 , * 5 , * 8
Input voltage (3)		VL	+ 0.3 to VEE	V	* 1 , * 6 , * 8
Input voltage (4)		VM	- 0.3 to + 5.0	V	* 1 , * 7 , * 8
Operating temperature		Topr	- 30 to + 75	°C	
Storage temperature		Tstg	- 55 to + 110	°C	

Notes: If the LSI is used beyond the above maximum ratings, it may be permanently damaged.
It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

*1 The reference point is GND (0V).
*2 Applies to DIO1 , $\overline{DISP}$, SHL , M , NWS0 , NWS1 , NWS2 , NWS3 , NWS4 , RESET , MODE0 , MODE1 , CL , M/S , AMP , CCL , DIO2*3 Applies to VLCDL, R pin.
*4 Applies to VHL, R pin.
*5 Applies to VEEL,R pin.
*6 Applies to VLL,R pin.

* 8 Follow the sequence of activation and inactivation for the following power supplies and signals.
And this sequence should be applied when using built - in switching circuit.
If the sequence is not followed, it may cause LSI malfunction, permanent damage, or adverse effects.



(0 ms: Minimum specification)

8.1 Power on

(1) Turn on the power supply in the order of GND-VCC, GND-VLCD (VH), and VM. VM-VEE is generated automatically. In this case, input GND to the DISP pin.
(2) The LCD level forcibly outputs the VM level by the DISPOFF function.
(3) The DISPOFF function has a priority even if input signal distortion occurs immediately after VCC input.
(4) Then input the predetermined signals to initialize the driver registers. In this case, assure a period for more than one frame.
(5) Preparation for normal display is thus completed. Cancel the DISPOFF function by setting the DISP pin to VCC. At this point, the levels of VEE (VL), VLCD (VH) and VM must have reached the predetermined respective voltage.

8.2 Shut down

As a rule, shut down should be in the oppsite order that is used for power on.
(1) Set the DISP pin to GND.
(2) At first shut off the LCD power supply GND-VCLD (VH). At the same time VM-VEE (VL) automaticaly get to VM level. Next shut off the VM.
(3) Set VCC and the input signal to GND.
At this point, VEE (VL), VLCD (VH) and VM pin input must completely drop to 0 V.
Since the DISPOFF function is inactivated when the VCC level drops to GND, the LCD output may output a level other than VM. Therefore, an incorrect display may appear at shut down or power on.

Electric Characteristics

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DC characteristics (VCC = 2.5 to 5.5V, GND = 0V, VLCD - VEE = 15 to 43V, Ta = - 30 to +75˚C

Items	Symbol	Applicable Pins	min.	typ.	max.	Unit	Conditions	Note
Input high level voltage	ViH	DIO1,$\overline{DISP}$,SHL,M,$\overline{M}$/S, MWS 0 to 4,RESET,CL, MODE0,MODE1,$\overline{DOC}$ AMP,CCL,DIO2	0.7 × VCC	–	VCC	V		
Input low level voltage	ViL		0	–	0.3×VCC	V		
Output high level voltage	VOH	M,$\overline{DOC}$,DIO1,DIO2	VCC - 0.4	–	–	V	IOH = - 0.4 mA	
Output low level voltage	VOL	M,$\overline{DOC}$,DIO1,DIO2	–	–	0.4	V	IOL = 0.4 mA	
ON resistance between Vi - Xj	RON	X1 to X240, V pin	–	0.7	2.0	kΩ	Ion = 150μA	*1
Input leak current (1)	IiL1	DIO1,$\overline{DISP}$,SHL,M,$\overline{M}$/S, MWS 0 to 4,RESET,CL, MODE0,MODE1,$\overline{DOC}$ AMP,CCL,DIO2	- 5	–	5	μA	VIN = VCC to GND	
Input leak current (2)	IiL2	VH,VL,VM,C1,C2	- 25	–	25	μA		
Current consumption (1)	ICC1	VCC	–	TBD	TBD	μA	Vcc=3.3V,VLCD-VEE=40V fCL=19.2kHz,fM=1.5kHz	*2
Current consumption (2)	ICC2	VCC	–	TBD	TBD	μA	Vcc=5.0V,VLCD-VEE=40V fCL=19.2kHz,fM=1.5kHz	
Current consumption (2)	ILCD	VLCD	–	TBD	TBD	μA	Vcc=3.3V,VLCD-VEE=40V fCL=19.2kHz,fM=1.5kHz	

*1 Indicates the resistance between one of the pins X1 -X240 and one of the voltage supply pins VH, VL,or VM,When load current is applied to the X pin; defined under the following conditions :

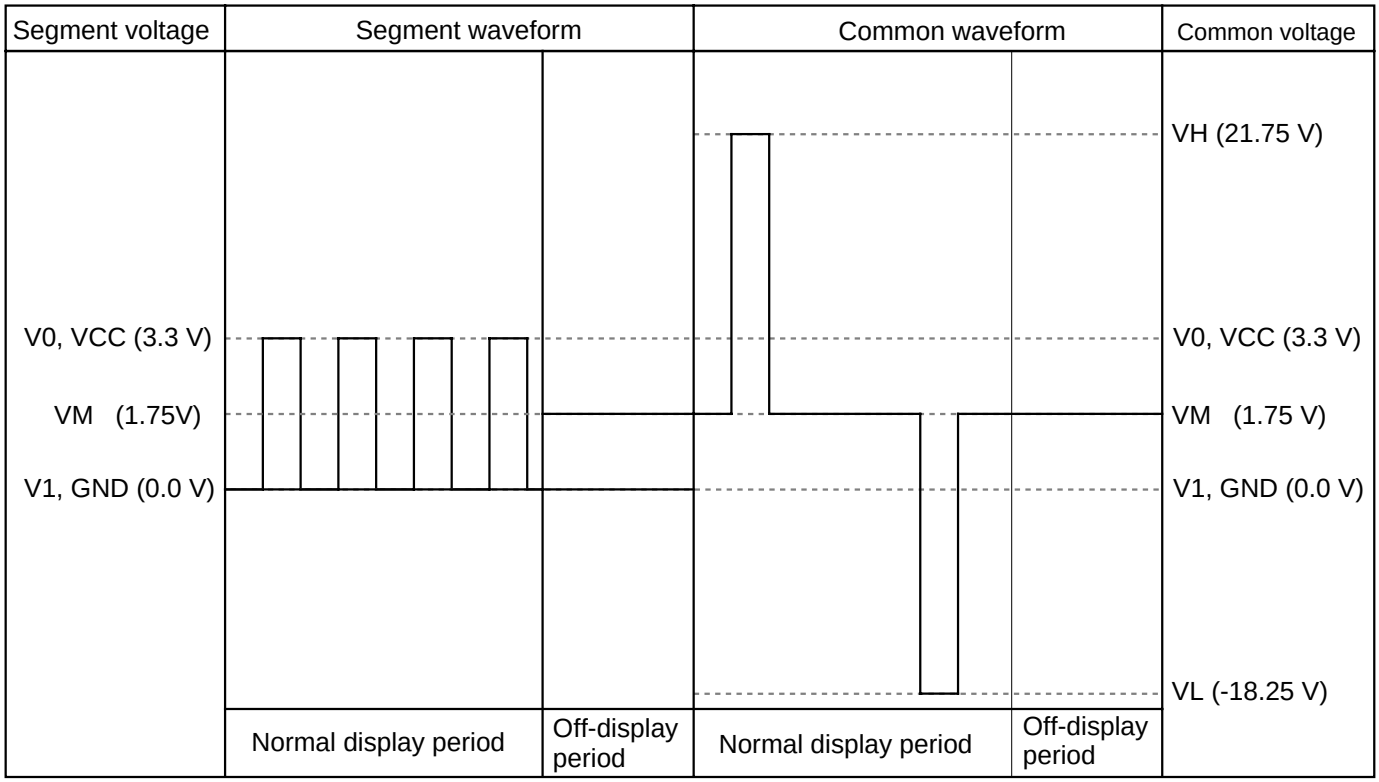
VLCD=VH=21.75V, VEE=VL= -18.5V, VM=1.75V, and GND= 0V.

VH, VL, and VM voltage must be within VLCD-VM ≥ VH-VM =21.5 to 7.5V

VEE-VM ≤ VL-VM= - 21.5 to -7.5V, 6.0 ≥ VM ≥ -0.3V , and VH > VM > VL.

*2 Input and output currents are excluded. When a CMOS input is left floating,excess current flows from the power supply through the input circuit. To avoid this,ViH and ViL must be held at VCC and GND, respectively.

*3 The voltage relationship of each signal is as follows:



AC characteristics (Common driver timing 1) : VCC = 2.5 to 5.5V, GND = 0V, VLCD - VEE = 15 to 43V, Ta = -30 +75°C

Item	Symbol	Pin Name	min.	max.	Unit	Note
Clock cycle time	tCYC	CL	400	—	ns	
CL high-level width	tCWH	CL	25	—	ns	
CL low-level width	tCWL	CL	370	—	ns	
CL rising time	tr	CL	—	30	ns	
CL falling time	tf	CL	—	30	ns	
Data set-up time	tDS	DIO1,DIO2, CL	100	—	ns	
Data hold time	tDH	DIO1,DIO2, CL	10	—	ns	
Data output delay time	tDD	DIO1,DIO2, CL	—	150	ns	*1
M output delay time	tMD	M, CL	—	150	ns	*1
M set uop time	tMS	M, CL	20	—	ns	
M Hold time	tMH	M,CL	20	—	ns	
DOC delay time 1	tDOC1	$\overline{DISP}$,$\overline{DOC}$	—	300	ns	*2
DOC delay time 2	tDOC2	DIO1,DIO2,$\overline{DOC}$	—	300	ns	*2

AC characteristics (Common driver timing 2) : VCC = 2.5 to 4.5V, GND = 0V, VLCD - VEE = 43 V, Ta = - 30 + 75°C

Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Output delay time 1	tpd1	X(n), M	—	1.2	µs	*2

Ac characteristics (Common driver timing 3) : VCC =42.5 to 4.5V, GND = 0V, VLCD - VEE = 43 V, Ta = - 30 + 75°C

Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Output delay time 1	tpd1	X(n), M	—	0.7	µs	*2

Notes : *1. Defined by connecting the load circuit shown in figure 4
*2. Defined by connecting the load circuit shown in figure 4

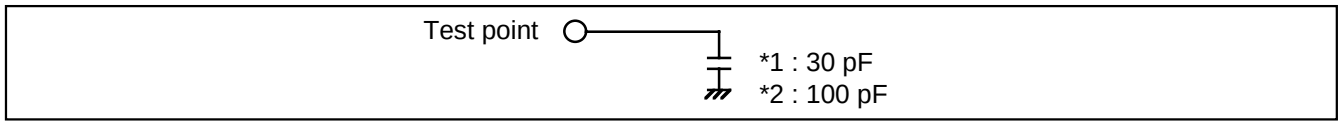
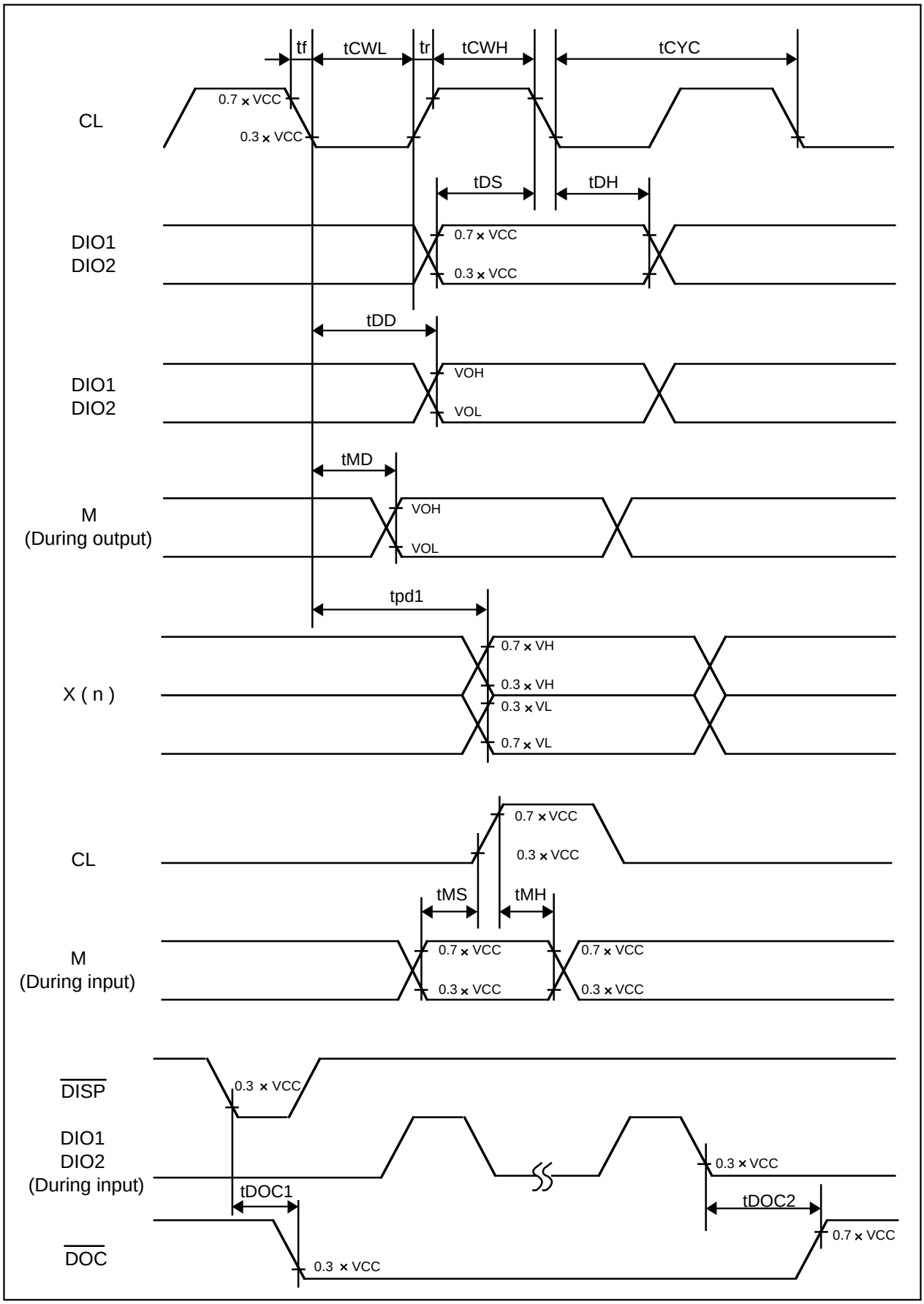
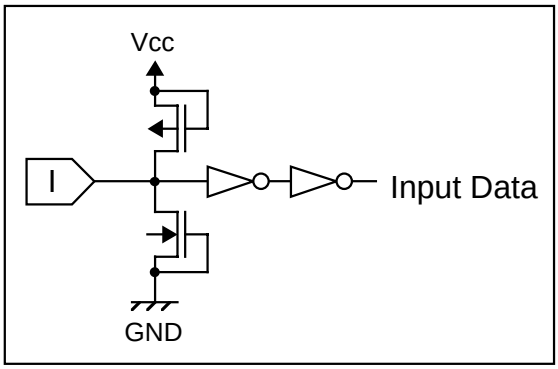


Figure 4 Load circuit

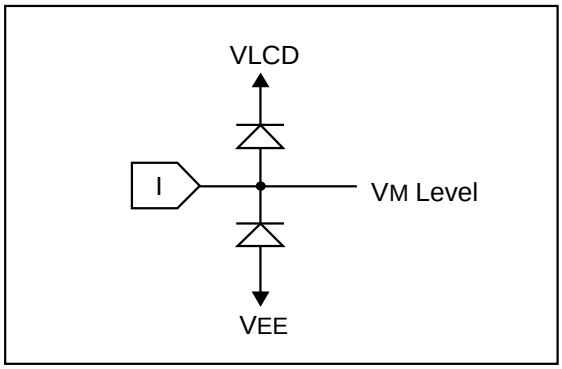

tf
tCWL
tr
tCWH
tCYC
CL
0.7 × VCC
0.3 × VCC
tDS
tDH
DIO1
DIO2
0.7 × VCC
0.3 × VCC
tDD
DIO1
DIO2
VOH
VOL
tMD
M
(During output)
VOH
VOL
tpd1
X (n)
0.7 × VH
0.3 × VH
0.3 × VL
0.7 × VL
CL
0.7 × VCC
0.3 × VCC
tMS
tMH
M
(During input)
0.7 × VCC
0.3 × VCC
0.7 × VCC
0.3 × VCC
DISP
0.3 × VCC
DIO1
DIO2
(During input)
0.3 × VCC
tDOC1
tDOC2
DOC
0.3 × VCC
0.7 × VCC

Terminal Configuration

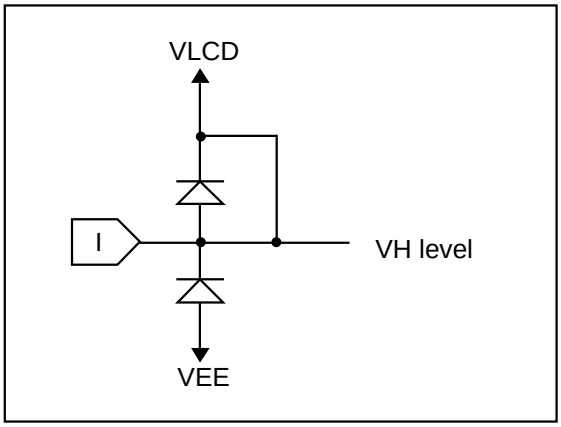
Terminal Configuration (1)



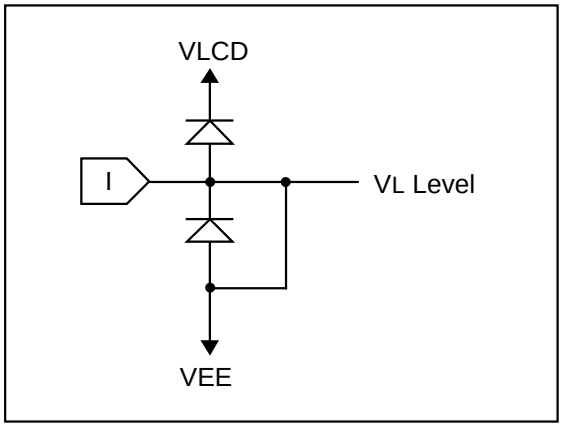
Input Terminal 1
Applicable terminals :
CL, CCL, SHL, MODE 0, 1, AMP
$\overline{DISP}$, RESET, MWS 0 to 4, $\overline{M}$/S



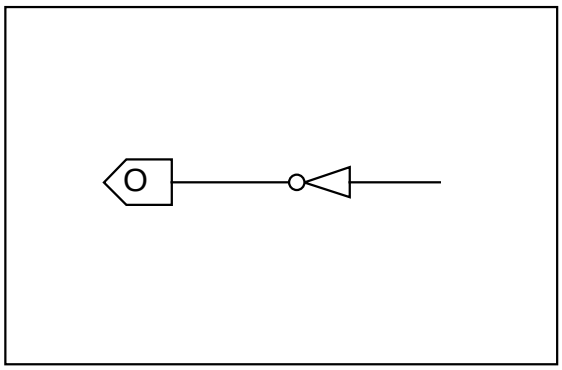
Input Terminal 2
Applicable terminals :$V_{MR,L}$
* V_{MR} terminal connect with V_{ML} terminal in LSI.



Input Terminal 3
Applicable terminals :V_{HR},
* V_{HR} terminal connect with V_{HL} terminal in LSI.

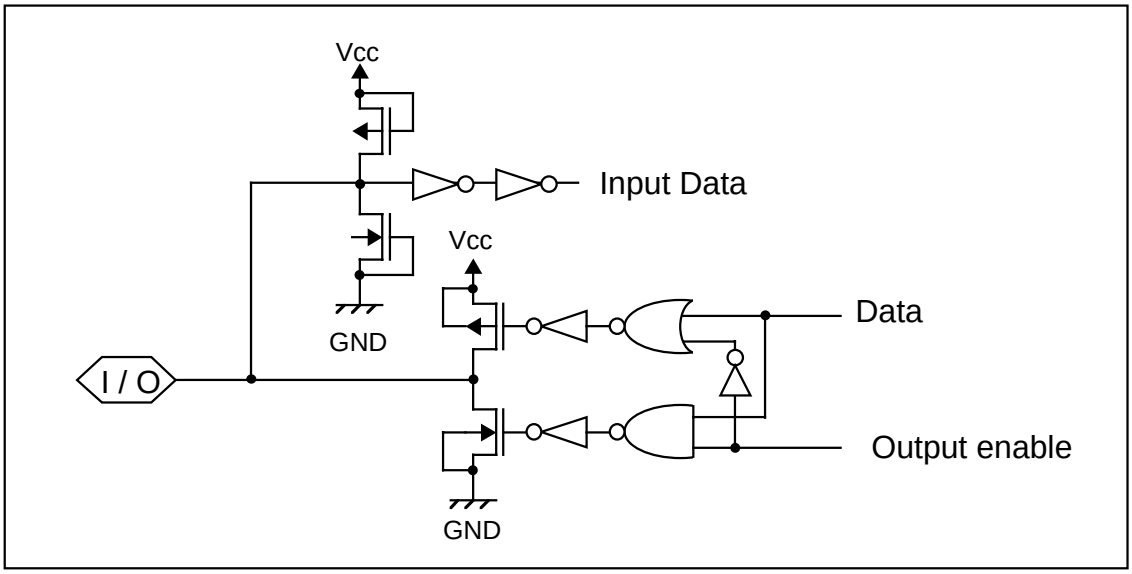


Input Terminal 4
Applicable terminals :V_{LR},
* V_{LR} terminal connect with V_{LL} terminal in LSI.

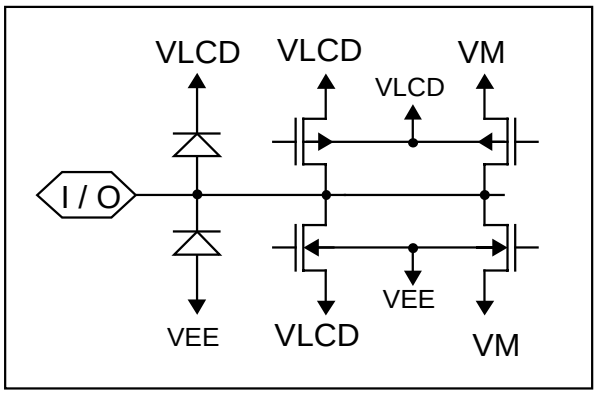


Output Terminal 1
Applicable terminals :$\overline{DOC}$

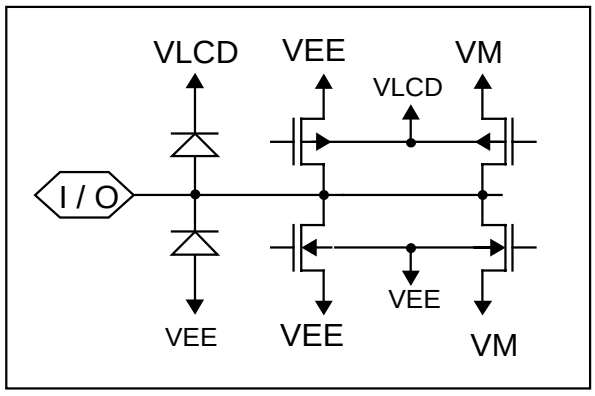
Terminal Configuration (2)



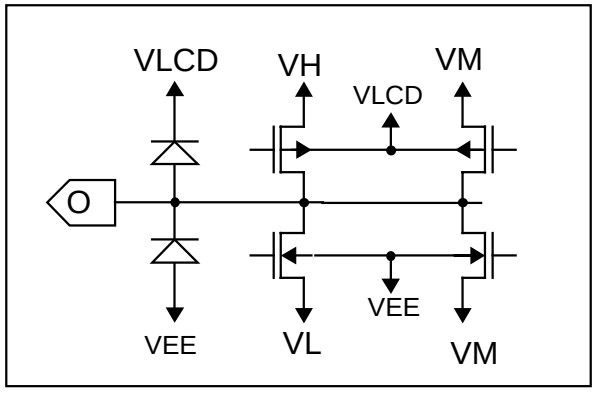
I/O Terminal 1 Applicable terminals : DIO1,DIO2, M



I/O Terminal 2
Applicable terminals :C1



I/O Terminal 3
Applicable terminals :C2



LCD drive Output Terminal
Applicable terminals :X1 to X240

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