

### 6.5 Gbps 8x8 Asynchronous Crosspoint Switch

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## Features

- 8 input by 8 output crosspoint switch
- 6.5 Gbps NRZ data bandwidth
- Global and individual programmable Input Signal Equalization (ISE) and output drive levels
- On-board PRBS Generator/Detector with 10-bit, user-definable pattern
- 2.5 or 3.3 V CMOS/TTL control I/O
- Differential CML data output driver
- Soft power-down for unused channels
- Programmable data output values
- 125 MHz program port
- On-chip input and output terminations
- Single 2.5 V supply, 3.3 V option for control port
- 1.8 W typical power dissipation
- High-performance CBGA package

## Applications

- Loopback
- Protection Switching
- Line Driver/Receiver
- Line Reordering
- Wideband Signal Clean-Up

## General Description

The VSC3108 is an 8x8 asynchronous crosspoint switch designed to carry broadband data streams. The fully non-blocking switch core is programmed through a multi-mode port interface that allows random access programming of each input/output connection. A high degree of signal integrity is maintained throughout the chip by fully differential signal paths.

Each data output can be programmed to connect to one of the eight inputs. The signal path is unregistered and fully asynchronous, so there are no restrictions on the phase, frequency, or signal pattern on any input. Each high-speed output is a fully differential switched current driver with on-die terminations for maximum signal integrity. Data inputs are terminated on-die through 100  $\Omega$  resistors between true and complement inputs with a common connection to an internal bias source, facilitating AC-coupling to the switch inputs.

Programming of the VSC3108 is effected using a 10-bit, non-multiplexed bus, in conjunction with the  $\overline{RD}$  and  $\overline{WR}$  pins.

Unused channels may be powered down by means of register programming. This allows more efficient use of the switch in applications that require only a subset of the channels.

The VSC3108 and VSC3108-01 are available in a 69-pin CBGA package.

## Block Diagrams

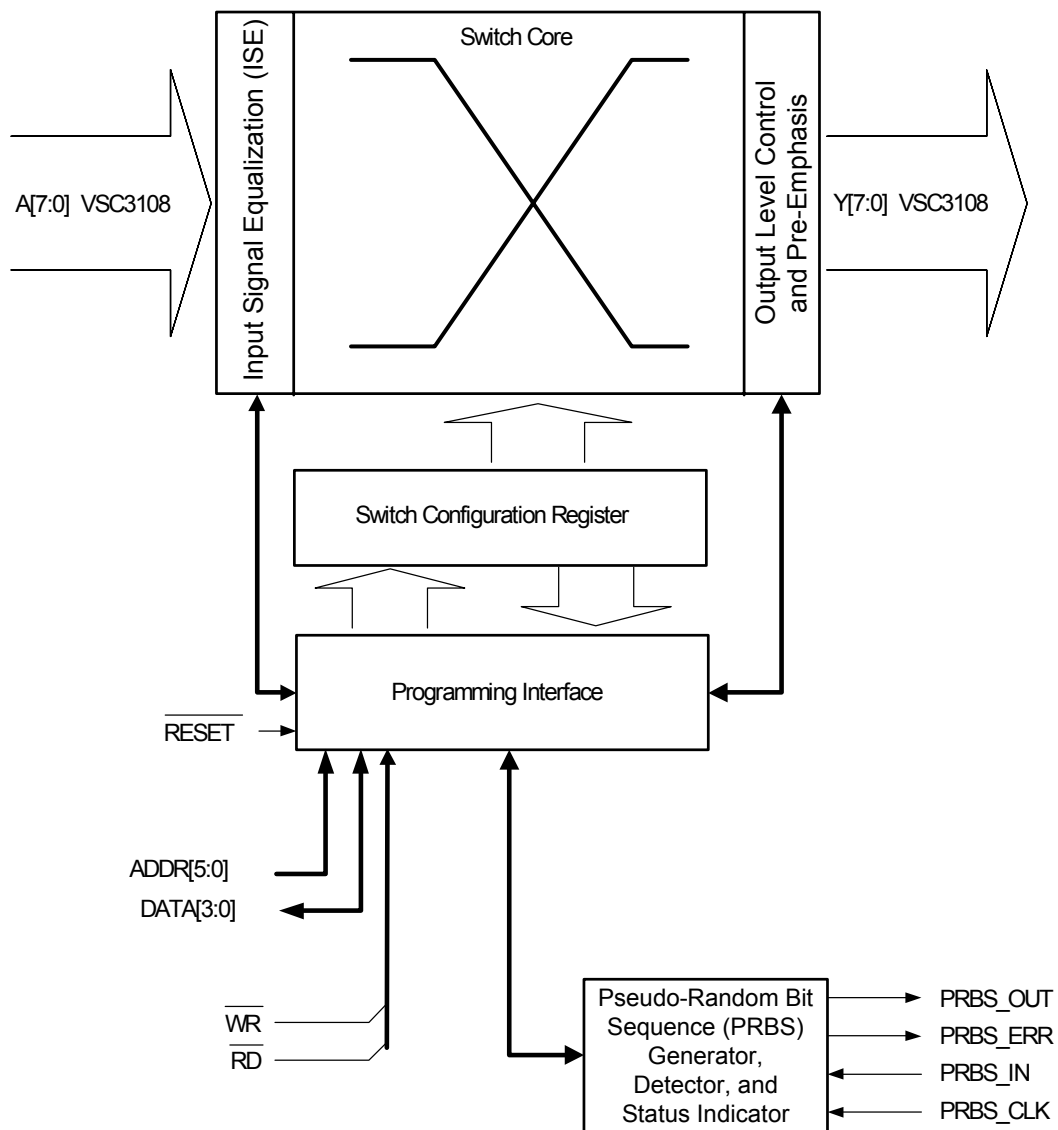


Figure 1. Block Diagram

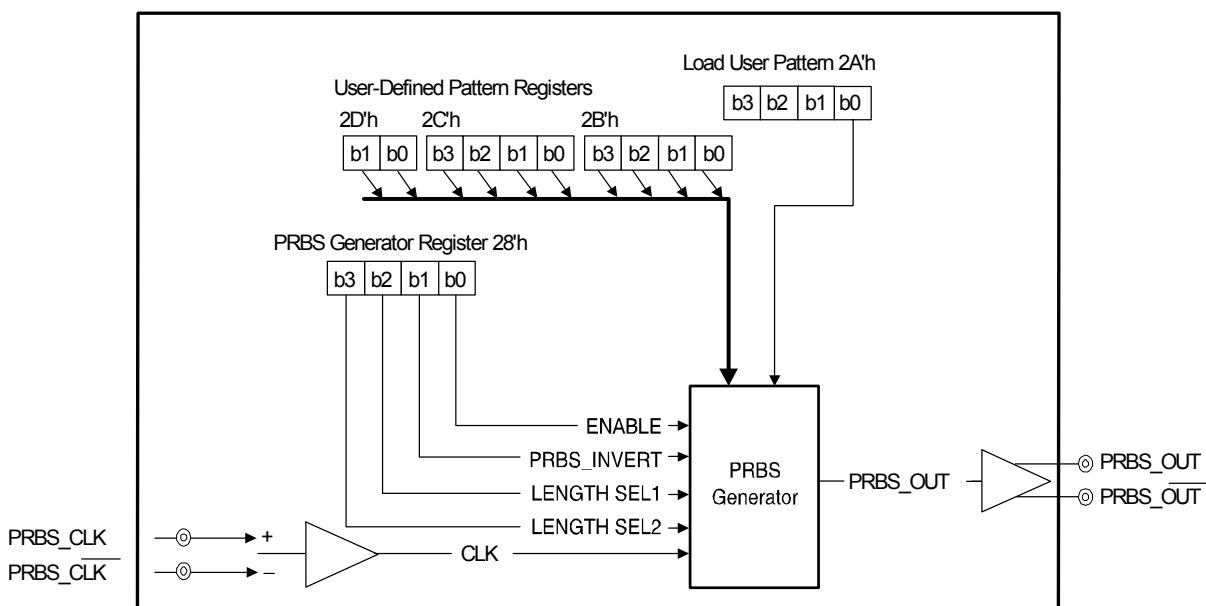


Figure 2. PRBS Generator Block Diagram

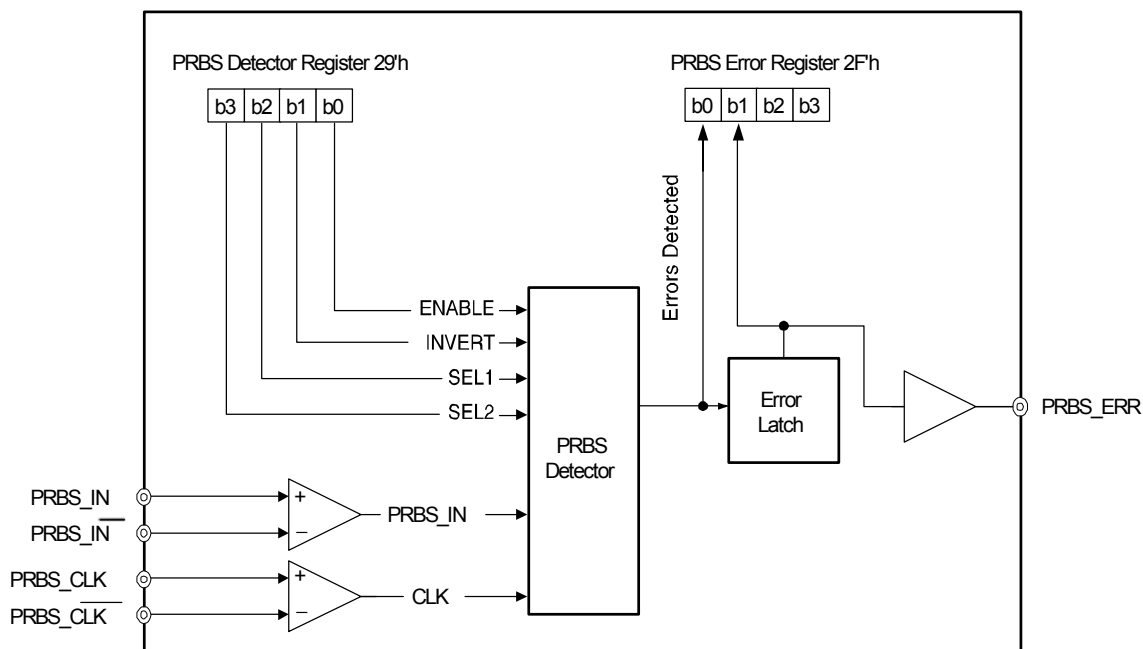


Figure 3. PRBS Error Detector Block Diagram

## Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

### Revision 4.3

Revision 4.3 of this datasheet was published on April 2, 2008. In revision 4.3 of the document, the VSC3108VP-01, VSC3108XVP-01, VSC3108SX-01, and VSC3108XSX-01 parts were added. For more information, see [“Ordering Information”](#), page 27.

### Revision 4.2

Revision 4.2 of this datasheet was published on June 4, 2007. The following is a summary of the changes implemented in the datasheet:

- In the Register Summary Map, the bit range for the global input signal equalization and individual input signal equalization registers was corrected from 1:0 to 2:0 and the address range for the switch array connection register was corrected from 0'h–3'h to 0'h–7'h.
- The output pre-emphasis section was updated to include information about the nominal boost output level settings.
- The PRBS detector rate parameter was added.
- The minimum value for the input common-mode voltage parameter was updated.

### Revision 4.1

Revision 4.1 of this datasheet was published on September 24, 2004. The following is a summary of the changes implemented in the datasheet:

- The device is now available in four package types, including lead(Pb)-free packages VSC3108XVP and VSC3108XSX.
- Thermal specifications were added for the VSC3108XVP, VSC3108SX, and VSC3108XSX packages.

### Revision 4.0

Revision 4.0 of this datasheet was published on April 21, 2004. This was the first production-level publication of the document.

# Functional Descriptions

## Power-On RESET

The VSC3108 has a built-in power-on reset function to ensure the matrix is properly configured as the chip powers up. After the power-on-reset, or when the  $\overline{\text{RESET}}$  pin has been asserted, the switch is configured in an “all outputs off” state. The switch then draws additional power as each output is programmed. Care must be taken to keep power supply above 2.25 Vdc by providing adequate supply decoupling.

## Software Power-Down

With the software power-down feature, unused outputs may be disabled by setting the MSB of the DATA bus to ‘1’ and executing a write to the register associated with the output (00’h to 07’h) that is to be shut down. Programming a valid input address reactivates the channel. It is recommended that any changes in programming that effect power be executed only as part of an initialization sequence. This guards against the effects of any switching transients that might result from a sudden change in the power supply current.

## Output Pre-Emphasis

Pre-emphasis at the output driver decreases deterministic jitter and increases signal amplitude of the signal after traveling through PCB traces and between devices. The output pre-emphasis is adjustable to compensate for different trace lengths and board characteristics. The settings in the Pre-emphasis Configuration register allow the user to choose between 16 different relaxation times for the signal amplitude boost.

The effectiveness of a given setting depends on both the length of the trace and the properties of the surrounding dielectric. This control can be applied either to all the outputs globally or to each output individually. [Register 1](#) on page 10 shows the format for programming the pre-emphasis globally and [Register 2](#) on page 10 shows the individual registers. To identify the correct address for programming the pre-emphasis setting of an individual output, the number of the output is added to the base address, 10’h.

Pre-emphasis must be enabled in the Output Configuration register before the pre-emphasis settings will take effect. Output pre-emphasis is only available with nominal boost output level settings. Pre-emphasis is not available in the high output level setting.

## Pre-Emphasis Enable

In addition to setting a pre-emphasis level, the pre-emphasis enable bit must be set in order to use the pre-emphasis feature of the output buffers. This control can be set either globally or individually. Setting the Global Output Configuration register affects all outputs and changes all of the settings in the register. For example, setting the global pre-emphasis also sets the output levels and output signal states for all of the outputs. The Individual Output Configuration registers allow each output to be configured independently. To identify the correct address for programming the configuration setting of an individual output, the number of the output is added to the base address, 18’h.

## PRBS Generator/Detector

The PRBS Generator/Detector is capable of generating and detecting four NRZ patterns:  $2^7-1$ ,  $2^{10}-1$ ,  $2^{23}-1$ , as well as a 10-bit, user-defined pattern. The main purpose of the PRBS Generator/Detector is switch diagnostics and signal tracing. See the block diagram of the PRBS Generator in [Figure 2](#) on page 3. The data rate of the PRBS Generator/Detector is determined by the external clock signal to a maximum of 4 Gbps. The PRBS output data is clocked on the

rising edge of the clock. The PRBS function controls are located in the PRBS Configuration registers at addresses 28'h to 2F'h.

The PRBS Generator is enabled by writing '1' into bit 0 of register 28'h. Pattern length is selected using register 28'h, bits 3 and 2. Setting '00' generates the pattern  $2^7-1$ , setting '01' generates  $2^{10}-1$ , and '10' generates  $2^{23}-1$ . Setting '11' generates the user-defined pattern. It is possible to invert the pattern by writing a '1' into register 28'h, bit 1.

The PRBS Detector uses the same clock as the PRBS Generator. See the block diagram of the PRBS Detector in [Figure 3](#) on page 3. It may be necessary to invert CLK in order to compensate for the phase difference between data input and the clock signal. The PRBS Detector is enabled by writing a '1' into bit 0 of register 29'h. The detector pattern length is selected by bits 3 and 2 of register 29'h, respectively: '00' represents pattern  $2^7-1$ , '01' represents  $2^{10}-1$ , '10' represents  $2^{23}-1$ , and '11' represents a user-defined pattern. It is possible to invert the PRBS pattern that is coming into the pattern detector by asserting '1' in register 29'h, bit 1. This is used to detect an inverted pattern from the PRBS Generator.

The 10-bit, user-defined pattern spans three, 4-bit registers at 2B'h, 2C'h, and 2D'h. Once the pattern has been set in the appropriate registers, it must be loaded into the PRBS Generator. To execute the pattern load operation, bit 0 in register 2A'h must be held HIGH for at least one clock cycle of the PRBS clock. The new pattern does not become active until the same load bit is de-asserted to '0'.

The Error Detector is not enabled until the Pattern Detector matches the pattern coming into the Detector. It can take up to 30 clock cycles to match the pattern. If an error is detected, bit 1 of register 2F'h is set to '1'. The error bit is cleared on READ. Bit 0 of register 2F'h mimics the PRBS\_ERR bit and may toggle while  $\overline{RD}$  is held LOW.

## Output Level

Two different output levels can be programmed for all outputs. The nominal output level is 650 mV peak-to-peak (p-p) differential and the high output level is 1300 mVp-p differential. This control can be set both globally and individually. Setting the Global Output Configuration register affects all outputs and changes all the settings in the register. For example, setting the global output level also sets the pre-emphasis enable and output signal states for all the outputs. The Individual Output Configuration registers allow each output to be configured independently. To identify the correct address for programming the configuration setting of an individual output, the number of the output is added to the base address, 18'h.

## Boost Mode

In addition to the regular drive settings, a boost mode is available that adds approximately 100-200 mV to the drive level of the programmed output. The level of boost depends upon both the current drive setting and the chip power supply voltage. Both the higher drive setting and higher supply voltages increases the boost level. By using the boost function, the output swing can be user-adjusted by controlling the power supply voltage (within the specified maximum limits).

The boost function is activated with a separate set of registers, 0D'h and 0E'h. Setting each bit in the register activates the boost function for its respective output. The LSB of 0D'h corresponds to output 0, LSB+1 corresponds to output 1, and so on. Register 0E'h controls the boost function for outputs 4 through 7 in the same manner. [Register 4](#), "Individual Output Boost Mode Configuration," on page 11 summarizes the Boost mode register configuration, relating the bit settings to individual output channels.

Note that activating the boost function overrides power-down programming operations through the connection registers. The result of a power-down connection leaves the output powered and operational, but with a low level output swing. To assure complete power-down of a given output, be sure to clear its respective bit in the boost register.

## Output Signal State

Manipulating the output signal state bits permits the user to force a DC signal of either polarity onto all of the outputs. With the bits set to '00', the outputs operate normally and pass the NRZ data from the connected input. Selecting any of the other three possible states overrides the output signal and sets all outputs to a DC state as described in [Register 3](#), "Global Output Configuration," on page 10 and [Register 5](#), "Individual Output Configuration," on page 11. This control can be set both globally and individually. Setting the Global Output Configuration register affects all outputs and changes all the settings in the register. For example, setting the global output state also sets the output levels and the pre-emphasis enable for all of the outputs. The Individual Output Configuration registers allow each output to be configured independently. To identify the correct address for programming the configuration setting of an individual output, the number of the output is added to the base address, 18'h.

## Equalization State

Adjusting the Input Signal Equalization (ISE) input setting changes the input response of the input buffers. Four levels of equalization are available ranging from "off," which provides no additional equalization, through "maximum," which provides the greatest amount of equalization. Less equalization is useful for shorter trace lengths, and more equalization helps compensate for signal degradation due to long trace lengths. This control can be set either globally or individually. Setting the Global Input Equalization register affects all inputs. The Individual Input Equalization registers allow each input to be configured independently. To identify the correct address for programming the ISE setting of an individual output, the number of the input is added to the base address, 20'h.

## Programming Interface

The VSC3108 programming interface uses a non-multiplexed address/data bus. The conventions listed in [Table 1](#) are used when describing the programming interface.

**Table 1. Conventions**

| Convention                      | Description                                       |
|---------------------------------|---------------------------------------------------|
| SIGNAL NAME                     | Active HIGH signal                                |
| $\overline{\text{SIGNAL NAME}}$ | Active LOW signal                                 |
| ADDR                            | Identifies OUTPUT channel to be programmed        |
| DATA                            | Identifies INPUT channel to be programmed         |
| '1'                             | A logic level high signal. Also denoted by "HIGH" |
| '0'                             | A logic level low signal. Also denoted by "LOW"   |

## Register Use

All registers are accessed in the manner described in the programming interface description read and write functions. Each register has a corresponding address which, when written to with a data word, alters the functions defined for that register as described by the registers listed in “Registers”, page 9. Except for a ‘1’ in bit 3 of each Switch Array register, all bits in all registers initialize to ‘0’. The first register table, Table 3, page 9, is a summary that provides an overview of the information in the other register tables. The register tables following Table 3 consist of detailed descriptions of the functions controlled in each register.

## Write Operation

A write operation is completed when the  $\overline{WR}$  signal is strobed LOW. On the rising edge of the  $\overline{WR}$  signal the value that is present on the DATA bus is latched into the register identified by the ADDR bus. Figure 4 on page 17 shows the programming sequence for parallel mode write operations.

## Parallel Mode—Read Operation

The VSC3108 supports parallel readback to verify programming information in the switch fabric and the various configuration registers. Upon assertion of the  $\overline{RD}$  signal LOW, the device reverses the direction of the DATA bus and asserts the requested data out onto the DATA pins. The read data will remain valid until  $\overline{RD} = '1'$ . Figure 4 on page 17 shows the programming sequence for parallel mode read operations.

## Switch Configuration

**Table 2. Switch Array Connection Examples**

| Output ADDR[5:0] | Input DATA[3:0] | Description                   | R/W |
|------------------|-----------------|-------------------------------|-----|
| 00000'b          | 0000'b          | Program output Y0 to input A0 | R/W |
| 00001'b          | 0000'b          | Program output Y1 to input A0 | R/W |
| 00010'b          | 0000'b          | Program output Y2 to input A0 | R/W |
| ⋮                | ⋮               | ⋮                             | ⋮   |
| 00111'b          | 0000'b          | Program output Y7 to input A0 | R/W |
| ⋮                | ⋮               | ⋮                             | ⋮   |
| 00000'b          | 0111'b          | Program output Y0 to input A7 | R/W |
| 00001'b          | 0111'b          | Program output Y1 to input A7 | R/W |
| 00010'b          | 0111'b          | Program output Y2 to input A7 | R/W |
| ⋮                | ⋮               | ⋮                             | ⋮   |
| 00111'b          | 0111'b          | Program output Y7 to input A7 | R/W |

# Registers

**Table 3. Register Map**

| Name                                 | ADDR[5:0]   | DATA[3:0]                                                                                                   |                                                             |                                           |                                                |
|--------------------------------------|-------------|-------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------|------------------------------------------------|
|                                      |             | Bit 3                                                                                                       | Bit 2                                                       | Bit 1                                     | Bit 0                                          |
| Switch Array Connection              | 0'h – 07'h  | 0'h through 7'h connects to input.<br>8'h through F'h turns off outputs specified in ADDR.                  |                                                             |                                           |                                                |
| Global Pre-Emphasis Duration         | 08'h        | Min = 0'h, Max = F'h                                                                                        |                                                             |                                           |                                                |
| Global Output Configuration          | 09'h        | 00 = No effect<br>01 = Force all outputs to 0<br>10 = Force all outputs to 1<br>11 = Force all outputs to 0 |                                                             | 1 = HIGH Power<br>0 = Nominal Power       | 1 = Pre-emphasis ON<br>0 = Pre-emphasis OFF    |
| Global Input Signal Equalization     | 0A'h        | Not used.<br>Resets to 0. Leave at 0 for normal operation.                                                  | 000 = OFF<br>001 = Minimum<br>011 = Medium<br>111 = Maximum |                                           |                                                |
| Individual Boost Mode                | 0D'h        | Output 3<br>1 = Boost ON<br>0 = Boost OFF                                                                   | Output 2<br>1 = Boost ON<br>0 = Boost OFF                   | Output 1<br>1 = Boost ON<br>0 = Boost OFF | Output 0<br>1 = Boost ON<br>0 = Boost OFF      |
| Individual Boost Mode                | 0E'h        | Output 7<br>1 = Boost ON<br>0 = Boost OFF                                                                   | Output 6<br>1 = Boost ON<br>0 = Boost OFF                   | Output 5<br>1 = Boost ON<br>0 = Boost OFF | Output 4<br>1 = Boost ON<br>0 = Boost OFF      |
| Individual Pre-Emphasis Duration     | 10'h – 17'h | Minimum = 0'h, Maximum = F'h                                                                                |                                                             |                                           |                                                |
| Individual Output Configuration      | 18'h – 1F'h | 00 = No effect<br>01 = Force all outputs to 0<br>10 = Force all outputs to 1<br>11 = Force all outputs to 0 |                                                             | 1 = HIGH Power<br>0 = Nominal Power       | 1 = Pre-emphasis ON<br>0 = Pre-emphasis OFF    |
| Individual Input Signal Equalization | 20'h – 27'h | Resets to 0. Leave at 0 for normal operation.                                                               | 000 = OFF<br>001 = Minimum<br>011 = Medium<br>111 = Maximum |                                           |                                                |
| PRBS Generator Configuration         | 28'h        | Generator pattern<br>00 = $2^7 - 1$ , 01 = $2^{10} - 1$ , 10 = $2^{23} - 1$                                 |                                                             | 1 = Invert pattern<br>0 = Normal pattern  | 1 = Enable generator<br>0 = Disable generator  |
| PRBS Detector Configuration          | 29'h        | Detector pattern<br>00 = $2^7 - 1$ , 01 = $2^{10} - 1$ , 10 = $2^{23} - 1$                                  |                                                             | 1 = Invert pattern<br>0 = Normal pattern  | 1 = Enable detector<br>0 = Disable detector    |
| PRBS User Pattern Select             | 2A'h        | Not used. Resets to zero. Leave at zero for normal operation.                                               |                                                             |                                           | 1 = Latch user pattern<br>0 = Normal operation |
| PRBS User-Defined Pattern            | 2B'h        | Bits [3:0] of user pattern [9:0]                                                                            |                                                             |                                           |                                                |
| PRBS User-Defined Pattern            | 2C'h        | Bits [7:4] of user pattern [9:0]                                                                            |                                                             |                                           |                                                |
| PRBS User-Defined Pattern            | 2D'h        | Not used.                                                                                                   |                                                             | Bits [9:8] of user pattern [9:0]          |                                                |

## Output Configuration

### Register 1: Global Pre-Emphasis Setting

| <b>Name:</b> Global Pre-Emphasis Setting                           |                                                                 | <b>Address:</b> 08'h |     |
|--------------------------------------------------------------------|-----------------------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                   |                                                                 |                      |     |
| <b>Description:</b> Adjusts pre-emphasis for varying line lengths. |                                                                 |                      |     |
| Bit                                                                | Bit Description                                                 | Reset Value          | R/W |
| 3-0                                                                | Range 0 to 15 0000 = 450 ps<br>0001 = ~450 ps to 1111 = ~700 ps | 0'h                  | R/W |

### Register 2: Individual Pre-Emphasis Setting

| <b>Name:</b> Individual Pre-Emphasis Setting                       |                                                                 | <b>Address:</b> 10'h – 17'h |     |
|--------------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------|-----|
| <b>Type:</b> R/W                                                   |                                                                 |                             |     |
| <b>Description:</b> Adjusts pre-emphasis for varying line lengths. |                                                                 |                             |     |
| Bit                                                                | Bit Description                                                 | Reset Value                 | R/W |
| 3-0                                                                | Range 0 to 15 0000 = 450 ps<br>0001 = ~450 ps to 1111 = ~700 ps | 0'h                         | R/W |

### Register 3: Global Output Configuration

| <b>Name:</b> Global Output Configuration                              |                                                                                                                                                 | <b>Address:</b> 09'h |     |
|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                      |                                                                                                                                                 |                      |     |
| <b>Description:</b> Sets output state, level and enable pre-emphasis. |                                                                                                                                                 |                      |     |
| Bit                                                                   | Bit Description                                                                                                                                 | Reset Value          | R/W |
| 3-2                                                                   | Output Signal State<br>00 = Normal operation<br>01 = All outputs are set to 0<br>10 = All outputs are set to 1<br>11 = All outputs are set to 0 | 00                   | R/W |
| 1                                                                     | Output Level<br>0 = Nominal level output<br>1 = High level output                                                                               | 0                    | R/W |
| 0                                                                     | Pre-Emphasis Enable<br>0 = Pre-emphasis disabled<br>1 = Pre-emphasis enabled                                                                    | 0                    | R/W |

**Register 4: Individual Output Boost Mode Configuration**

| <b>Name:</b> Boost Mode Enable/Disable                                                 |                                                                   | <b>Address:</b> 0D'h |     |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                                       |                                                                   |                      |     |
| <b>Description:</b> Activate/de-activate Boost mode for corresponding output channels. |                                                                   |                      |     |
| Bit                                                                                    | Bit Description                                                   | Reset Value          | R/W |
| 3                                                                                      | 0 = Boost mode OFF for output 3<br>1 = Boost mode ON for output 3 | 0                    | R/W |
| 2                                                                                      | 0 = Boost mode OFF for output 2<br>1 = Boost mode ON for output 2 | 0                    | R/W |
| 1                                                                                      | 0 = Boost mode OFF for output 1<br>1 = Boost mode ON for output 1 | 0                    | R/W |
| 0                                                                                      | 0 = Boost mode OFF for output 0<br>1 = Boost mode ON for output 0 | 0                    | R/W |

| <b>Name:</b> Boost Mode Enable/Disable                                                 |                                                                   | <b>Address:</b> 0E'h |     |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                                       |                                                                   |                      |     |
| <b>Description:</b> Activate/de-activate Boost mode for corresponding output channels. |                                                                   |                      |     |
| Bit                                                                                    | Bit Description                                                   | Reset Value          | R/W |
| 3                                                                                      | 0 = Boost mode OFF for output 7<br>1 = Boost mode ON for output 7 | 0                    | R/W |
| 2                                                                                      | 0 = Boost mode OFF for output 6<br>1 = Boost mode ON for output 6 | 0                    | R/W |
| 1                                                                                      | 0 = Boost mode OFF for output 5<br>1 = Boost mode ON for output 5 | 0                    | R/W |
| 0                                                                                      | 0 = Boost mode OFF for output 4<br>1 = Boost mode ON for output 4 | 0                    | R/W |

**Register 5: Individual Output Configuration**

| <b>Name:</b> Individual Output Configuration                           |                                                                                                                                                 | <b>Address:</b> 18'h – 1F'h |     |
|------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|-----|
| <b>Type:</b> R/W                                                       |                                                                                                                                                 |                             |     |
| <b>Description:</b> Sets output state, level, and enable pre-emphasis. |                                                                                                                                                 |                             |     |
| Bit                                                                    | Bit Description                                                                                                                                 | Reset Value                 | R/W |
| 3-2                                                                    | Output Signal State<br>00 = Normal operation<br>01 = All outputs are set to 0<br>10 = All outputs are set to 1<br>11 = All outputs are set to 0 | 00                          | R/W |
| 1                                                                      | Output Level<br>0 = Nominal level output<br>1 = High level output                                                                               | 0                           | R/W |
| 0                                                                      | Pre-Emphasis Enable<br>0 = Pre-emphasis disabled<br>1 = Pre-emphasis enabled                                                                    | 0                           | R/W |

## Input Configuration

### Register 6: Global Input Equalization

| <b>Name:</b> Global Input Equalization              |                                                                                                                                      | <b>Address:</b> 0A'h |     |
|-----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                    |                                                                                                                                      |                      |     |
| <b>Description:</b> Adjusts the input equalization. |                                                                                                                                      |                      |     |
| Bit                                                 | Bit Description                                                                                                                      | Reset Value          | R/W |
| 3                                                   | Not used                                                                                                                             | 0                    |     |
| 2-0                                                 | Equalization State<br>000 = No equalization<br>001 = Minimum equalization<br>011 = Medium equalization<br>111 = Maximum equalization | 000                  | R/W |

### Register 7: Individual Input Equalization

| <b>Name:</b> Individual Input Equalization          |                                                                                                                                      | <b>Address:</b> 20'h – 27'h |     |
|-----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|-----|
| <b>Type:</b> R/W                                    |                                                                                                                                      |                             |     |
| <b>Description:</b> Adjusts the input equalization. |                                                                                                                                      |                             |     |
| Bit                                                 | Bit Description                                                                                                                      | Reset Value                 | R/W |
| 3                                                   | Not used                                                                                                                             | 0                           |     |
| 2-0                                                 | Equalization State<br>000 = No equalization<br>001 = Minimum equalization<br>011 = Medium equalization<br>111 = Maximum equalization | 000                         | R/W |

## PRBS Control

### Register 8: PRBS Generator Configuration

| <b>Name:</b> PRBS Generator Configuration                                        |                                                                                                                                 | <b>Address:</b> 28'h |     |
|----------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                                 |                                                                                                                                 |                      |     |
| <b>Description:</b> Configures the operating mode of the on-chip PRBS generator. |                                                                                                                                 |                      |     |
| Bit                                                                              | Bit Description                                                                                                                 | Reset Value          | R/W |
| 3-2                                                                              | Select PRBS generator pattern length<br>11 = 10-bit, user-defined pattern<br>10 = $2^{23}-1$<br>01 = $2^{10}-1$<br>00 = $2^7-1$ | 00                   | R/W |
| 1                                                                                | PRBS output pattern<br>0 = Non-inverted pattern<br>1 = Inverted pattern                                                         | 0                    | R/W |
| 0                                                                                | PRBS generator control<br>0 = Disable PRBS generator<br>1 = Enable PRBS generator                                               | 0                    | R/W |

**Register 9: PRBS Detector Configuration**

| <b>Name:</b> PRBS Detector Configuration                                               |                                                                                                                         | <b>Address:</b> 29'h |     |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                                       |                                                                                                                         |                      |     |
| <b>Description:</b> Configures the operating mode of the on-board PRBS error detector. |                                                                                                                         |                      |     |
| Bit                                                                                    | Bit Description                                                                                                         | Reset Value          | R/W |
| 3-2                                                                                    | Error counter length control<br>11 = 10-bit, user-defined pattern<br>10 = $2^{23}-1$<br>01 = $2^{10}-1$<br>00 = $2^7-1$ | 00                   | R/W |
| 1                                                                                      | PRBS input pattern<br>0 = Non-inverted PRBS input<br>1 = Inverted PRBS input                                            | 0                    | R/W |
| 0                                                                                      | PRBS receiver control<br>0 = Disable PRBS detector<br>1 = Enable PRBS detector                                          | 0                    | R/W |

**Register 10: PRBS Error Status**

| <b>Name:</b> PRBS Error Status                                            |                                                                                                                                       | <b>Address:</b> 2F'h |           |
|---------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------|
| <b>Type:</b> R/W                                                          |                                                                                                                                       |                      |           |
| <b>Description:</b> Reports error status from the on-board PRBS detector. |                                                                                                                                       |                      |           |
| Bit                                                                       | Bit Description                                                                                                                       | Reset Value          | R/W       |
| 3-2                                                                       | Not used                                                                                                                              | 00                   |           |
| 1                                                                         | Latched Error (cleared on read)<br>0 = No errors detected since last read<br>1 = At least one error since last time register was read | 0                    | Read Only |
| 0                                                                         | Unlatched Error Strobe (may toggle during read)<br>0 = No error<br>1 = One or more errors detected                                    | 0                    | Read Only |

**Register 11: PRBS User-Defined Pattern Control**

| <b>Name:</b> PRBS User-Defined Pattern Control                            |                                                                                                                                                                           | <b>Address:</b> 2A'h |     |
|---------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                          |                                                                                                                                                                           |                      |     |
| <b>Description:</b> Reports error status from the on-board PRBS detector. |                                                                                                                                                                           |                      |     |
| Bit                                                                       | Bit Description                                                                                                                                                           | Reset Value          | R/W |
| 3-1                                                                       | Not used                                                                                                                                                                  | 000                  |     |
| 0                                                                         | Load User-defined pattern<br>0 = User pattern active when selected in the PRBS generator configuration<br>1 = Load user pattern. Must remain high for one PRBS_CLK cycle. | 0                    | R/W |

## Register 12: PRBS User-Defined Pattern 1

| <b>Name:</b> PRBS User-Defined Pattern 1                        |                                               | <b>Address:</b> 2B'h |     |
|-----------------------------------------------------------------|-----------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                |                                               |                      |     |
| <b>Description:</b> Defines pattern used by the PRBS generator. |                                               |                      |     |
| Bit                                                             | Bit Description                               | Reset Value          | R/W |
| 3-0                                                             | Bits [3:0] of the 10-bit user-defined pattern | 0000                 | R/W |

## Register 13: PRBS User-Defined Pattern 2

| <b>Name:</b> PRBS User-Defined Pattern 2                        |                                               | <b>Address:</b> 2C'h |     |
|-----------------------------------------------------------------|-----------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                |                                               |                      |     |
| <b>Description:</b> Defines pattern used by the PRBS generator. |                                               |                      |     |
| Bit                                                             | Bit Description                               | Reset Value          | R/W |
| 3-0                                                             | Bits [7:4] of the 10-bit user-defined pattern | 0000                 | R/W |

## Register 14: PRBS User-Defined Pattern 3

| <b>Name:</b> PRBS User-Defined Pattern 3                        |                                                | <b>Address:</b> 2D'h |     |
|-----------------------------------------------------------------|------------------------------------------------|----------------------|-----|
| <b>Type:</b> R/W                                                |                                                |                      |     |
| <b>Description:</b> Defines pattern used by the PRBS generator. |                                                |                      |     |
| Bit                                                             | Bit Description                                | Reset Value          | R/W |
| 3-2                                                             | Not used                                       | 00                   | R/W |
| 1-0                                                             | Bits [9:8] of the 10-bit, user-defined pattern | 00                   | R/W |

## Electrical Specifications

All specifications are qualified under recommended operating conditions unless stated otherwise.

### Maximum Ratings

Table 4. Absolute Maximum Ratings

| Symbol    | Parameter                                          | Minimum | Maximum         | Unit |
|-----------|----------------------------------------------------|---------|-----------------|------|
| $V_{CC}$  | Power supply voltage, potential to GND             | -0.5    | 3.5             | V    |
|           | DC input voltage applied (TTL)                     | -0.5    | $V_{DD0} + 1.0$ | V    |
|           | DC input voltage applied (CML)                     | -0.5    | $V_{CC} + 0.5$  | V    |
| $I_{OUT}$ | Output current                                     | -50     | 50              | mA   |
| $T_C$     | Case temperature under bias                        | -30     | 25              | °C   |
| $T_S$     | Storage temperature                                | -40     | 125             | °C   |
| $V_{ESD}$ | Electrostatic discharge voltage (human body model) | -500    | 500             | V    |

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.



#### ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

### Operating Conditions

Table 5. Recommended Operating Conditions

| Symbol    | Parameter                                                | Minimum | Typical    | Maximum | Unit |
|-----------|----------------------------------------------------------|---------|------------|---------|------|
| $V_{CC}$  | Power supply voltage                                     | 2.375   | 2.5        | 2.625   | V    |
| $V_{DD0}$ | Power supply voltage, programming port <sup>(1, 2)</sup> |         | 2.5 or 3.3 |         | V    |
| T         | Operating temperature range <sup>(3)</sup>               | 0       |            | 110     | °C   |

1. All timing specifications and diagrams reflect 3.3 V.
2. Must track  $V_{CC}$  when  $V_{DD0} = 2.5$  V.
3. Lower limit of specification is ambient temperature and upper limit is die backside temperature.

## AC Characteristics

**Table 6. High-Speed Data Inputs (A,  $\bar{A}$ )<sup>(1)</sup>**

| Symbol                              | Parameter                                          | Typical | Maximum | Unit | Condition                                                                             |
|-------------------------------------|----------------------------------------------------|---------|---------|------|---------------------------------------------------------------------------------------|
| DR <sub>A</sub>                     | Serial NRZ input data rate                         |         | 6.5     | Gbps | Minimum data rate will be limited by the AC-coupling capacitor value (if AC-coupled). |
| t <sub>PD-AY</sub>                  | Propagation delay from any A input to any Y output | 500     |         | ps   |                                                                                       |
| t <sub>SKEW</sub>                   | Output channel-to-channel delay skew               | 20      | 60      | ps   |                                                                                       |
| t <sub>R-A</sub> , t <sub>F-A</sub> | Serial data input rise and fall times              |         | 200     | ps   | 20% to 80%                                                                            |
| D <sub>PRBS-DET</sub>               | PRBS detector rate                                 |         | 4.0     | Gbps | 4.0 GHz differential PRBS clock.                                                      |

1. Inputs are guaranteed by characterization.

**Table 7. High-Speed Data Outputs (Y,  $\bar{Y}$ )<sup>(1)</sup>**

| Symbol                              | Parameter                                                       | Minimum | Typical | Maximum | Unit | Condition                                                                             |
|-------------------------------------|-----------------------------------------------------------------|---------|---------|---------|------|---------------------------------------------------------------------------------------|
| DR <sub>Y</sub>                     | Serial NRZ output data rate                                     |         |         | 6.5     | Gbps | Minimum data rate will be limited by the AC-coupling capacitor value (if AC-coupled). |
| t <sub>Jp-p</sub>                   | Serial output data added delay jitter, peak-peak <sup>(2)</sup> |         |         | 20      | ps   |                                                                                       |
| t <sub>R-Y</sub> , t <sub>F-Y</sub> | Serial output data rise and fall times                          |         | 50      | 80      | ps   | 20% to 80%<br>With 50 $\Omega$ to V <sub>CC</sub> .                                   |
| DC <sub>Y</sub>                     | Serial data output duty cycle                                   | 40      | 50      | 60      | %    | Only relevant with 101010 input data patterns.                                        |
| D <sub>PRBS-DET</sub>               | PRBS detector rate                                              |         |         | 4.0     | Gbps | 4.0 GHz differential PRBS clock.                                                      |

1. Outputs are guaranteed by characterization.

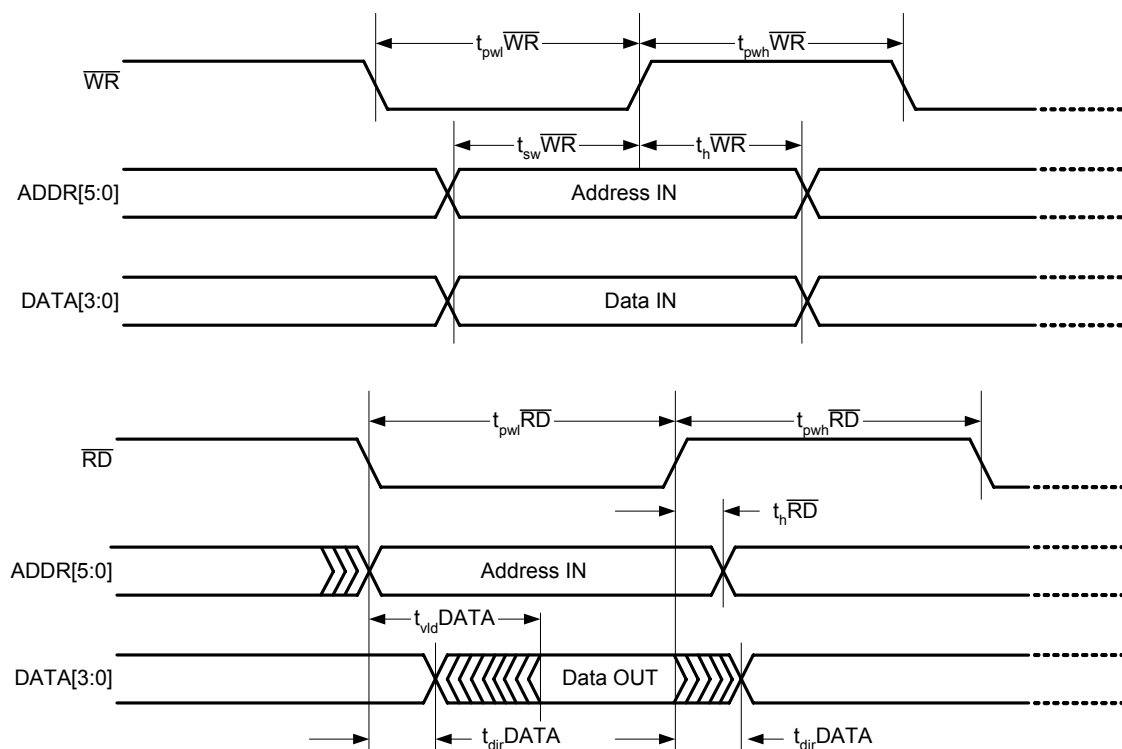
2. Broadband (unfiltered) deterministic jitter added to input: 2<sup>23</sup>-1 PRBS data pattern.

**Table 8. Program Interface**

| Symbol                           | Parameter                                                          | Minimum | Maximum | Unit |
|----------------------------------|--------------------------------------------------------------------|---------|---------|------|
| t <sub>pwl</sub> $\overline{WR}$ | Pulse width for $\overline{WR}$ LOW                                | 4       |         | ns   |
| t <sub>pwh</sub> $\overline{WR}$ | Pulse width for $\overline{WR}$ HIGH                               | 4       |         | ns   |
| t <sub>s</sub> $\overline{WR}$   | Setup time from DATA[3:0] stable to rising edge of $\overline{WR}$ | 4       |         | ns   |
| t <sub>h</sub> $\overline{WR}$   | Hold time for DATA[3:0] after rising edge of $\overline{WR}$       | 4       |         | ns   |
| t <sub>pwl</sub> $\overline{RD}$ | Pulse width for $\overline{RD}$ LOW                                | 24      |         | ns   |
| t <sub>pwh</sub> $\overline{RD}$ | Pulse width for $\overline{RD}$ HIGH                               | 4       |         | ns   |

**Table 8. Program Interface**

| Symbol               | Parameter                                                    | Minimum | Maximum | Unit |
|----------------------|--------------------------------------------------------------|---------|---------|------|
| $t_{h\overline{RD}}$ | Hold time for ADDR[5:0] after rising edge of $\overline{RD}$ | 3       |         | ns   |
| $t_{dirDATA}$        | Time required for ADDR/DATA bus to change direction          | 3       | 8       | ns   |
| $t_{vldDATA}$        | Time until data valid after falling $\overline{RD}$          |         | 20      | ns   |



**Figure 4. Parallel Mode Timing**

## DC Characteristics

**Table 9. High-Speed Data Inputs (A,  $\bar{A}$ ) — Differential CML**

| Symbol     | Parameter                                | Minimum | Typical | Maximum        | Unit     | Condition                           |
|------------|------------------------------------------|---------|---------|----------------|----------|-------------------------------------|
| $V_{A-DE}$ | Voltage input swing (differential drive) | 100     |         | 2400           | mVp-p    | Differential peak-to-peak.          |
| $V_{ICM}$  | Input common-mode voltage                | 1.0     | 2       | $V_{CC} - 0.3$ | V        |                                     |
| $R_{IN-A}$ | Input resistance                         | 80      | 100     | 120            | $\Omega$ | Between true and complement inputs. |

**Table 10. High-Speed Data Outputs (Y,  $\bar{Y}$ ) — Differential CML**

| Symbol       | Parameter                                            | Minimum | Typical | Maximum | Unit     | Condition                                                                                                         |
|--------------|------------------------------------------------------|---------|---------|---------|----------|-------------------------------------------------------------------------------------------------------------------|
| $V_{OUT-LD}$ | Serial data output voltage swing:<br>Low Drive mode  | 505     | 650     | 850     | mVp-p    | Peak-to-peak differential amplitude between true and complement outputs terminated with 50 $\Omega$ to $V_{CC}$ . |
| $V_{OUT-HD}$ | Serial data output voltage swing:<br>High Drive mode | 1000    | 1300    | 1700    | mVp-p    | Peak-to-peak differential amplitude between true and complement outputs terminated with 50 $\Omega$ to $V_{CC}$ . |
| $R_{OUT-Y}$  | Back-terminated output resistance                    | 40      | 50      | 60      | $\Omega$ | See Figure 5 on page 20.                                                                                          |

**Table 11. LVTTTL/CMOS Inputs**

| Symbol   | Parameter          | Minimum | Maximum         | Unit          | Condition                             |
|----------|--------------------|---------|-----------------|---------------|---------------------------------------|
| $V_{IH}$ | Input HIGH voltage | 1.7     | $V_{DD0} + 1.0$ | V             | $V_{DD0} = 2.5\text{ V}/3.3\text{ V}$ |
| $V_{IL}$ | Input LOW voltage  | 0       | 0.8             | V             | $V_{DD0} = 2.5\text{ V}/3.3\text{ V}$ |
| $I_{IH}$ | Input HIGH current |         | 100             | $\mu\text{A}$ |                                       |
| $I_{IL}$ | Input LOW current  | -100    |                 | $\mu\text{A}$ |                                       |

**Table 12. LVTTTL/CMOS Outputs**

| Symbol   | Parameter           | Minimum         | Maximum   | Unit | Condition                   |
|----------|---------------------|-----------------|-----------|------|-----------------------------|
| $V_{OH}$ | Output HIGH voltage | $V_{DD0} - 0.2$ | $V_{DD0}$ | V    | DC load < 500 $\mu\text{A}$ |
| $V_{OL}$ | Output LOW voltage  | 0               | 0.2       | V    | DC load < 2 mA              |

**Table 13. Power Supply Requirements**

| Symbol                | Parameter                                                | Minimum | Typical    | Maximum | Unit | Condition     |
|-----------------------|----------------------------------------------------------|---------|------------|---------|------|---------------|
| V <sub>CC</sub>       | Power supply voltage <sup>(1)</sup>                      | 2.375   | 2.5        | 2.625   | V    | ±5% tolerance |
| V <sub>DD0</sub>      | Power supply voltage, programming port <sup>(1, 2)</sup> |         | 2.5 or 3.3 |         | V    |               |
| P <sub>D-LDPRBS</sub> | Total power dissipation:<br>Nominal drive mode with PRBS |         |            | 2.7     | W    |               |
| P <sub>D-HDPRBS</sub> | Total power dissipation:<br>High drive mode with PRBS    |         |            | 3.3     | W    |               |
| P <sub>D-LD</sub>     | Total power dissipation:<br>Nominal drive mode           |         |            | 2.1     | W    |               |
| P <sub>D-HD</sub>     | Total power dissipation:<br>High drive mode              |         |            | 2.65    | W    |               |

1. All timing specifications and diagrams reflect 3.3 V.
2. Must track V<sub>CC</sub> when V<sub>DD0</sub> = 2.5 V.

## I/O Equivalent Circuits

### Input Termination

Termination resistor pairs are isolated between each input to minimize crosstalk. The termination will self-bias to 2.0 V (nominal) for AC-coupled applications.

All input data must be differential and nominally biased to 2.0 V relative to V<sub>EE</sub> or AC-coupled. Internal terminations are provided with nominally 50  $\Omega$  from the true and complement inputs to a common bias point.

### Output Termination

The high-speed outputs of the VSC3108 are current sinks, internally back-terminated by 50  $\Omega$  pull-up resistors to the positive supply rail. Typical DC terminations are 50  $\Omega$  pull-ups to the positive supply rail, 50  $\Omega$  terminations to 2.0 V, and 100  $\Omega$  from true to complement.

Data outputs are provided through differential current switches with on-chip 50  $\Omega$  back-termination. Two drive levels are provided to facilitate power and noise margin optimization on a per-output basis.

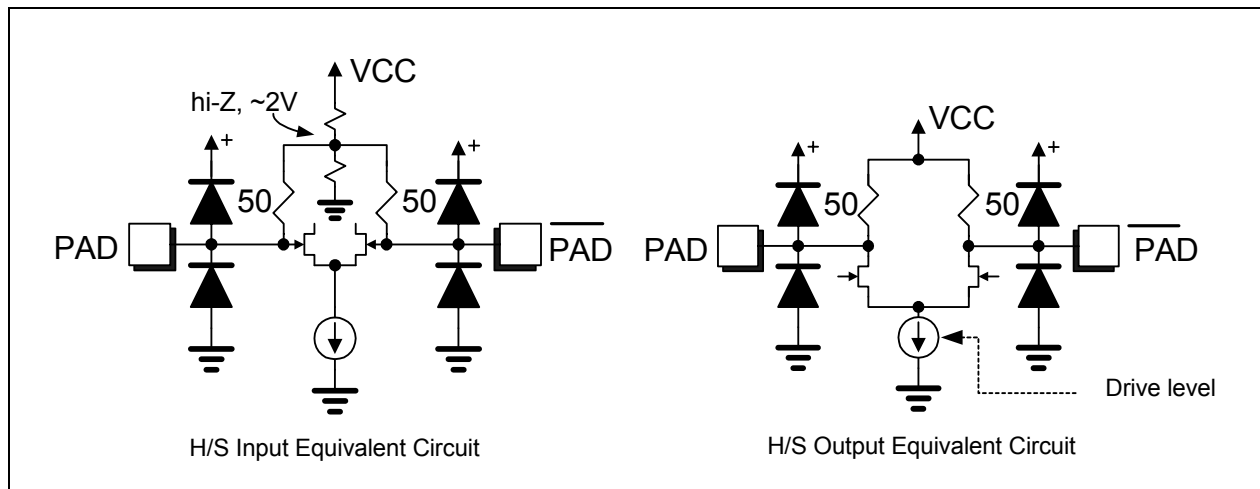


Figure 5. Input and Output Equivalent Circuits

## PRBS Clock Input

The PRBS Clock Input must have a common-mode bias of no less than 2.2 V in order to maintain specified sensitivity. Direct coupling a high-speed switch output to the PRBS Clock Input will meet this requirement, as will any CML driver with less than 600 mV peak-to-peak swing. In cases where the common-mode bias cannot be controlled, AC-coupling is recommended, using the diagram shown in [Figure 6](#).

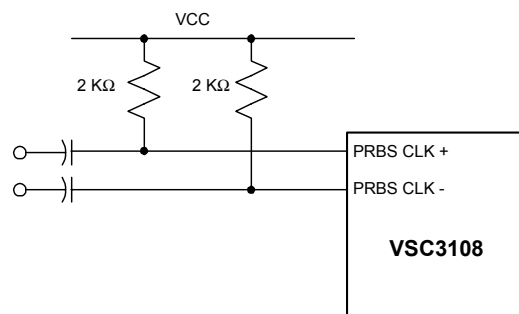


Figure 6. AC-Coupling for the PRBS Clock Input

## Package Information

The VSC3108 device is available in several packages. VSC3108VP and VSC3108VP-01 have a 69-pin ceramic ball grid array (CBGA) with an 8 mm × 8 mm body size and a 0.8 mm pin pitch. VSC3108SX and VSC3108SX-01 have a 69-pin CBGA with a 10 mm × 10 mm body size and a 1.0 mm pin pitch. VSC3108 is also available in lead(Pb)-free packages designated as VSC3108XVP, VSC3108XVP-01, VSC3108XSX, and VSC3108XSX-01.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides package information including the pin diagram and pin descriptions, package drawings, thermal specifications, and moisture sensitivity information.

## Pin Diagram

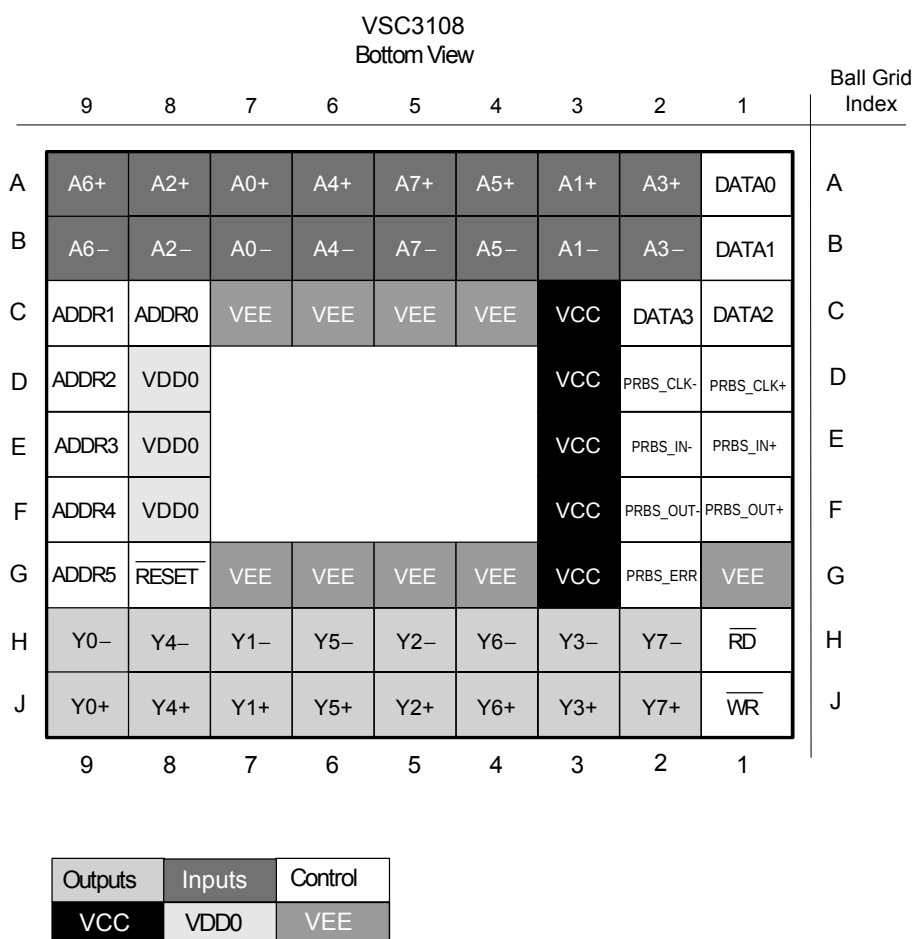


Figure 7. Pin Diagram

## Pinout Information

Table 14. Ball Identifications

| Signal                         | Pin Number | I/O | Level | Description                       |
|--------------------------------|------------|-----|-------|-----------------------------------|
| <b>High-Speed Data Inputs</b>  |            |     |       |                                   |
| A0–                            | B7         | I   | CML   | Data input channel 0; complement  |
| A0+                            | A7         | I   | CML   | Data input channel 0; true        |
| A1–                            | B3         | I   | CML   | Data input channel 1; complement  |
| A1+                            | A3         | I   | CML   | Data input channel 1; true        |
| A2–                            | B8         | I   | CML   | Data input channel 2; complement  |
| A2+                            | A8         | I   | CML   | Data input channel 2; true        |
| A3–                            | B2         | I   | CML   | Data input channel 3; complement  |
| A3+                            | A2         | I   | CML   | Data input channel 3; true        |
| A4–                            | B6         | I   | CML   | Data input channel 4; complement  |
| A4+                            | A6         | I   | CML   | Data input channel 4; true        |
| A5–                            | B4         | I   | CML   | Data input channel 5; complement  |
| A5+                            | A4         | I   | CML   | Data input channel 5; true        |
| A6–                            | B9         | I   | CML   | Data input channel 6; complement  |
| A6+                            | A9         | I   | CML   | Data input channel 6; true        |
| A7–                            | B5         | I   | CML   | Data input channel 7; complement  |
| A7+                            | A5         | I   | CML   | Data input channel 7; true        |
| <b>High-Speed Data Outputs</b> |            |     |       |                                   |
| Y0–                            | H9         | O   | CML   | Data output channel 0; complement |
| Y0+                            | J9         | O   | CML   | Data output channel 0; true       |
| Y1–                            | H7         | O   | CML   | Data output channel 1; complement |
| Y1+                            | J7         | O   | CML   | Data output channel 1; true       |
| Y2–                            | H5         | O   | CML   | Data output channel 2; complement |
| Y2+                            | J5         | O   | CML   | Data output channel 2; true       |
| Y3–                            | H3         | O   | CML   | Data output channel 3; complement |
| Y3+                            | J3         | O   | CML   | Data output channel 3; true       |
| Y4–                            | H8         | O   | CML   | Data output channel 4; complement |
| Y4+                            | J8         | O   | CML   | Data output channel 4; true       |
| Y5–                            | H6         | O   | CML   | Data output channel 5; complement |
| Y5+                            | J6         | O   | CML   | Data output channel 5; true       |
| Y6–                            | H4         | O   | CML   | Data output channel 6; complement |
| Y6+                            | J4         | O   | CML   | Data output channel 6; true       |
| Y7–                            | H2         | O   | CML   | Data output channel 7; complement |
| Y7+                            | J2         | O   | CML   | Data output channel 7; true       |
| <b>Control Pins</b>            |            |     |       |                                   |
| ADDR0                          | C8         | I   | LVTTL | Address/data bus bit 0            |
| ADDR1                          | C9         | I   | LVTTL | Address/data bus bit 1            |

Table 14. Ball Identifications (*continued*)

| Signal                    | Pin Number | I/O | Level | Description                                     |
|---------------------------|------------|-----|-------|-------------------------------------------------|
| ADDR2                     | D9         | I   | LVTTL | Address/data bus bit 2                          |
| ADDR3                     | E9         | I   | LVTTL | Address/data bus bit 3                          |
| ADDR4                     | F9         | I   | LVTTL | Address/data bus bit 4                          |
| ADDR5                     | G9         | I   | LVTTL | Address/data bus bit 5                          |
| DATA0                     | A1         | I/O | LVTTL | Address/data bus bit 0                          |
| DATA1                     | B1         | I/O | LVTTL | Address/data bus bit 1                          |
| DATA2                     | C1         | I/O | LVTTL | Address/data bus bit 2                          |
| DATA3                     | C2         | I/O | LVTTL | Address/data bus bit 3                          |
| PRBS_CLK <sup>+</sup> (1) | D1         | I   | CML   | PRBS external clock input; true                 |
| PRBS_CLK <sup>-</sup> (1) | D2         | I   | CML   | PRBS external clock input; complement           |
| PRBS_ERR                  | G2         | O   | LVTTL | PRBS error detect                               |
| PRBS_IN+                  | E1         | I   | CML   | PRBS detector input; true                       |
| PRBS_IN-                  | E2         | I   | CML   | PRBS detector input; complement                 |
| PRBS_OUT+                 | F1         | O   | CML   | PRBS generator output; true                     |
| PRBS_OUT-                 | F2         | O   | CML   | PRBS generator output; complement               |
| $\overline{WR}$           | J1         |     |       | Write enable, active low.                       |
| $\overline{RD}$           | H1         | I   | LVTTL | Read enable, active low.                        |
| $\overline{RESET}$        | G8         | I   | LVTTL | Address/data multiplexed bus reset, active low. |

1. See Figure 6 on page 20 for special bias requirements.

Table 15. Power Supplies

| Signal | Pin Number                         | Description                                                    |
|--------|------------------------------------|----------------------------------------------------------------|
| VCC    | C3, D3, E3, F3, G3                 | Positive power supply, 2.5 V                                   |
| VDD0   | D8, E8, F8                         | Positive power supply for control port, V <sub>CC</sub> /3.3 V |
| VEE    | C4, C5, C6, C7, G1, G4, G5, G6, G7 | Ground                                                         |

## Package Drawings

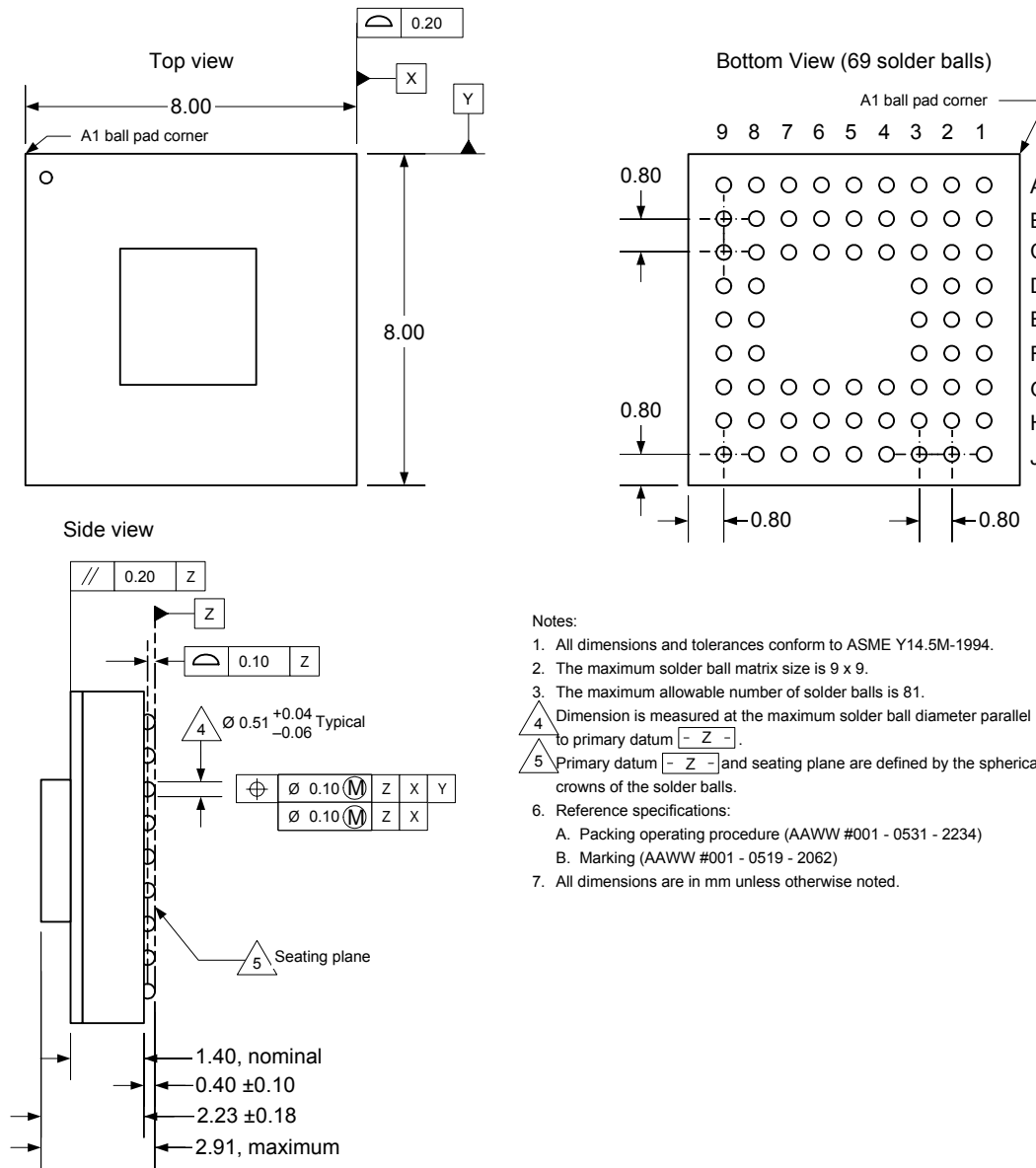


Figure 8. Package Drawing for 69-Pin CBGA (VP and XVP)

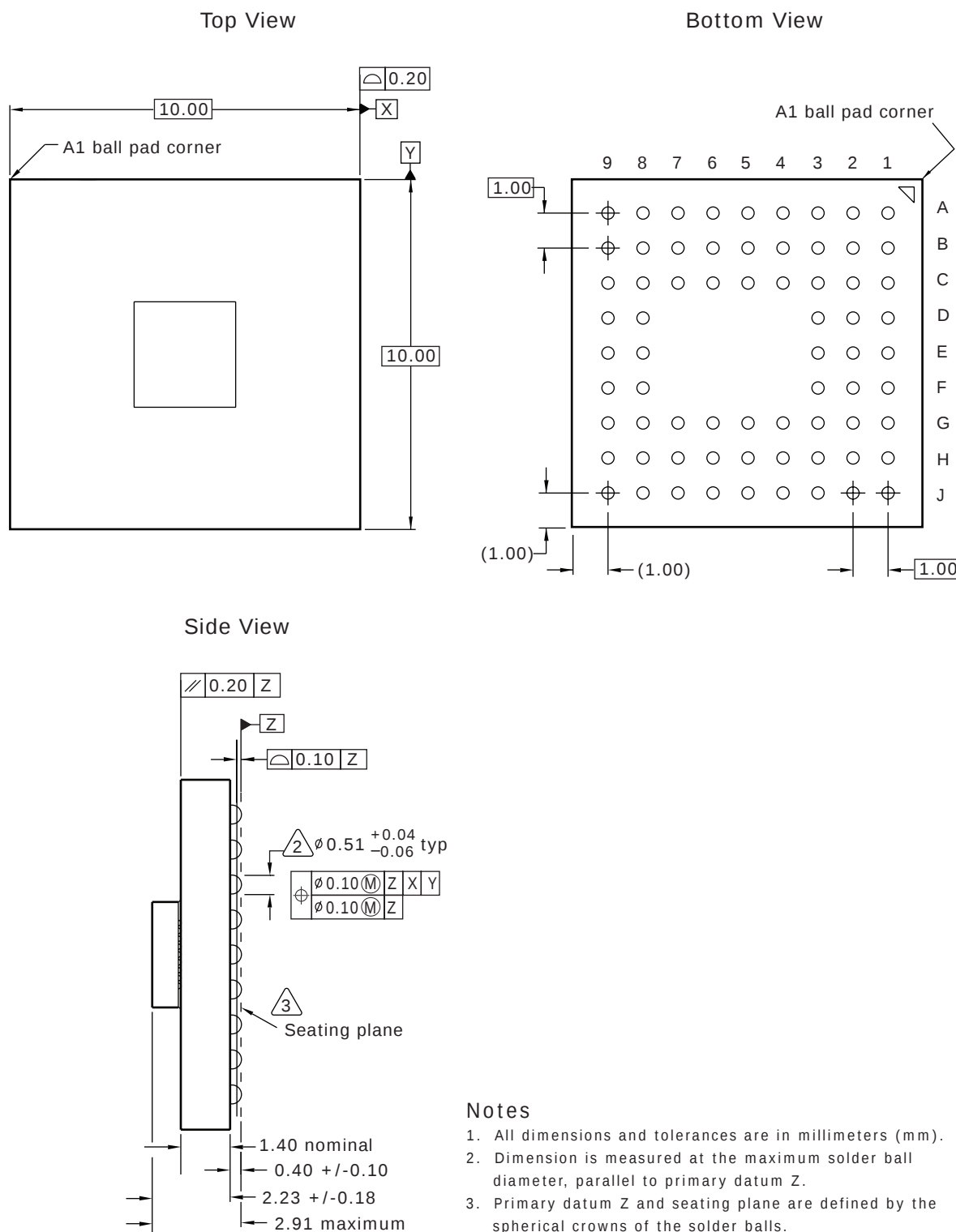


Figure 9. Package Drawing for 69-Pin CBGA (SX and XSX)

## Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

**Table 16. Thermal Resistances**

| Part Number                 | $\theta_{JC}$ | $\theta_{JA}$ (°C/W) vs. Airflow (ft/min) |     |     |
|-----------------------------|---------------|-------------------------------------------|-----|-----|
|                             |               | 0                                         | 100 | 200 |
| VSC3108VP<br>VSC3108VP-01   | 0.5           | 32                                        | 29  | 27  |
| VSC3108XVP<br>VSC3108XVP-01 | 0.5           | 32                                        | 29  | 27  |
| VSC3108SX<br>VSC3108SX-01   | 0.5           | 32                                        | 29  | 27  |
| VSC3108XSX<br>VSC3108XSX-01 | 0.5           | 32                                        | 29  | 27  |

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

## Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

## Ordering Information

The VSC3108 device is available in several packages. VSC3108VP and VSC3108VP-01 have a 69-pin ceramic ball grid array (CBGA) with an 8 mm × 8 mm body size and a 0.8 mm pin pitch. VSC3108SX and VSC3108SX-01 have a 69-pin CBGA with a 10 mm × 10 mm body size and a 1.0 mm pin pitch. VSC3108 is also available in lead(Pb)-free packages designated as VSC3108XVP, VSC3108XVP-01, VSC3108XSX, and VSC3108XSX-01.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

### VSC3108 6.5 Gbps 8x8 Asynchronous Crosspoint Switch

| Part Number                 | Description                                                          |
|-----------------------------|----------------------------------------------------------------------|
| VSC3108VP<br>VSC3108VP-01   | 69-pin CBGA, 8 mm x 8 mm body size, 0.8 mm pin pitch                 |
| VSC3108XVP<br>VSC3108XVP-01 | Lead(Pb)-free 69-pin CBGA, 8 mm x 8 mm body size, 0.8 mm pin pitch   |
| VSC3108SX<br>VSC3108SX-01   | 69-pin CBGA, 10 mm x 10 mm body size, 1.0 mm pin pitch               |
| VSC3108XSX<br>VSC3108XSX-01 | Lead(Pb)-free 69-pin CBGA, 10 mm x 10 mm body size, 1.0 mm pin pitch |

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