



ICs for Communications

Smart Integrated Digital Echo Canceller
SIDE C

PEB 20954 Version 1.1

Preliminary Product Overview Apr.1999

PEB 20954		
Revision History:		Current Version: Apr.1999, Version 1.1
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
7	7	power dissipation is 700-900 mW instead of 1200 mW
7,74	7,76	temperature range -40°C - 85°C instead of 0°C - 70°C
-	10	section about SIDEC in VoIP added
58,60	60,62	µP max. timing changed from 20 ns to 25 ns
68,69	70,71	Fig. 37 and Fig. 38 interchanged (Now Fig 38 and Fig.39)
75	77,78	AC Characteristics added
76	78	Capacitances added

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1 Introduction

The **S**mart **I**ntegrated **D**igital **E**cho **C**anceller (SIDECE) suppresses echoes in telecommunication networks which might disturb any kind of terrestrial or wireless communication. It incorporates leading edge CMOS technology as well as SIEMENS' many years' experience in Telecommunication ICs.

In communication links reflections resulting in an electrical echo are due to hybrid splits or imperfect terminations in subscriber loops. Acoustical echoes may occur due to poor isolation of microphone and speaker of some telephone system. These electrical and acoustical echoes disturb the quality of the transmission. To ensure high quality, pure data transmission the ITU-T (International Telecommunications Union, Telecommunication Standardization Sector) suggests in the recommendation G.131 the use of echo cancellers. Echo cancellation is extremely desirable for data links with total round trip transmission times of more than 50 ms.

Smart Integrated Digital Echo Canceller SIDE C

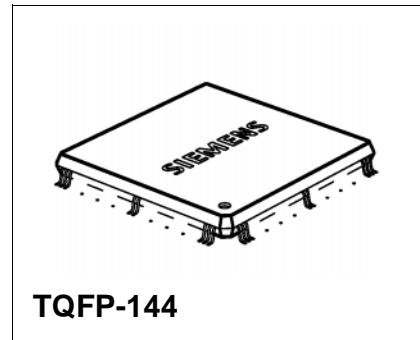
PEB 20954

Version 1.1

CMOS

1.1 Key Features

- 2.048 MHz PCM input and output interfaces with selectable μ - and A-Law coding according to ITU G.711
- Rapid convergence of patented algorithm at the beginning or during a connection even in the presence of background noise at the near end subscriber
- Echo return loss enhancement of > 30 dB (ERLE)
- Detection of double talk for adaptive convergence control
- Independently controlled voiceband echo cancelling according to ITU G.165 and G.168 for
 - 32 channels with end echo path delay of less than 63.75 ms
 - 16 channels with end echo path delay of less than 127.75 ms (usage of two SIDE C in parallel for simultaneous processing of 32 channels is easily possible)
- Smart Non Linear Processor controlled by echoloss, echo path delay and background noise
- Various options for comfort noise injection
- Maskable disabling functions
 - 2100 Hz tone with phase reversal detection
 - 2100 Hz tone without phase reversal detection
 - 2010 Hz continuity check (SS7)
 - via PCM timeslot 16 Bit a, b, c or d according to ITU G.704
 - individual channels maskable via Microprocessor Interface, UCC Interface and Serial Interface
- Integrated Universal Control and Communication Interface (UCCI) for signaling highways with direct hardware control for:
 - disable cancelling
 - configurable disabling functions
 - communication between board controllers



Type	Package
PEB 20954	TQFP-144

- Support of Channel Associated Signaling (CAS) BR transparency (robbed bits) in send path
- Selectable μ - to A-Law or A- to μ -Law Conversion on a global or per channel basis
- Configurable idle channel supervision
- Clear channel capability (64 clear) on a per channel basis
- Special evaluation of bit 8 in T1 Modem calls possible (56 clear)
- Serial 256 kbit/s interface to control the functions disable cancelling, freeze coefficients, clear channel, disable NLP, PCM Law conversion control or combinations of above
- Monitor pins for several internal states
- Switchable global loop from receive output to send input and send output to receive input
- Switchable global attenuation (2.5 dB or 6 dB) at the receive and send output
- Flexible Microprocessor Interface (SIEMENS/Intel or Motorola type, Mux and Demux mode) usable for:
 - configuration of parameters such as thresholds and functions on a global basis
 - Disable cancelling, freeze coefficients, clear channel, disable NLP, PCM Law conversion control (all functions individually for each channel)
 - support of background tests for disabled or idle timeslots (feeding and reading of test levels)
 - possibility to read levels, attenuations, internal states, signal values or all coefficients of a selected timeslot
 - control of the RAM Built In Self Test
- Advanced Integrated Watchdog Timer
- Supervision of the input clocks
- Various clock modes possible for 32.768 MHz and 8.192 MHz
- Boundary Scan according to IEEE 1149.1 Standard
- Power supply: 3.3 V, 5V tolerant inputs
- Typical power dissipation: 700 - 900 mW
- Plastic package TQFP 144
- Temperature range: -40°C - 85°C

1.2 Logic Symbol

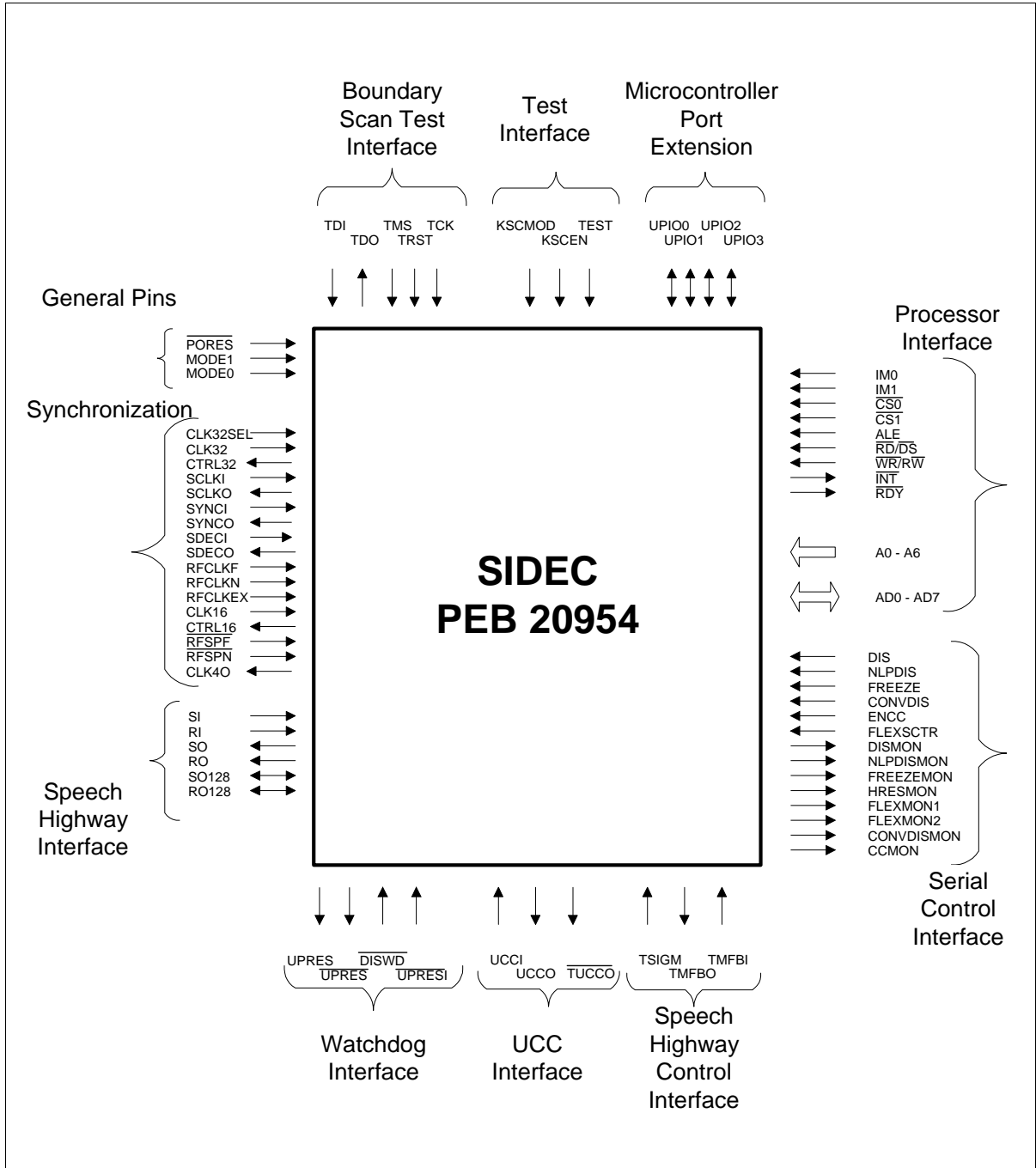


Figure 1 Logic Symbol of the SIDE PEB 20954

1.3 Typical Applications

The SIDEC can be used for various applications.

Figure 2 to Figure 5 display typical examples.

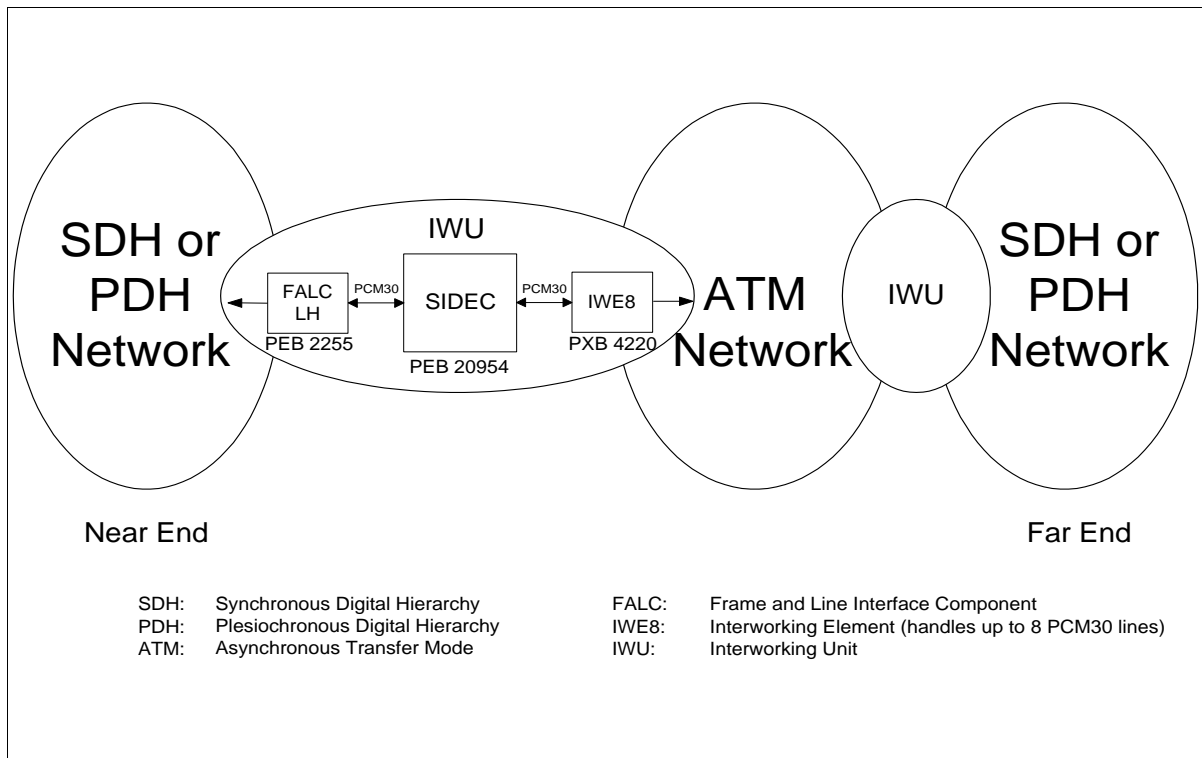


Figure 2 SIDEC in a Circuit Emulation Service Carried over ATM

In this interworking unit there are two SIEMENS products connected to the SIDEC. The FALC PEB 2255 serves as a frame and line interface component whereas the IWE8 PXB 4220 operates as an interworking element.

The delays of networks and the inter working units are usually long. In the application above the SIDEC cancels the echo that is generated by reflection on the near end side and heard by the far end speaker. The SIDEC can cancel end echo paths (SDH or PDH Network on near end side) up to 128 ms. For details see **Figure 11**.

For the set up illustrated in **Figure 2** a application note "Using SIDEC in a Voice over ATM Application" is available.

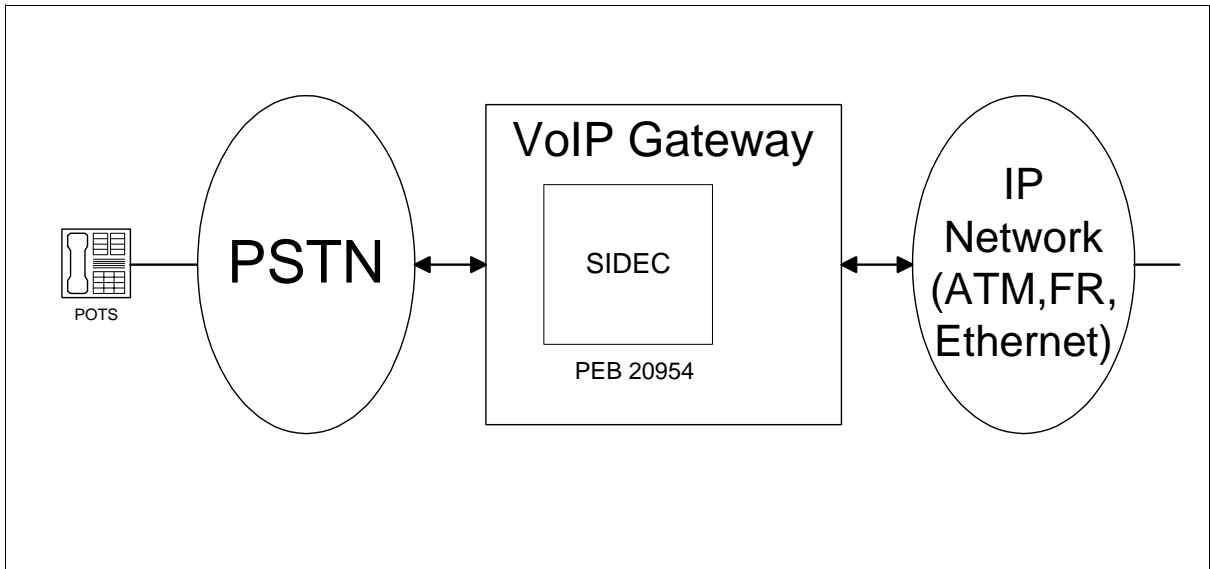


Figure 3 **SIDEC in a Voice over IP Gateway**

An emerging market in the telecom industry is “Voice Over IP”. Due to the long delay echo cancellation is required. The delay is introduced through packetizing and voice compression. The SIDEC handles different functions in a Voice over IP gateway, such as Voice Detection, Voice Activity Detection, Comfort Noise and A-law u-law conversion regarding G.711.

In a gateway the SIDEC points into the PSTN network as shown in **Figure 3**. The echo itself is generated by the hybrid in the PSTN cloud. Before the voice signal from the POTS gets packetized into ATM, FR or Ethernet cells the echo is being cancelled by the SIDEC.

For a high voice quality in “Voice Over IP” environment echo cancellation is a major requirement.

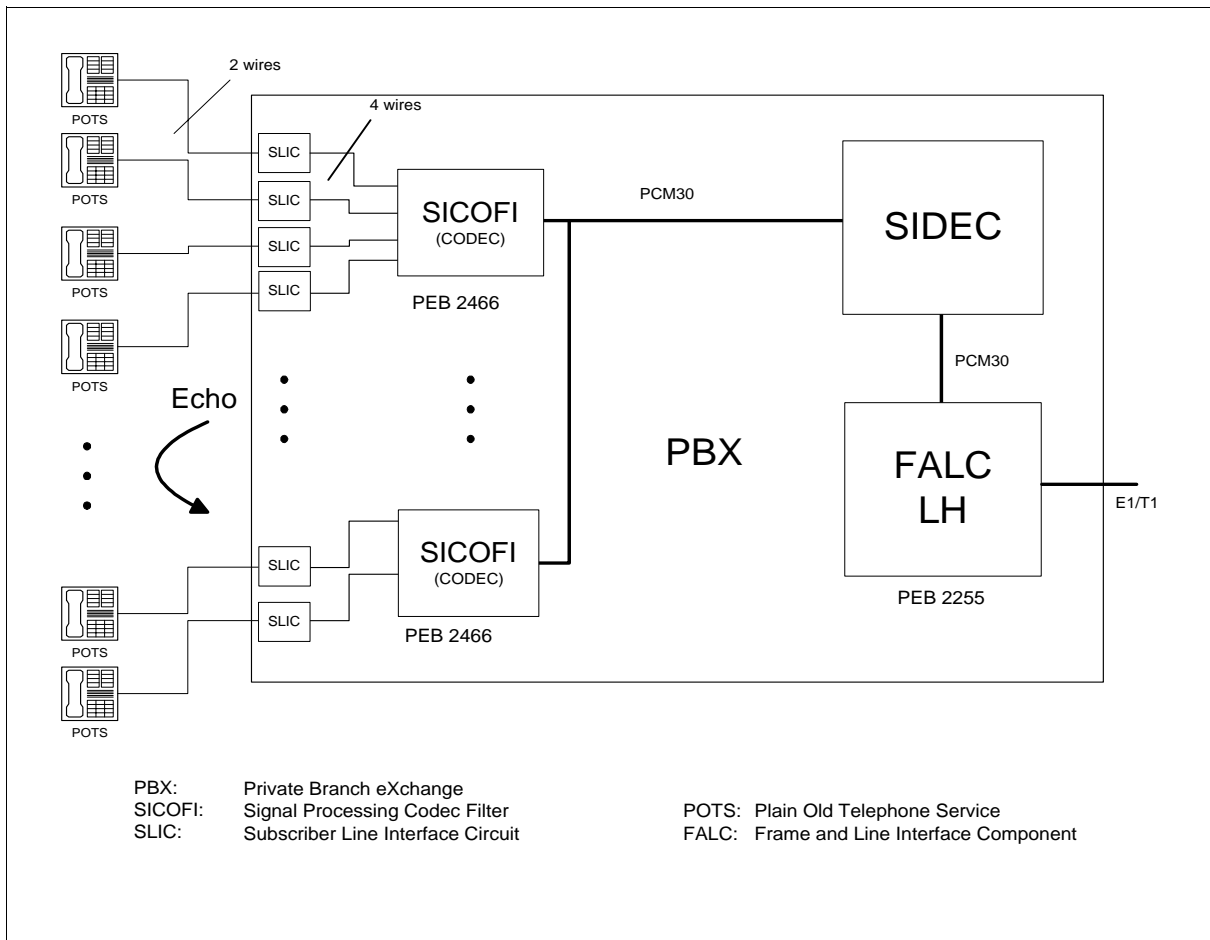


Figure 4 SIDEC in a Private Branch Exchange (PBX)

SIDEC can be used in a PBX or Central Office (CO) to cancel the echo next to the customer side (near end echo). The echo delay is kept short. The delay for this application is usually less than 64ms and the SIDEC can cancel up to 32 channels.

Figure 4 shows a PBX with a T1/E1 interface FALC LH to the CO on the one side. On the other side analog phones are connected.

A possible SIEMENS solution with the SICOFI (includes D/A and A/D conversion) and the SLIC (hybrid) to connect the analog phone is shown above.

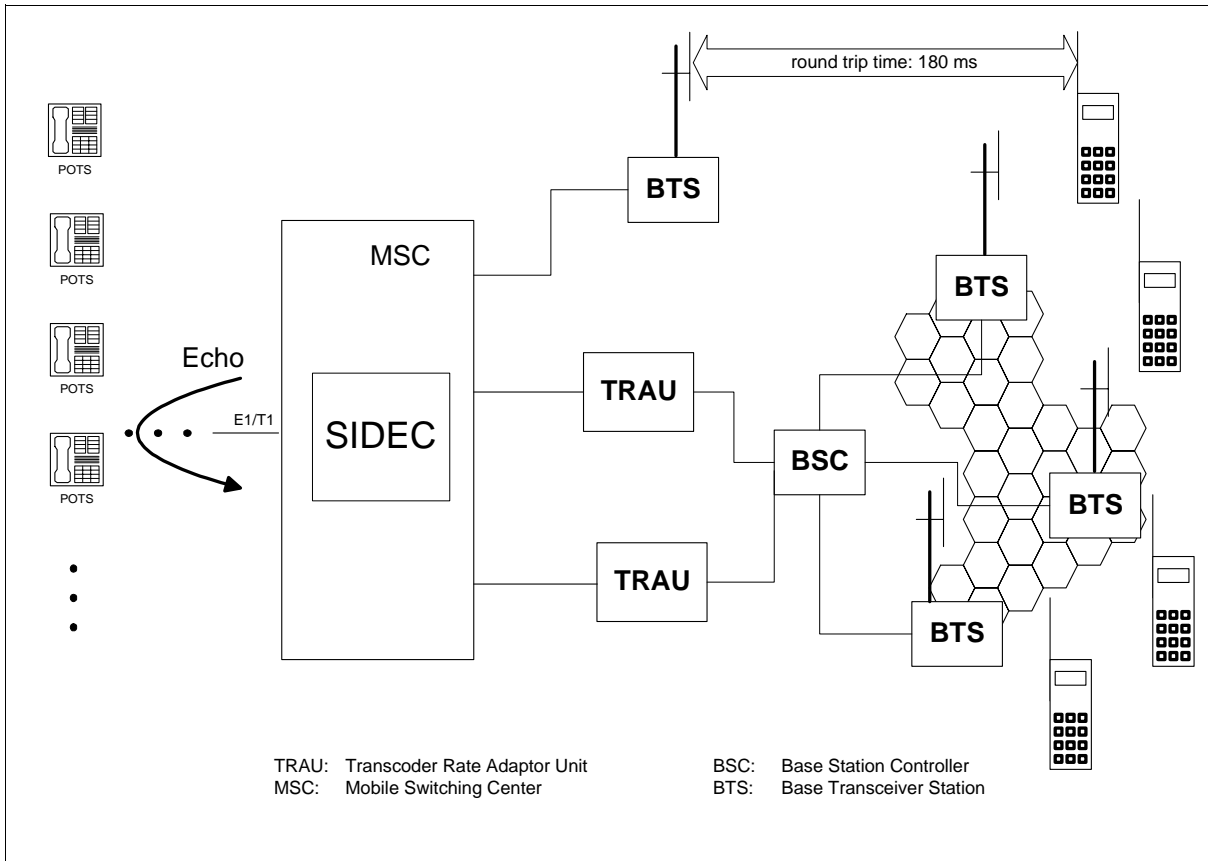


Figure 5 SIDEC in a Wireless System

Due to voice compression and error correction the one way transmission time for wireless voice signals is typically 90 ms. With 180 ms roundtrip time the 50 ms roundtrip time for echo free transmission is exceeded by at least 130 ms. Hence, the speaker on the mobile phone will hear any kind of echo generated in the hybrid next to the POTS or the acoustical echo of the POTS. The SIDEC suppresses those two kinds of echoes if it is incorporated in the MSC. Depending on the individual call the end echo path can differ dramatically. In Europe the end echo path could even go to different countries causing strong dispersion of the echo. Only a high quality echo canceller with long end path delay options guarantees compensation of the strongly varying echoes.

2 Pin Descriptions

2.1 Pin Diagram

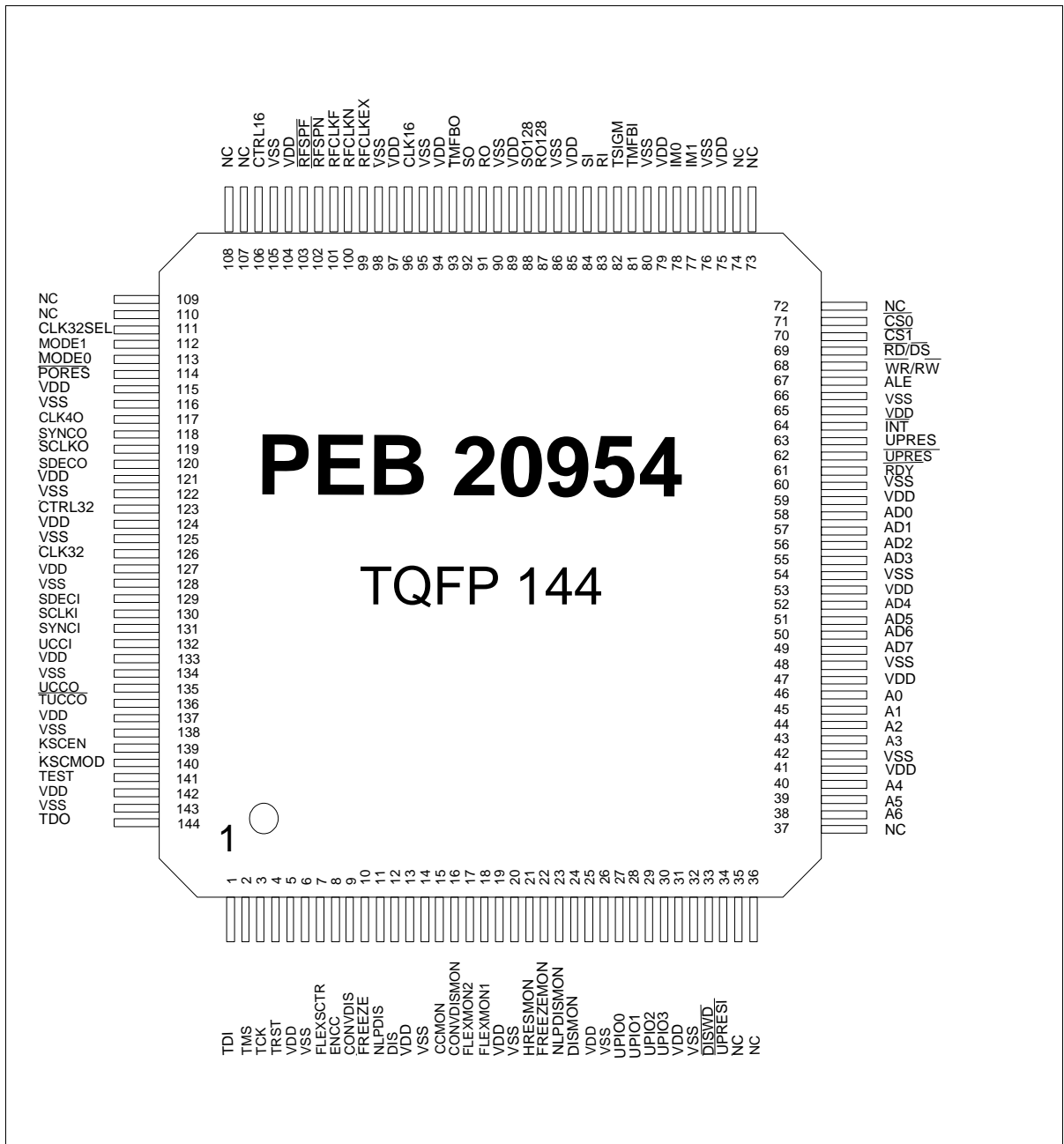


Figure 6 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 General Pins

Pin No.	Symbol	Input (I) Output (O) Pull Up / Pull Down	Function			
114	PORES	I, PU	Power On Reset. A low on this pin forces all registers and counters to predefined values			
112	MODE1	I, PU	1	End delay < 64ms	1	For future use
113	MODE0	I, PU	1		0	
112	MODE1	I, PU	0	End delay < 128 ms Master Mode	0	End delay < 128 ms Slave Mode
113	MODE0	I, PU	1		0	

Table 2 Synchronization

Pin No.	Symbol	I/O, PU/PD	Function
111	CLK32SEL	I, PU	Selects from which source SCLKO will be derived: '1': SCLKO will be derived from CLK32 by dividing by 4 '0': SCLKO will be derived from CLK16 by dividing by 2
126	CLK32	I, PU	32.768 MHz Operating Clock for the SIDEC
123	CTRL32	O	Control voltage for the 32.768 MHz operating Clock VCO, maskable for reduced power consumption
130	SCLKI	I, PU	System clock input (8.192 MHz) for PCM- and UCCI
119	SCLKO	O	8.192 MHz system clock output, source CLK32 or CLK16 is selectable via pin CLK32SEL, maskable for reduced power consumption
117	CLK40	O	4.096 MHz system clock output for subsequent circuits, derived from SCLKI, maskable for reduced power consumption

Pin Descriptions

Pin No.	Symbol	I/O, PU/PD	Function
131	SYNCI	I, PU	System Synchronization input pulse. Defines the frame alignment of PCM and UCCI signals in conjunction with the values in registers RIALIGN, SIALIGN, SOALIGN, UCCALIGN, PHALIGN and also the multiframe alignment of the UCCI. Must be integer multiple of 125 μ s if UCC Interface is not used. Must be multiple integer of 4 ms if UCC interface is used. Leave open if not used or connect to V_{DD}
118	SYNCO	O	System Synchronization output pulse (see SYNCI), duration configurable one or two SCLKO periods, period 125 μ s. If the UCC interface is not used and no SYNCI is applied, SYNCO can take over the part and role of SYNCI.
120	SDECO	O	Synchronization output pulse for other SIDECS if this SIDECS uses its own 32.768 MHz VCO. Can also be used for synchronization of external devices to the serial control input and monitor output signals of the SIDECS. The pulse width is 488 ns with a period of 125 μ s.
129	SDECI	I, PU	Synchronization input pulse if the SIDECS uses the 32.768 MHz VCO of another SIDECS. The same SCLKI signal can be applied to SDECI and SCLKI pin if the SCLKI is supplied by a source with correct phase condition to the CLK32 (see Figure 14). If the pin is not used leave it open or connect it to V_{DD} .
101	RFCLKF	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPV[6:5]="00"
100	RFCLKN	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPV[6:5]="01"

Pin Descriptions

Pin No.	Symbol	I/O, PU/PD	Function
99	RFCLKEX	I, PU	Reference clock (2.048 MHz) for frequency comparison to generate the control voltage for the 16.384 MHz VCXO if Register FSLIPIV[6]='1'
96	CLK16	I, PU	Clock from 16.384 MHz VCXO
106	CTRL16	O	Control voltage for the 16.384 MHz VCXO
103	$\overline{\text{RFSPF}}$	I, PU	Receive Frame Sync Pulse from the far end side (F1). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '0'.
102	$\overline{\text{RFSPN}}$	I, PU	Receive Frame Sync Pulse from the near end side (F2). This pulse of 488 ns width marks timeslot 0 when writing into Elastic Store (e.g. FALC) to prevent faults in one frame length mode. To use this pin Register FSLIPIV[5] must be '1'.

Table 3 Microprocessor Interface

Pin No.	Symbol	I/O, PU/PD	Function
78	IM0	I, PU	Interface Mode SIEMENS/Intel = low, Motorola = high
77	IM1	I, PU	Interface Mode MUXED = low, DEMUXED = high
71	$\overline{CS0}$	I, PU	Chip Select. A low signal selects the SIDEDEC (internally "anded" with $\overline{CS1}$).
70	$\overline{CS1}$	I, PU	Chip Select. A low signal selects the SIDEDEC (internally "anded" with $\overline{CS0}$).
46-43 40-38	A0..A6	I, PU	Address Bus. Only used in demuxed mode, can be left open in muxed mode.
58-55 52-49	AD0..AD7	I/O, -	Multiplexed Address/Data Bus in multiplexed mode, Data Bus in demultiplexed mode
67	ALE	I, PU	Address Latch Enable in multiplexed mode. Address on AD bus is internally latched with the falling edge of ALE. This signal is also used for the internal clock supervision. In Demuxed mode there must be provided an external independent clock signal (i.e. processor clock) in order to enable proper clock supervision.
69	$\overline{RD/DS}$	I, PU	SIEMENS/Intel mode. A low indicates a read operation. Motorola mode. Data Strobe, active low to control read/write
68	$\overline{WR/RW}$	I, PU	SIEMENS/Intel mode. A low indicates a write operation. Motorola mode. High = read cycle, low = write cycle
64	\overline{INT}	O, (od)	Interrupt request from the SIDEDEC, active low
61	\overline{RDY}	O, (od)	Ready signal for μC devices that support this feature. For read cycles the signal is asserted after the data on the AD bus is valid. For writing cycles the signal is asserted when a write access is ready to be concluded.

Table 4 Microcontroller Port Extension

Pin No.	Symbol	I/O, PU/PD	Function
27	UPIO0	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
28	UPIO1	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
29	UPIO2	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO
30	UPIO3	I/O, PU	Pin that can be read and controlled by the on board processor via register UPIO

Table 5 Processor Watchdog Circuit

Pin No.	Symbol	I/O, PU/PD	Function
63	UPRES	O	μ P-Reset. High pulse (125 μ s) if the μ P fails to write predefined values to the registers WDG1 to WDG3 in this sequence within 2 s and $\overline{\text{DISWD}}='1'$. Also active if $\overline{\text{PORES}}='0'$ or $\overline{\text{UPRESI}}='0'$
62	$\overline{\text{UPRES}}$	O	Same as UPRES, but low active
33	$\overline{\text{DISWD}}$	I, PU	Disable of μ P-Reset on active watchdog condition if set to low
34	$\overline{\text{UPRESI}}$	I, PU	Produces a reset signal at UPRES, $\overline{\text{UPRES}}$ if set to low

Table 6 Speech Highways

Pin No.	Symbol	I/O, PU/PD	Function
84	SI	I, PD	2.048 Mbit/s Send speech highway input. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers SIALIGN and PHALIGN[3:2]
83	RI	I, PD	2.048 Mbit/s Receive speech highway input. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers RIALIGN and PHALIGN[1:0]

Pin Descriptions

Pin No.	Symbol	I/O, PU/PD	Function
92	SO	O	2.048 Mbit/s Send speech highway output. Start of timeslot 0, bit 7 can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers SOALIGN and PHALIGN[5:4]
91	RO	O	2.048 Mbit/s Receive speech highway output. This signal will has a fixed delay of one PCM frame (125 μ s) with respect to RI
88	SO128	I/O, PU	Auxiliary 2.048 Mbit/s Send speech highway output in 128 ms mode. Input in master mode, output in slave mode. The pins of master and slave SIDEC in 128 ms mode should be connected to enable a 32 channel system. The signal from the slave is multiplexed in the master with the internally generated signal and output (clocked) with the system clock. Tristate and meaningless in 64 ms mode
87	RO128	I/O, PU	Auxiliary 2.048 Mbit/s Receive speech highway output in 128 ms mode. Input in master mode, output in slave mode. The pins of master and slave SIDEC in 128 ms mode should be connected to enable a 32 channel system. The signal from the slave is multiplexed in the master with the internally generated signal and output (clocked) with the system clock. Tristate and meaningless in 64 ms mode

Table 7 UCC Interface

Pin No.	Symbol	I/O, PU/PD	Function
132	UCCI	I, PD	2.048 Mbit/s UCC highway input. Start of timeslot 0, bit 7 and frame number can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers UCCMFR, UCCALIGN and PHALIGN[7:6]
135	UCCO	O	2.048 Mbit/s UCC highway output. Start of timeslot 0, bit 7 and frame number can be flexibly aligned to the SYNCI/SYNCO pulse in 122 ns steps via registers UCCMFR, UCCALIGN and PHALIGN[7:6]
136	TUCCO	O	Tristate control signal for external tristate output buffer at the UCCO bus, active low. Remains inactive after a power on reset until the configuration by the μ P has been settled. Active only at UCC timeslot 0 for UCC frames that correspond to processed PCM channels

Table 8 Speech Highway Control Signals for Channel Associated Signaling (CAS) in T1 Systems

Pin No.	Symbol	I/O, PU/PD	Function
82	TSIGM	I, PD	Transmit Signaling Marker, indicating robbed bits at SI, corresponding to the delay of SI
81	TMFBI	I, PD	Transmit Multiframe Begin Input corresponding to the delay of SI
93	TMFBO	O	Transmit Multiframe Begin Output corresponding to the delay of SO. The delay of TMFBI to TMFBO is identical to the delay of SI to SO

Table 9 Channelwise Serial Interface

Pin No.	Symbol	I/O, PU/PD	Function
12	DIS	I, PD	Serial 256 kbit/s disable signal to bypass the canceller, NLP and attenuator and to reset the H-Register and Speech Control unit on a per channel basis. High active, maskable, leave open or connect to ground if unused
11	NLPDIS	I, PD	Serial 256 kbit/s signal to disable the NLP on a per channel basis. High active, maskable, leave open or connect to ground if unused
10	FREEZE	I, PD	Serial 256 kbit/s signal to freeze the H-Registers on a per channel basis. High active, maskable, leave open or connect to ground if unused
9	CONVDIS	I, PD	Serial 256 kbit/s signal to disable A/ μ -Law conversion on a per channel basis. High active, maskable, leave open or connect to ground if unused
8	ENCC	I, PD	Serial 256 kbit/s signal to enable clear channel transparency on a per channel basis. High active, maskable, leave open or connect to ground if unused, same function as DIS='1' and CONVDIS='1'
7	FLEXSCTR	I, PD	Flexible serial 256 kbit/s control signal on a per channel basis. Configurable by register CONFLEXSCTR. High active, maskable, leave open or connect to ground if unused
24	DISMON	O	Serial 256 kbit/s EC disable (signals bypass channels) monitor output signal ('0': EC on, '1': EC off)
23	NLPDISMON	O	Serial 256 kbit/s NLP disable monitor output signal ('0': NLP on, '1': NLP off)
22	FREEZEMON	O	Serial 256 kbit/s H-Register freeze monitor output signal ('1': freeze, '0': no freeze)
21	HRESMON	O	Serial 256 kbit/s H-Register reset monitor output signal ('1': reset, '0': no reset)

Pin Descriptions

Pin No.	Symbol	I/O, PU/PD	Function
18	FLEXMON1	O	Serial 256 kbit/s monitor output signal (32 channels at 8 kbit/s), monitoring according to settings of the bits CONFLEXMON[7:4], e.g. Idle channel detection, 2010 Hz tone detected, 2100 Hz tone with or without phase reversal detected, double talk detected, no speech detected
17	FLEXMON2	O	Serial 256 kbit/s monitor output signal (32 channels at 8 kbit/s), monitoring according to settings of the bits CONFLEXMON[3:0], e.g. Idle channel detection, 2010 Hz tone detected, 2100 Hz tone with or without phase reversal detected, double talk detected, no speech detected
16	CONVDISMON	O	Serial 256 kbit/s law conversion disable monitor output signal ('1': conversion disabled, '0': conversion enabled)
15	CCMON	O	Serial 256 kbit/s clear channel transparency (64 clear) monitor output signal ('1': clear channel on, '0': clear channel off), same as DISMON='1' and CONVDISMON='1'

Table 10 Test Interface for Boundary Scan according to IEEE 1149.1

Pin No.	Symbol	I/O, PU/PD	Function
1	TDI	I, PU	Test Data Input
144	TDO	O	Test Data Output
2	TMS	I, PU	Test Mode Select
3	TCK	I, PU	Test Clock
4	TRST	I, PU	Boundary Test Reset (active low, should be tied to '0' for normal operation)

Table 11 Test Interface

Pin No.	Symbol	I/O, PU/PD	Function
140	KSCMOD	I, PD	SCAN MODE ENABLE pin for enabling of scan test. For normal operation this pin should be left unconnected or connected to V_{SS} .
139	KSCEN	I, PD	SCAN SHIFT ENABLE pin for shift enabling in scan test. For normal operation this pin should be left unconnected or connected to V_{SS} .
141	TEST	I, -	Reserved for special tests (i.e. IDDQ, MBIST, etc.). For normal operation this pin must be connected to V_{SS} . Disables all pull resistances for IDDQ if set to '1'. Normal operation: '0'.

3 Functional Description

Figure 7 depicts the Functional Block Diagram of the SIDEc.

3.1 Functional Block Diagram and Description

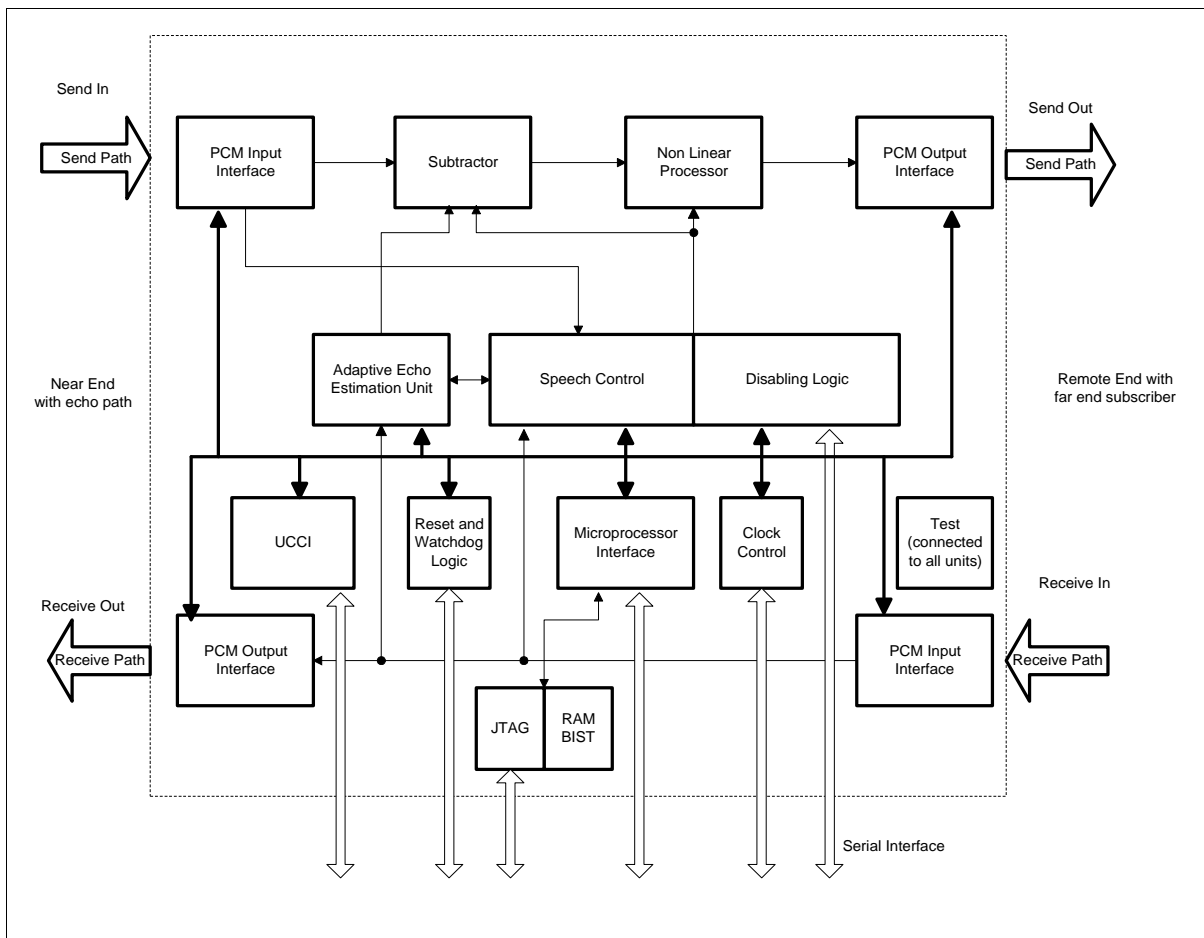


Figure 7 Block Diagram

The following paragraphs describe the functions of the SIDEc block diagramm shown in Figure 7.

3.1.1 Speech Control

The Speech Control analyzes the data from the PCM Input Interfaces and external inputs and supervises the functions of the other system components. As soon as the far end subscriber talks, the Adaptive Echo Estimation Unit is activated by the Speech Control. If the double talk condition is detected or a non speech signal with an adequate echo loss enhancement is identified by the Speech Control, the content of the Adaptive Echo Estimation Unit is frozen. Under specific circumstances a reset of the H-Register

(described in Section 3.1.3) of the Adaptive Echo Estimation Unit might be necessary. The H-Register reset signal is also provided by the Speech Control.

3.1.2 Disabling Logic

Upon request of the Speech Control and depending on external inputs the Disabling Logic disables the Non Linear Processor and/or the Subtractor or even the complete Echo Canceller.

If the Speech Control Unit detects, that one of the following conditions is applied to the Echo Canceller, it will disable the device via the Disabling Logic:

- Disabling via 2100 Hz tone without phase reversal
- Disabling via 2100 Hz tone with phase reversal
- Disabling via 2010 Hz continuity check
- Disabling via PCM timeslot 16 Bit a, b, c or d according to ITU G. 704
- Disabling via Idle channel detection.
- Disabling of individual channels via external interfaces (μ P, serial and/or UCC interface)

3.1.3 Adaptive Echo Estimation Unit

The Adaptive Echo Estimation Unit contains for each 8 bit signal sampled at 8 kHz memory for 512 / 1024 byte. This is equivalent to 64 / 128 ms end echo path delay. Depending on the end echo path delay of 64 or 128 ms the Adaptive Echo Estimation Unit processes 32 or 16 channels simultaneously, respectively. The corresponding 32 / 16 H-Register for each channel representing the pulse response of the complete echo path are also stored in the Adaptive Echo Estimation Unit. This information simplifies the detection of double speech. A highly sophisticated and patented algorithm guarantees fast and stable convergence even in the presence of near end speech.

The Adaptive Echo Estimation Unit is connected to the Microprocessor Interface in order to configure parameters of the algorithm and to read the content of the H-Register.

3.1.4 PCM Input/Output Interface

Each PCM Input/Output Interface contains a delay element, that is adjustable for max 125 μ s delay in 122 ns steps in order to align the corresponding PCM signal to the synchronizing pulse. Unless not bypassed, the delay from Receive In to Receive Out is fixed to one PCM Frame equivalent to 125 μ s. The signal Multiframe Begin is delayed accordingly to the send path delay.

Encoder to convert A- or μ -Law PCM signals to linear, and decoder to convert linear PCM signals to A- or μ -Law allow for channelwise Law Conversion (transcoding).

Functional Description

Offset adjustment is implemented at the output of the canceller. The attenuation of 0 dB, 2.5 dB or 6 dB is programmable by a register. The use of this feature requires that the cancelling function for the corresponding timeslot is enabled.

The complete bypassing of individual timeslots and connections from and to the processor interface with the internal canceller is provided for testing of cancelling timeslots.

The least significant bit in the send path can be transmitted transparently to the output if the corresponding external pin TSIGM is activated (CAS bit robbing).

The block PCM Input/Output Interface provides time multiplexing/demultiplexing for 16 or 32 timeslots. (depending on configuration, see section above). In 128 ms echo end path mode the selection of timeslots at the input is assigned as follows:

- Master: Timeslot 0,1,2,3, 8,9,10,11, 16,17,18,19, 24,25,26,27
- Slave: Timeslot 4,5,6,7, 12,13,14,15, 20,21,22,23, 28,29,30,31

The PCM Input/Output Interfaces are connected to the Speech Control Unit, Disabling Logic and the Microprocessor Interface.

3.1.5 Subtractor

The subtractor calculates the difference between the signal from the PCM Send In Interface and the artificial echo provided by the Adaptive Echo Estimation Unit. The subtractor is controlled by the Speech Control.

3.1.6 Non Linear Processor

The Non Linear Processor (NLP) limits the residual echo if only far end talk is present. Three programmable functions are available:

- Block echo and background noise.
- Replace echo and background noise by comfort noise with the level of the determined background noise.
- Clip the level of the echo and the background noise to the level of the background noise. (Experiments show that most people prefer this configuration)

The NLP is controlled by the Disabling Logic and Speech Control.

3.1.7 Microprocessor Interface

The Microprocessor Interface can operate in Intel and Motorola Mode. It provides access to the internal configuration, control states and monitor registers.

3.1.8 Universal Control and Communication Interface

The UCC Interface is a serial hardware interface for SIDEC control and supervision by other boards via a Microprocessor. A special feature of the SIDEC-UCC Interface is, that

Functional Description

certain controlling functions like the channelwise disabling or A/ μ -Law conversion can be operated directly by the hardware without intervention of the microprocessor. This feature reduces the work load of the processor dramatically.

3.1.9 Watchdog Timer

A Watchdog timer is implemented to reset the on board processor if the software gets stuck in an undefined state as a result of a faulty operation. A reset condition is met if the microprocessor fails to write predefined values to the three watchdog registers in the correct sequence within 2 s. As long as the watchdog is active the SIDEC generates interrupts and/or reset pulses of 125 μ s width with a period of 2 s.

3.1.10 Clock Control

The Clock Control supervises and generates all clock signals for proper operation of the ASIC hardware.

3.1.11 JTAG and RAM BIST

The JTAG (Joint Test Application Group) has been implemented according to IEEE 1149.1. A RAM BIST (Random Access Memory Built In Self Test) is also provided.

3.1.12 Test

The Test Unit controls the background test on disabled channels. A built in self test is used for testing internal RAMs. This test can be activated after switching on the supply voltage. The test unit also supervises the Clock Control Unit.

A notebook register allows the check of the μ P Interface.

Within the Test Unit the registers for background testing of idling channels are implemented. In this test a pattern is input in the idling channel at Receive in and Send in and evaluated at the Send out port.

During normal operation the Test Unit supervises functions such as read out of levels, internal states and coefficients.

3.2 Description of Functional Features

3.2.1 Channelwise and Global A- and μ -Law Conversion

The SIDEC allows channel individual conversion. **Figure 8** depicts the implementation of the different options for the A- to μ - or μ - to A-Law conversion. Depending on the requirements of the application two settings can be configured: Either global or channel individual law conversion.

Global A- to μ - and μ - to A-Law conversion:

Functional Description

If this modus is chosen by setting CONFLAW.CHIND='0' all 32 PCM channels are converted according to the settings of GALAWFE for the far end and GALAWNE for the near end. A '1' in GALAWFE and GALAWNE indicates that A-Law is used for the corresponding end. A '0' indicates usage of μ -Law. The conversion can be disabled channel individually by setting the CHCTRL0-31.CONVDIS = '1' via software. Law decoding/encoding is then carried out according to GCONVDISLAW. To activate the serial control signal and the UCC interface as disabling source for the PCM law conversion the bits CHCTRL0-31.ENPCTRL must be set to '0'.

Channel individual A- to μ - and μ - to A-Law conversion:

For channel individual conversion the user can configure independently for each channel whether A- to μ -, μ - to A- or no Law conversion is selected via setting IALAWNE for the near end and IALAWFE for the far end with the corresponding value for A- or μ -Law. The conversion can be disabled channel individually by setting the CHCTRL0-31.CONVDIS = '1' via software. Law decoding/encoding is then carried out according to CHCTRL0-31.CONVDISLAW. To activate the serial control signal and the UCC interface as disabling source for the PCM law conversion the bits CHCTRL0-31.ENPCTRL must be set to '0'.

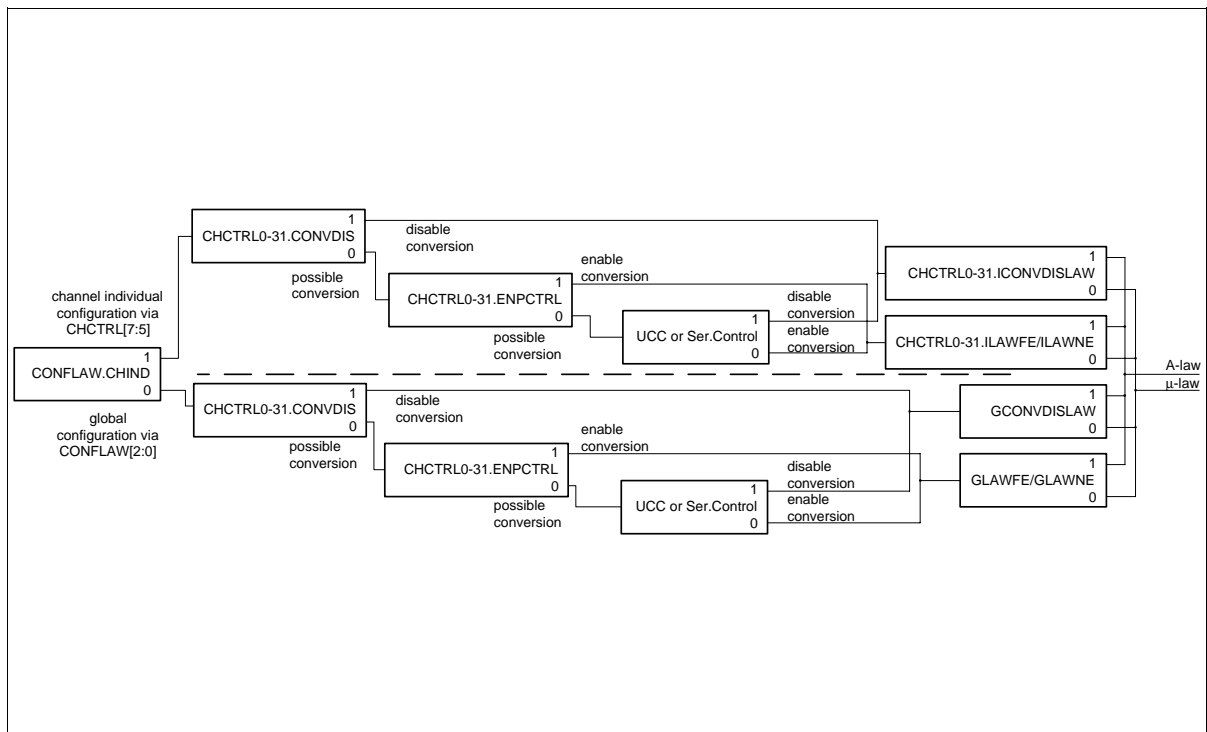


Figure 8 Explanation of Options for A- and μ -Law Conversion

3.2.2 Bypass and Disabling Functions

Figure 9 depicts the bypass and disabling functions of the SIDEC. They can be configured via UCC, Serial and μ P Interface.

Setting NLPDIS = '1' (pin or register setting) leads to bypassing of the Non Linear Processor.

Setting BYPASS = '1' (Serial control signal, UCC or 2100 Hz tone via register settings) results in bypassing the Attenuator in the Receive Path as well as in bypassing the Subtractor, the Non Linear Processor and the Attenuator in the Send Path.

Disabling a channel or the complete canceller will result in a BYPASS function, a H-Register reset and a reset of the Speech Control Unit. A bypassed or disabled channel of the SIDEC can still be converted from A/ μ - Law or vice versa.

If a Modem call is detected the user can define what action is related to the detection of a Modem call (2100 Hz with phase reversal or without reversal): bypassing, NLP bypassing, H-Register Reset or combination of the functions.

The 64 Clear mode is activated by bypassing and defining the same Law Conversion at near end and far end. In 64 Clear mode the signal is still passed through the frame alignment.

For testing purposes the canceller can be completely bypassed by setting SBYPASS and RBYPASS.

The Receive out signal can be input directly to the Send In port by setting the RSLOOP = '1'. The Send out signal can be input directly to the Receive in port by setting the SRLOOP = '1'. If both loops are configured only RSLOOP will be enabled in the SIDEC.

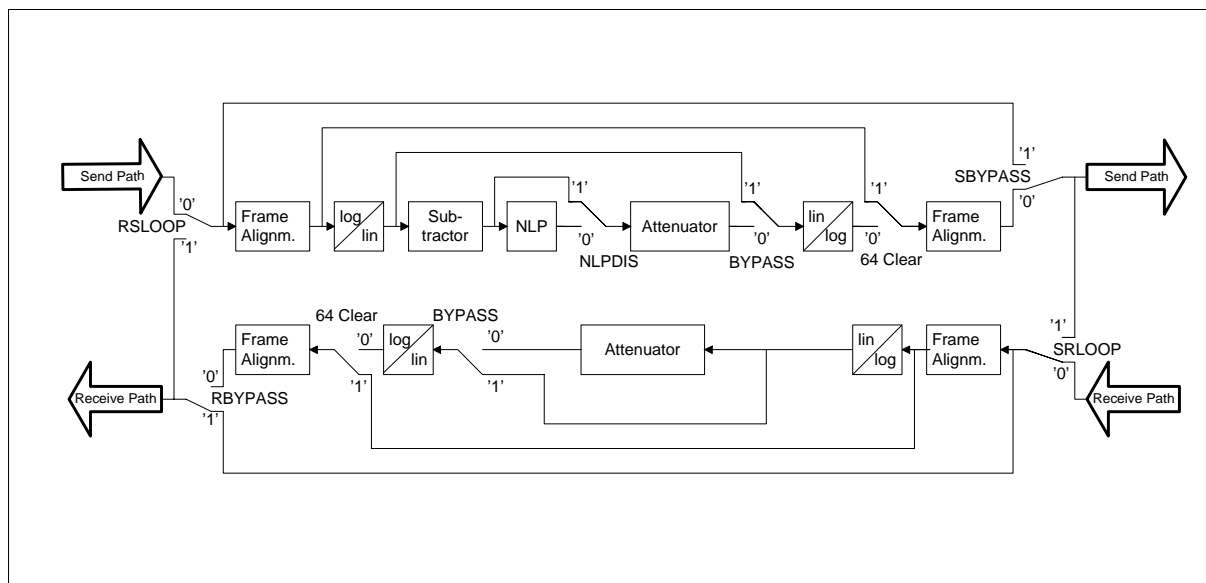


Figure 9 Bypass and Disabling Functions of the SIDEC

3.2.3 UCC Interface

The UCC Interface uses a clock frequency of 2048 kHz. The UCC Signal is structured into frames (period 125 μ s) consisting of 32 channels (period 3.9 μ s) and a multiframe consisting of 32 frames (period 4 ms). The multiframe is synchronized with the SYNCI Input pulse. The SIDEC reads and writes (tristate controlled) only the channels 0 of the frames. The 32 channels 0 of each multiframe are used to control and supervise the associated PCM channels. UCC Frame 0 corresponds to PCM channel 0, UCC Frame 1 corresponds to PCM channel 1, This relation is depicted in **Figure 10**. It is also possible to use one special UCC-Frame for a general purpose. With the registers UCCMFR, UCCALIGN and PHALIGN[7:6] the UCC channel 0 of frame 0 can be shifted to any channel and frame. Hence, up to 32 different devices can be connected in parallel to the UCC Interface.

The output signal UCCO is always in phase with the UCCI input signal.

Functional Description

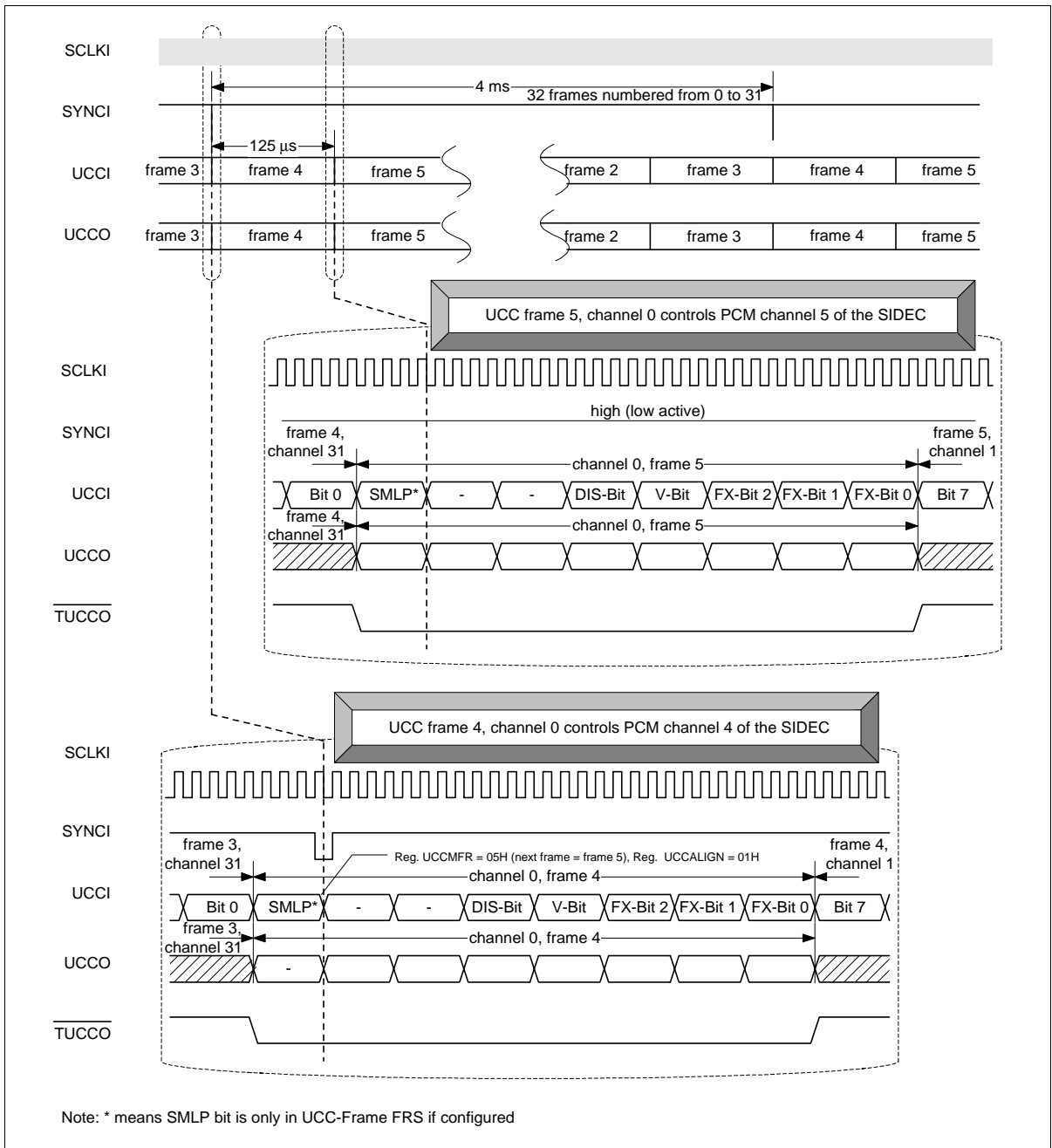


Figure 10 UCC Signal for control of PCM Signal

4 Operational Description

4.1 Pin Connection Diagram for SIDEC

Figure 11 illustrates an example for the pin connection of the SIDEC to an E1/T1 IC and to an interworking element IC.

The SIDEC is used to cancel the echo on the side of the FALC PEB 2254 or FALC-LH PEB 2255 which is the near end in this case. There are two SIEMENS products in this Inter working unit connected to the SIDEC. The FALC serves as a frame and line interface component whereas the IWE8 PEB 4220 operates as an interworking element. For multiframe alignment in the IWE8, FRMFBX must have a correct timing relation to FRDATX. For this purpose the SIDEC adjusts the delay from the TMFBI input to the TMFBO output to the delay of the SI input to the SO output. For the support of the CAS-BR transparency the SIDEC passes the robbed bits that are indicated by the FALC via the TSIGM input directly through to the SO output by overwriting the computed value of the robbed bit with the value of the SI input.

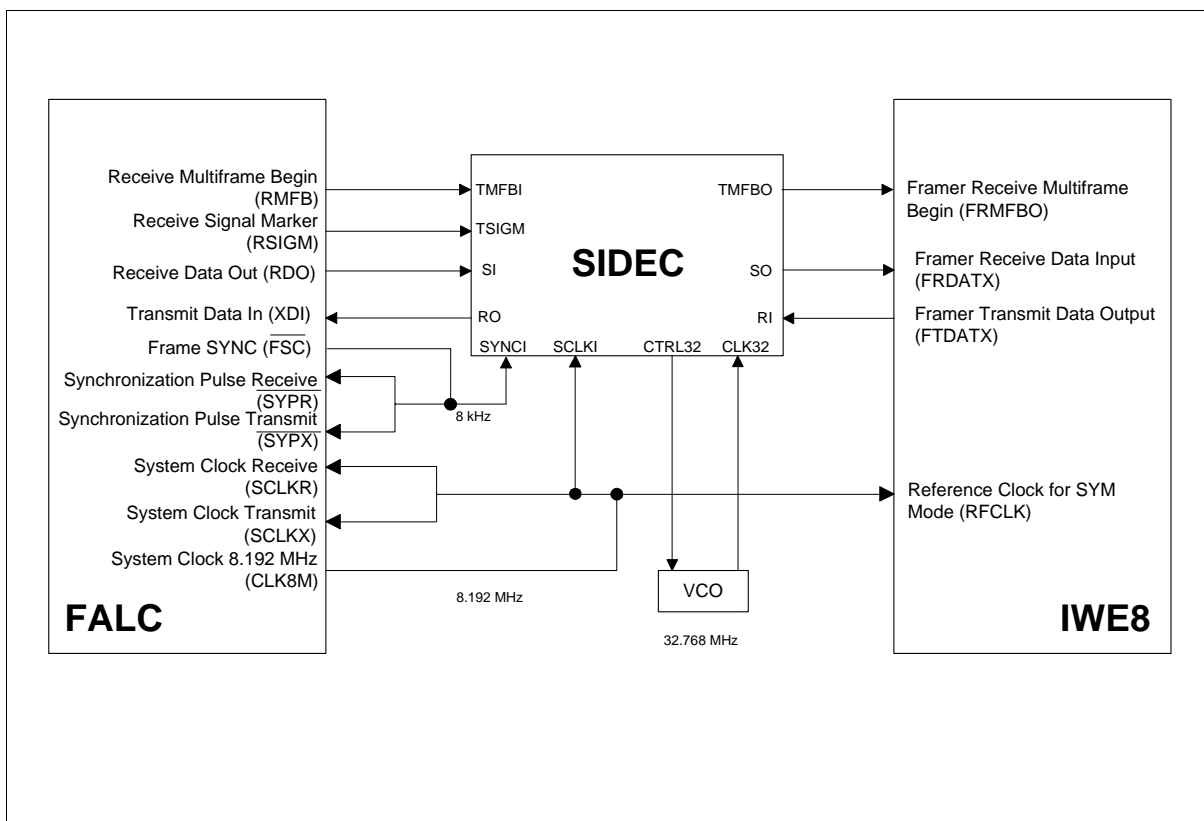


Figure 11 Internet Working Unit: SIDEC between a FALC and IWE8

4.2 Synchronization and Clock Modes

The SIDEc can be connected in different synchronization and clock modes. These modes can be used for several applications.

Basically there are two clock modes, slave and master clock mode (not to be mixed up with 128 ms master and slave mode). The internal clock system in master clock mode is automatically synchronized to the system clock by using an external 32.768 MHz VCO or by generating and deriving the system clock at output pin SCLKO directly from the CLK32 input. SIDEc in master clock mode provides a synchronization pulse at pin SDECO. This pulse can be used by a SIDEc in slave clock mode to synchronize its internal clock system to the system clock without the needs for additional external VCO.

Examples for this mode are the 128 ms delay application and the multiple SIDEc application, see also **Figure 16** and **Figure 17**.

CLK40 is 4.096 MHz system clock output for subsequent circuits, derived from SCLKI.

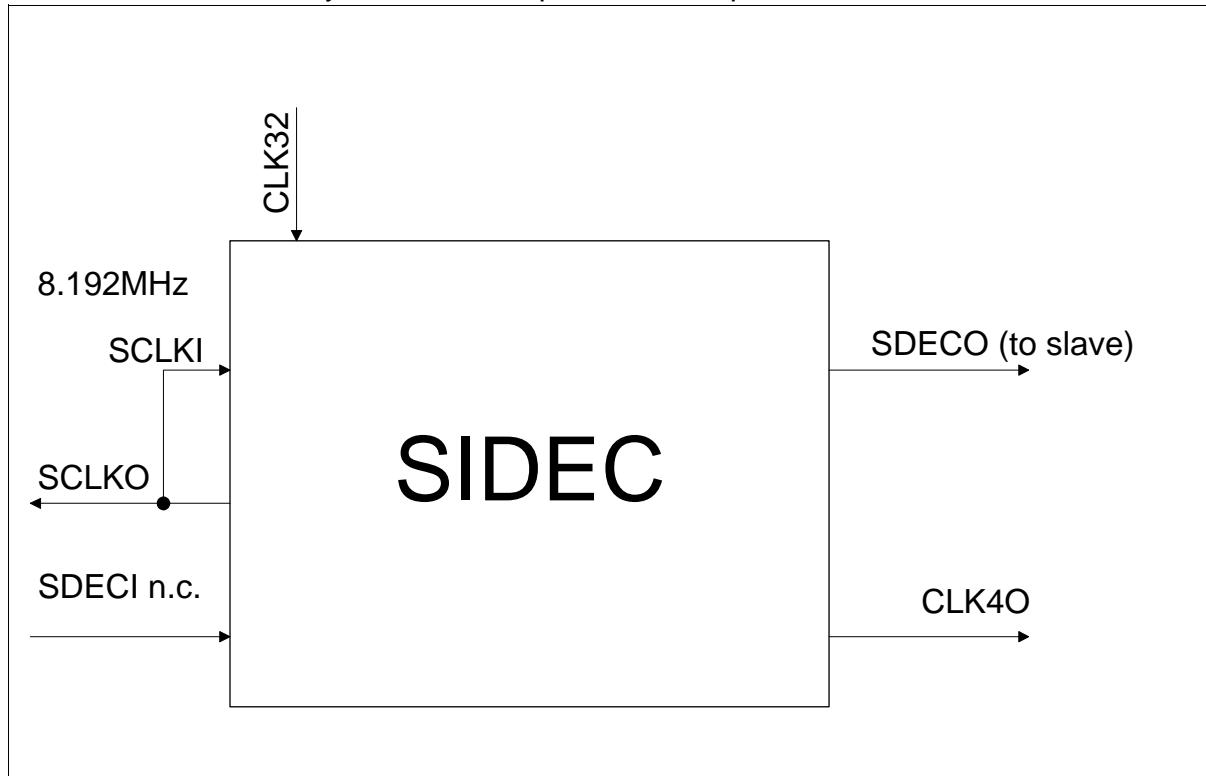


Figure 12 Master Clock Mode with External 32.768 MHz Clock without 8.192 MHz System Clock Input

In **Figure 12** the system clock is reconnected from SCLKO to SCLKI in order to properly process the PCM signals. The system clock at pin SCLKO can also be provided for other devices. The SDECI pin is not connected in the master clock mode. A 32.768 MHz clock has to be provided by an external clock oscillator or other clock source on the system.

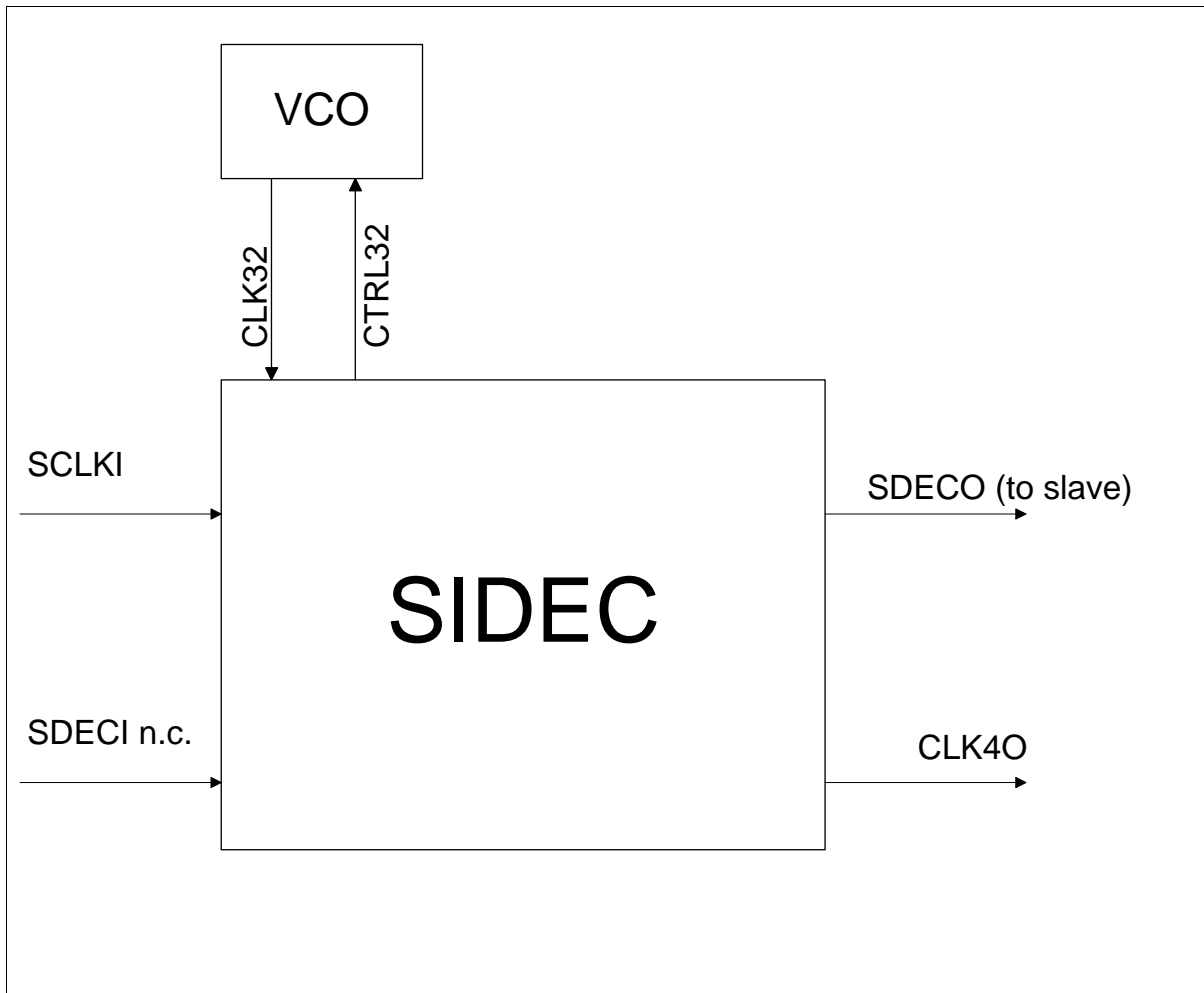


Figure 13 Master Clock Mode with External 8.192 MHz Clock

In the master clock mode with 8.192 MHz clock (**Figure 13**), the 32.768 MHz operating clock is supplied by the VCO. The SIDEc provides a controlling voltage for the VCO in order to synchronize the CLK32 to the system clock SCLKI.

SDECI is not connected and the SDECO can be connected to other SIDEcs.

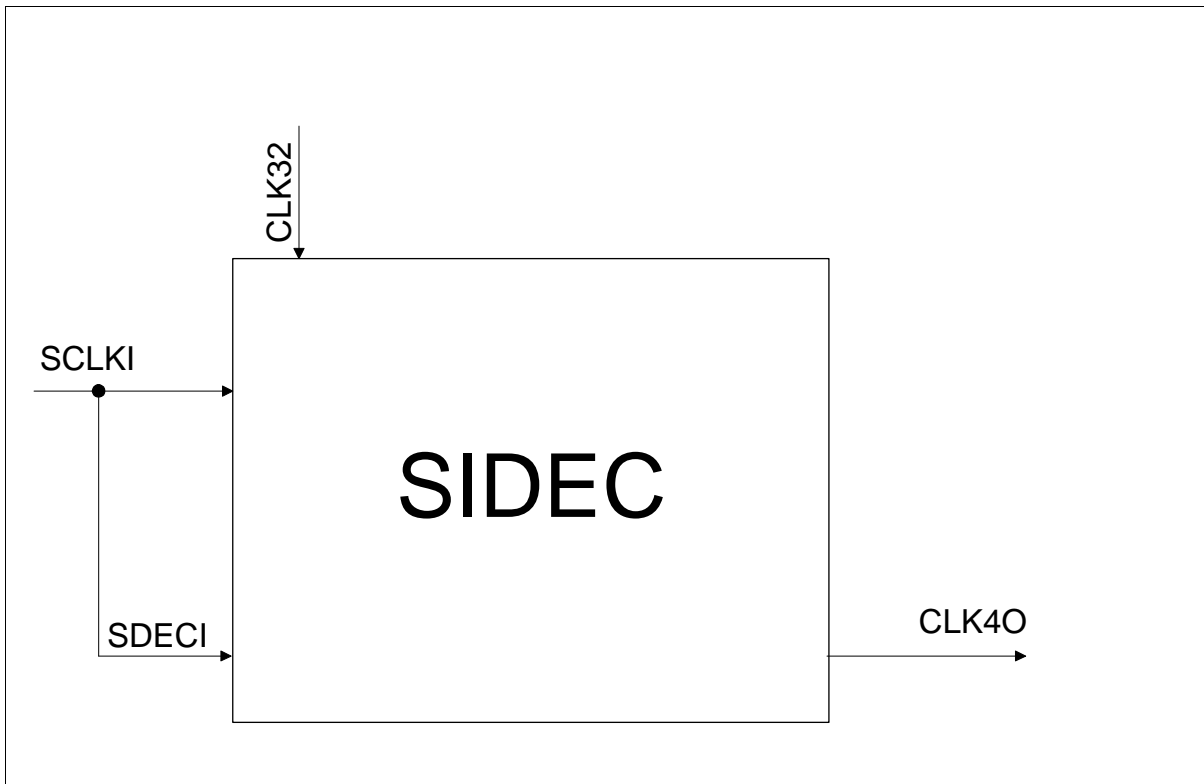


Figure 14 Slave Clock Mode with External 8.192 MHz and 32.768 MHz

In the slave clock mode the 8.192 MHz and the 32.768 MHz clock have to be synchronous and phase aligned (e.g. SCLKI has been derived from CLK32 by some external device). There is no internal synchronization between SCLKI and CLK32. SDECI is needed for correct phase alignment of SCLKI to the internal system clock.

CLK40 is a 4.096 MHz system clock output for subsequent circuits, derived from SCLKI

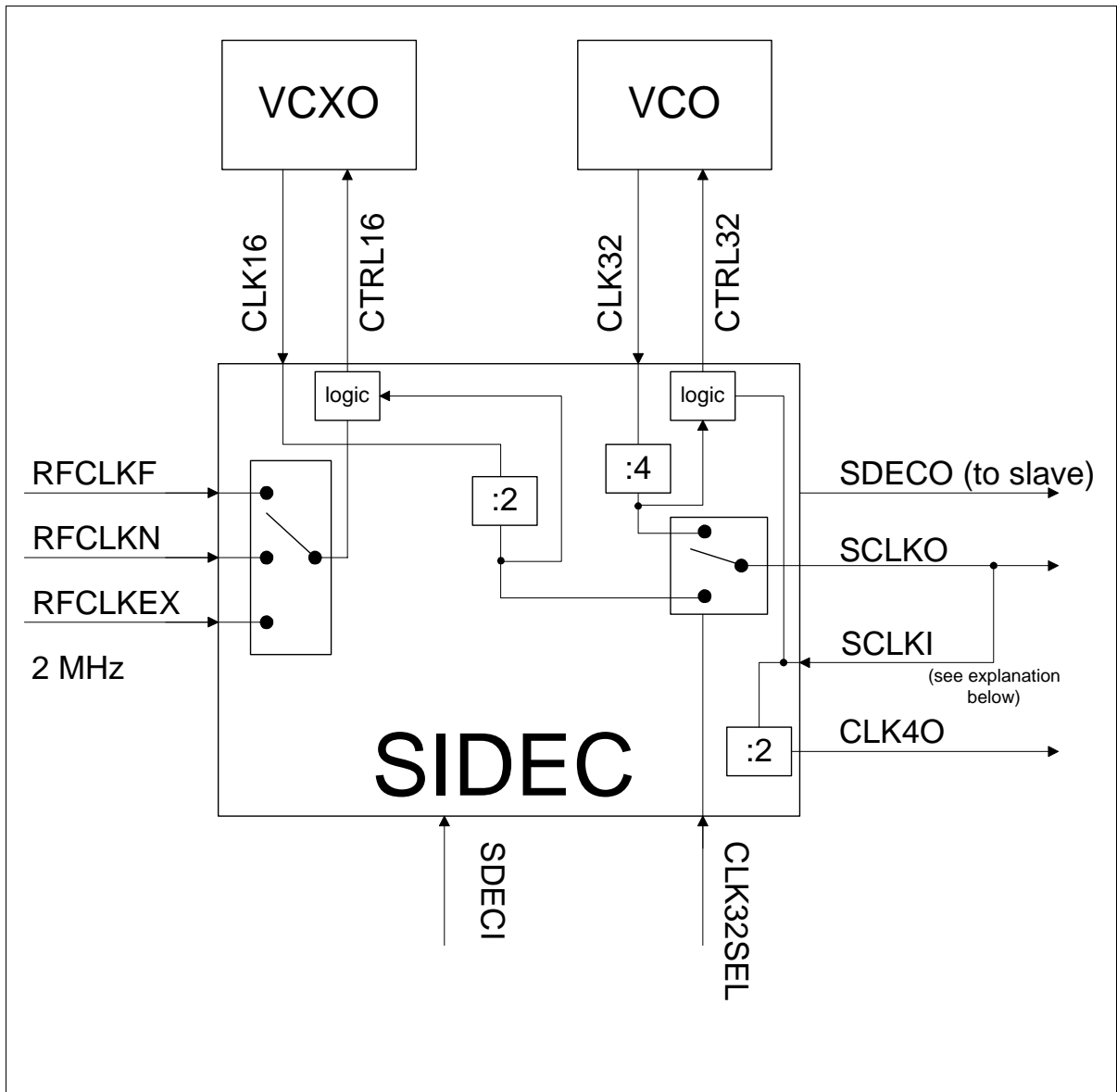


Figure 15 Reference Clock Mode with 2.048 MHz

In this mode a 2.048 MHz system clock is provided at either the RFCLKF, RFCLKN or the RFCLKEX pin. The VCXO and VCO supply the operating clocks for the SIDEc. SDECO can be connected to slave. The feedback from SCLKO to SCLKI in order to generate a control voltage for the 32 MHz VCO makes only sense if SCLKO is derived from CLK16. The SDECI initializes the counter.

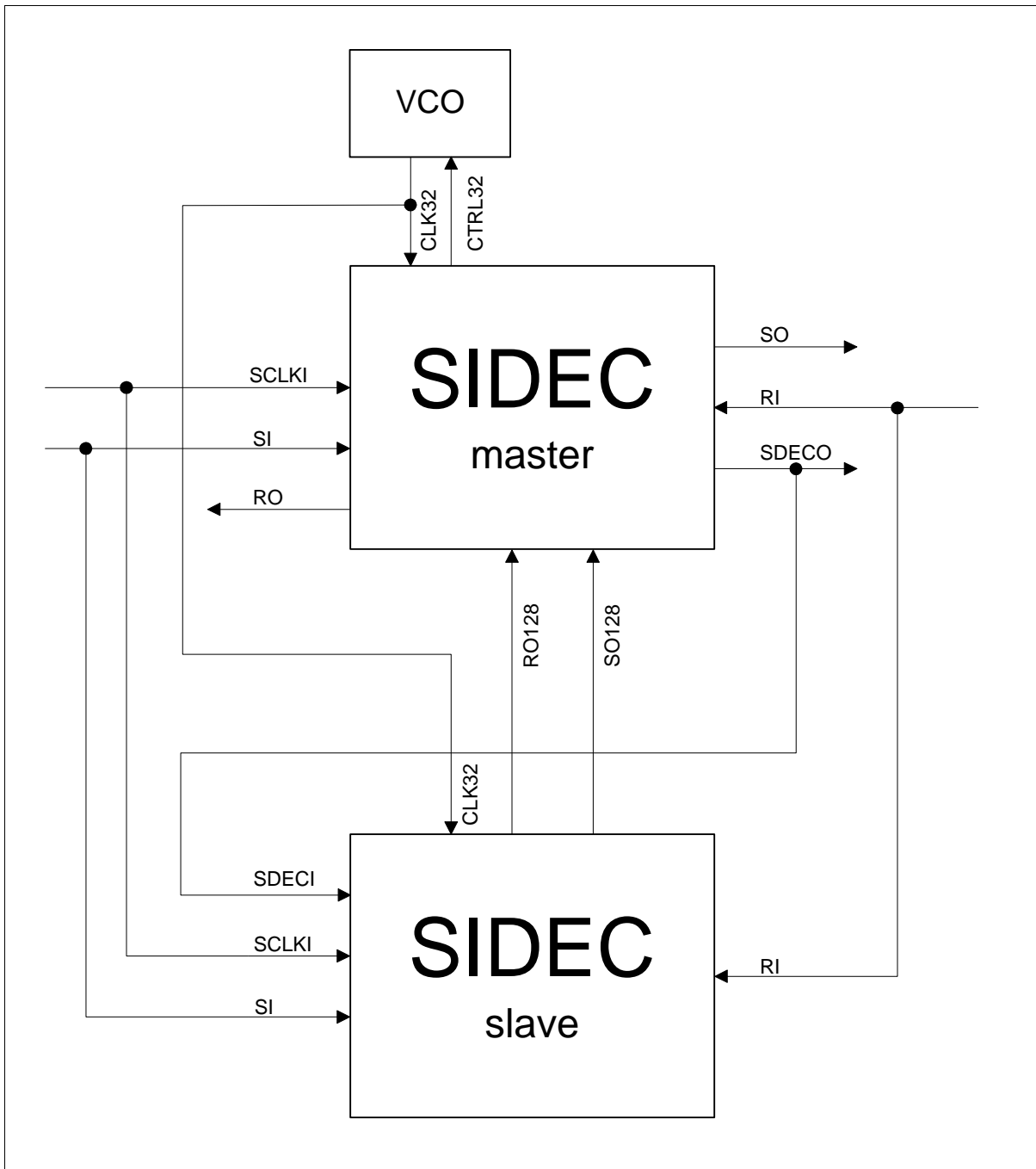


Figure 16 128 ms Delay Mode

The pin connection of a 128 ms master and slave SIDEC is shown in **Figure 16**. The SI and RI is supplied to both SIDECs. The RO and SO is provided by the master. The RO128 and SO128 signals are used to multiplex the 128 ms slave data into the PCM data stream outputs of the master.

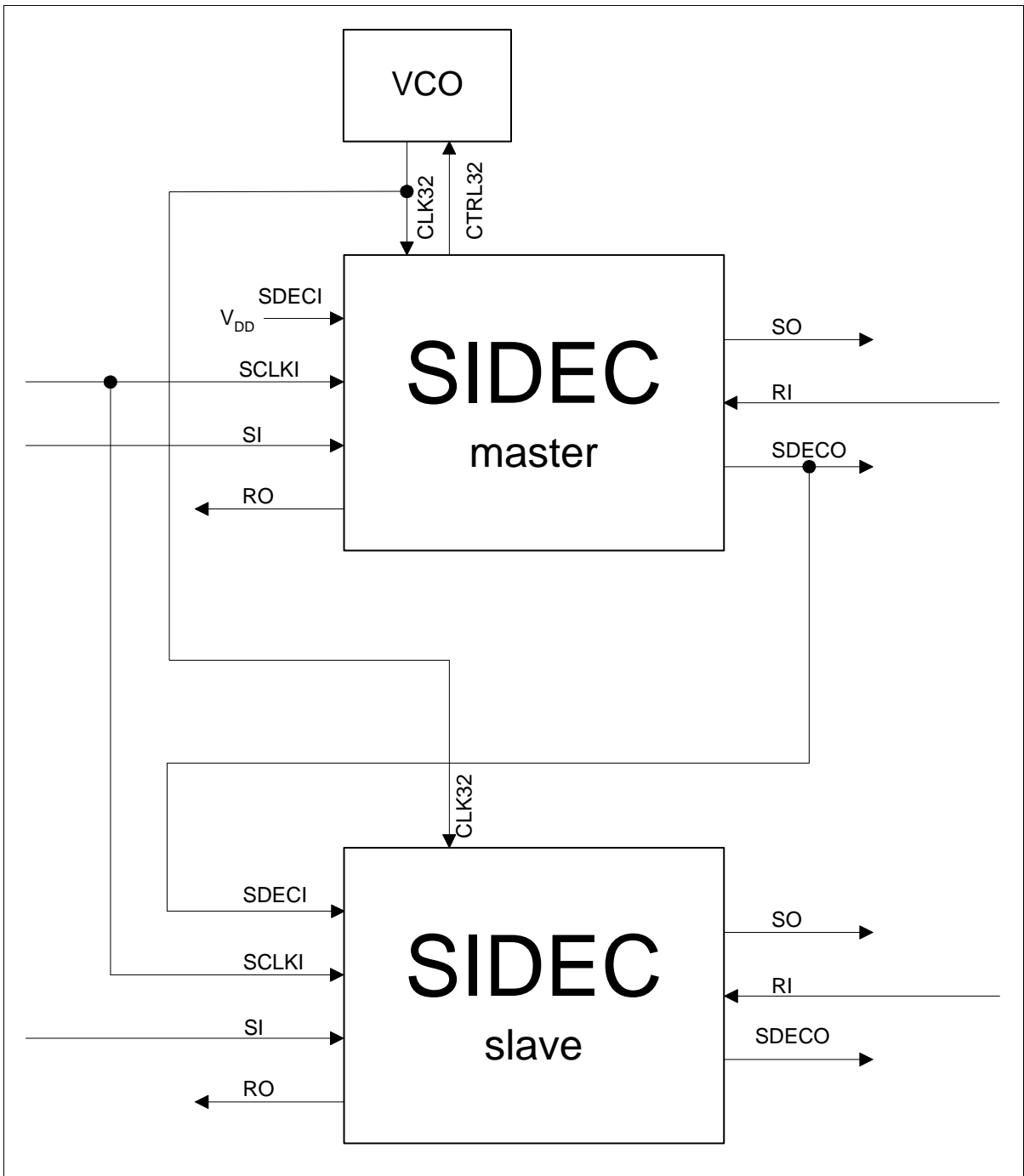


Figure 17 Multiple SIDEC

In multiple SIDEC mode the output SDECO of the clock master SIDEC is used to synchronize clock slave SIDECs to the system clock. In this application multiple E1/T1 lines can be echo cancelled, one E1/T1 line per SIDEC. Leave the SDECI of the master SIDEC open or connect it to ground.

4.3 Timing Patterns

4.3.1 Clock Timing

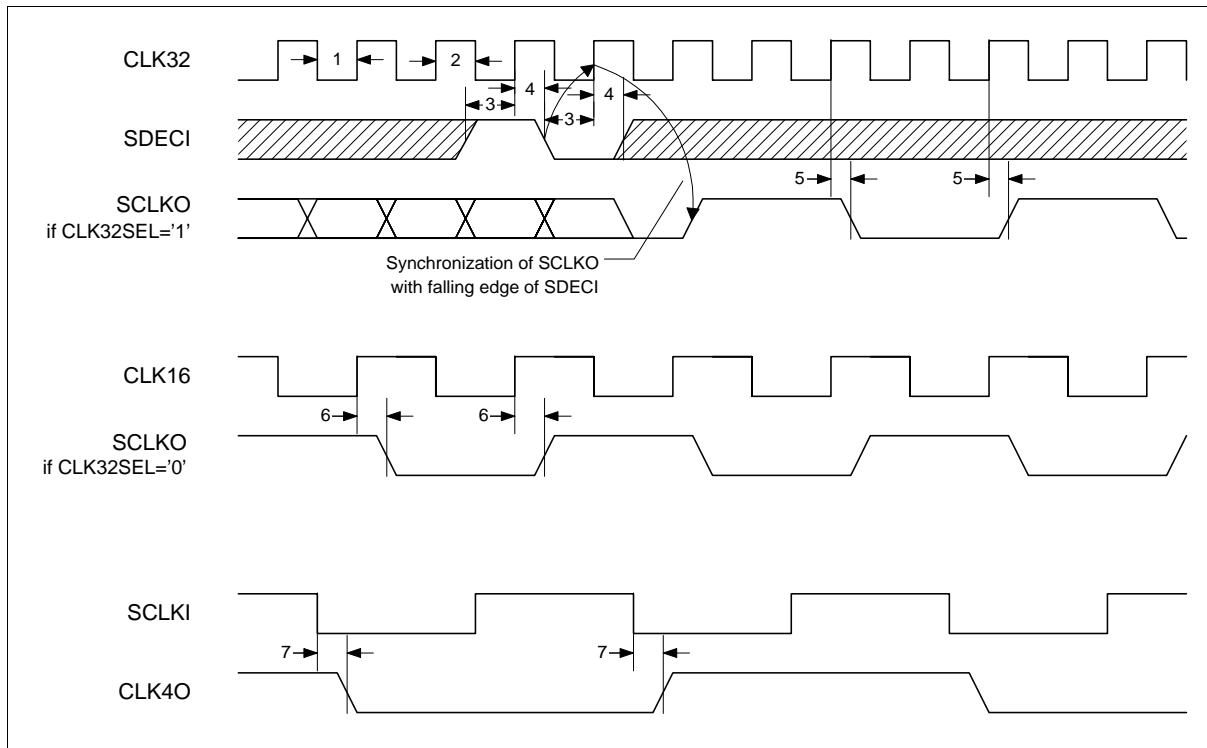


Figure 18 Clock Timing

Table 12 Clock Timing Characteristics (preliminary)

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_clk32_low	CLK32 low time	12		ns
2	t_clk32_high	CLK32 high time	12		ns
3	t_sdeci_setup	SDECI setup time before CLK32 ↑	10		ns
4	t_sdeci_hold	SDECI hold time after CLK 32 ↑	15		ns
5	t_sclko_delay_clk32	SCLKO output delay after CLK32 ↑		30	ns

Operational Description

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
6	t_sclko_delay_clk16	SCLKO output delay after CLK16 ↑	0	30	ns
7	t_clk4o_delay	CLK4O output delay after SCLKI ↓	0	30	ns

Table 13 **Periods of Clock Signals**

No.	Parameter	min.	nom.	Unit
	CLK32	30	30.52	ns
	CLK16		61.04	ns
	SCLKI		122.07	ns
	CLK4O		244.14	ns

4.3.2 PCM Signal Timing and Frame Alignment

The SIDEDEC requires the MSB (bit7) first and the LSB (bit0) last as input

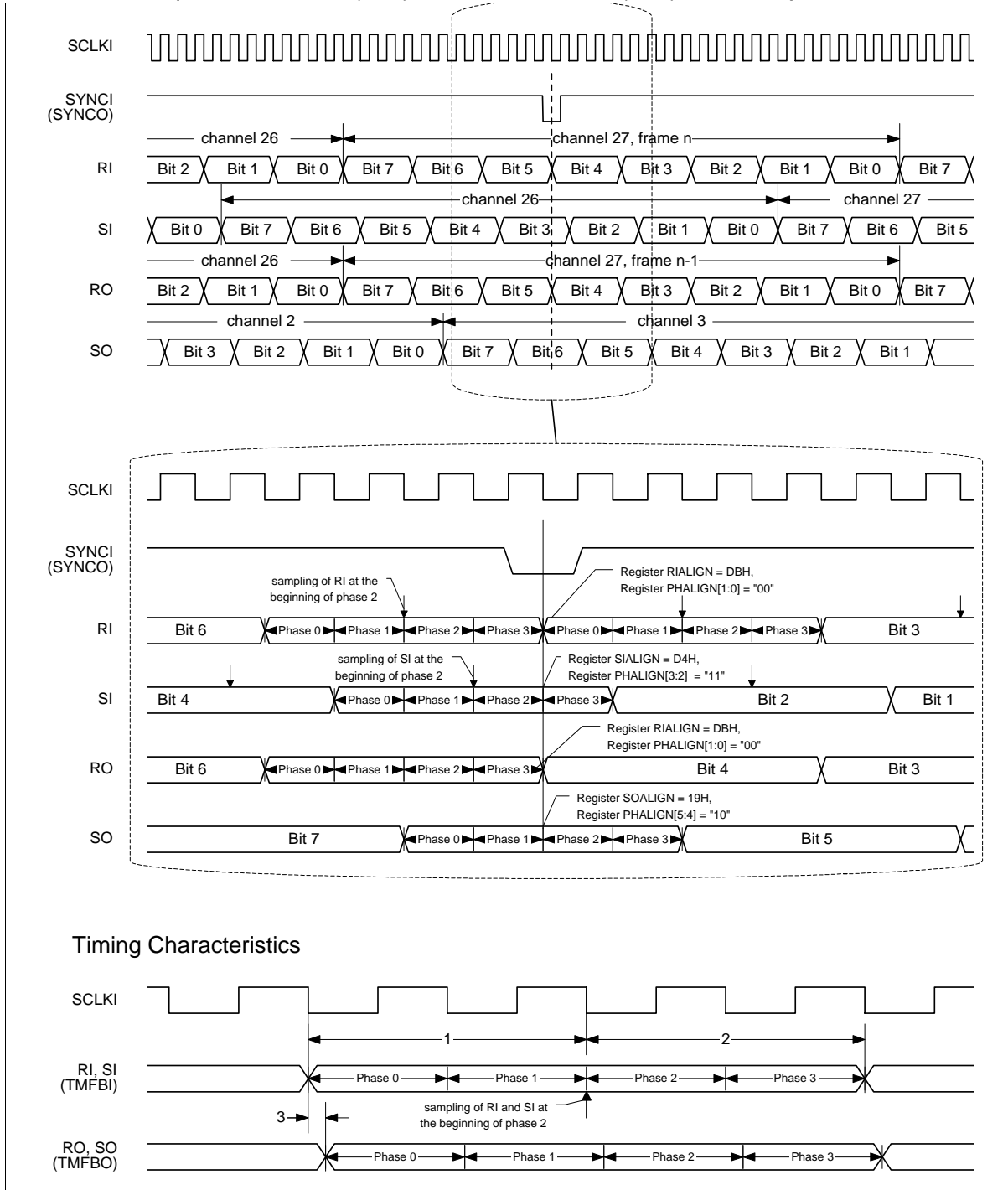


Figure 19 PCM Signal Timing and Frame Alignment

Operational Description

Note: Above values are examples only. PCM frame alignment with respect to the first detection of an active SYNCI (or SYNCO: If no SYNCI is applied, SYNCO takes over the part and role of SYNCI) with the falling edge of SCLKI can be configured by writing to the registers RIALIGN, SIALIGN and SOALIGN. For finer adjustments, the valid bit phase of the PCM signals at the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the register PHALIGN. The configured frame and bit phase alignment always denotes the beginning of the ideal bit phase (no signal delay) at the falling edge of SCLKI.

PCM inputs are always sampled with the falling edge of SCLKI at the beginning of bit phase 2, outputs are clocked with the falling edge of SCLKI at the beginning of bit phase 0. Unless not bypassed the PCM output RO has a fixed delay of one PCM frame (125 μ s) with respect to RI.

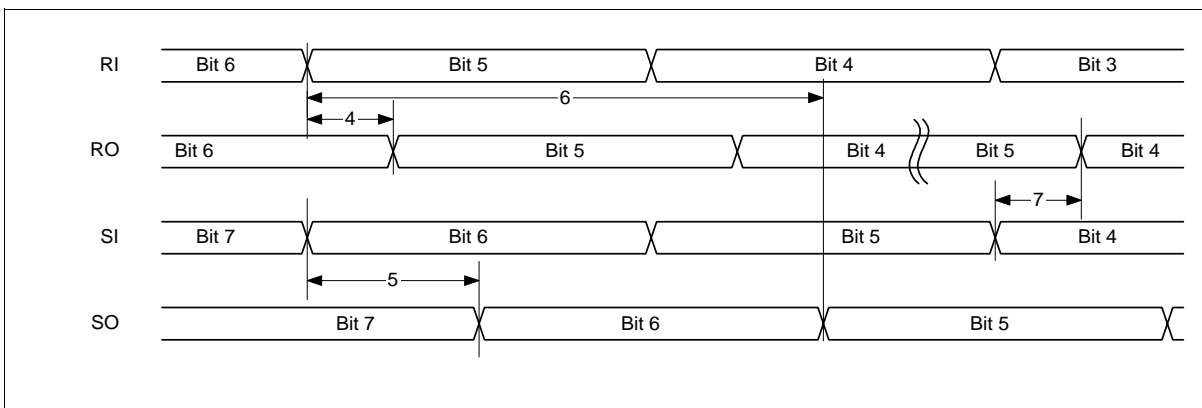


Figure 20 Delay of PCM Signals

Figure 21 illustrates the synchronization of the 2048 kBit/s PCM and UCC signal for a low active SYNCI signal with respect to the internal 8192 kHz SCLKI signal. If SYNCI is sampled with the falling edge of SCLKI (CONFCC.SSCLKEDGE='0') this edge is the synchronization point for PCM and UCC signals. If SYNCI is sampled with the rising edge of SCLKI (CONFCC.SSCLKEDGE='1') the next falling SCLKI edge is the synchronization point for PCM and UCC signals. The SYNCO signal may only be used instead of the SYNCI signal if the UCC Interface is not used

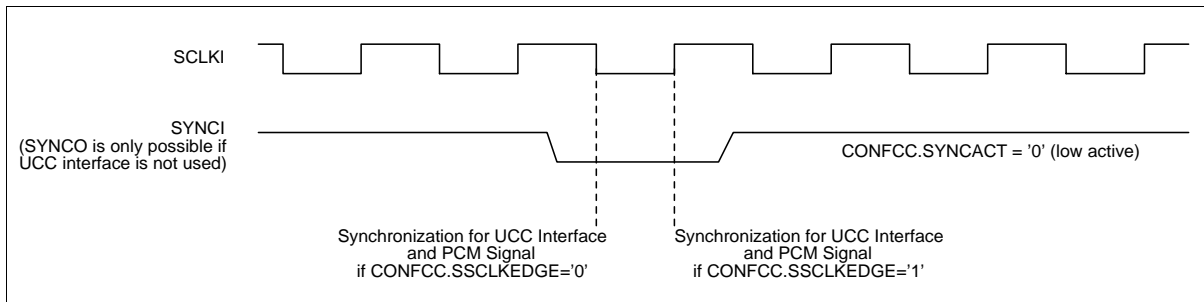


Figure 21 Synchronization of PCM and UCC Signal with respect to SCLKI and SYNCI

Table 14 PCM Signal Timing and Frame Characteristics (preliminary)

No.		Parameter	Limit Values		Unit
			min.	max.	
1	t_pcm_setup	PCM input (RI,SI) input setup time before sampling with SCLKI ↓	15		ns
2	t_pcm_hold	PCM input (RI,SI) input hold time after sampling with SCLKI ↓	15		ns
3	t_pcm_delay	PCM output (RO,SO) delay after SCLKI ↓	0	30	ns
4	t_pcm_ri2ro_delay	delay for bypass RI to RO	0	30	ns
5	t_pcm_si2so_delay	delay for bypass SI to SO	0	30	ns
6	t_pcm_ri2so_delay	delay for bypass RI to SO	0	30	ns
7	t_pcm_si2ro_delay	delay for bypass SI to RO	0	30	ns

4.3.3 Timing of SYNCI and SYNCO

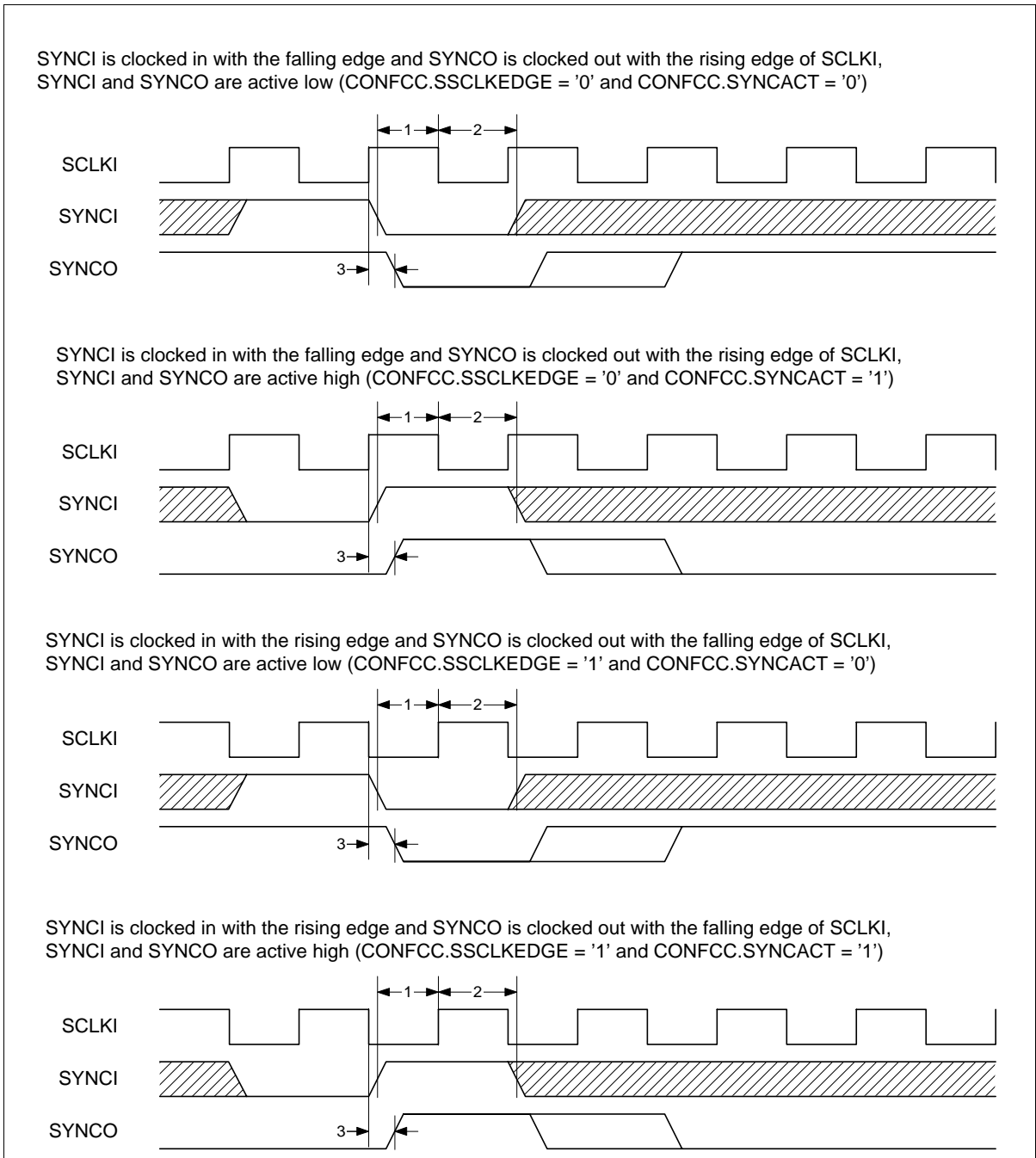


Figure 22 Timing of SYNCI and SYNCO

Figure 22 shows the timing of the synchronization pulses for different configurations.

Operational Description

Note: The duration of SYNCO pulse can be configured by register CONFCC.SYNCODUR to either one or two SCLKI (8.192 MHz) periods.

Table 15 Characteristics of Timing of SYNCI and SYNCO (preliminary)

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_synci_setup	SYNCI setup time before active sampling edge of SCLKI	10		ns
2	t_synci_hold	SYNCI hold time after active sampling edge of SCLKI	10		ns
3	t_synco_delay	SYNCO delay after active output edge of SCLKI	0	30	ns

4.3.4 Clock Timing within External VCO Capture Range

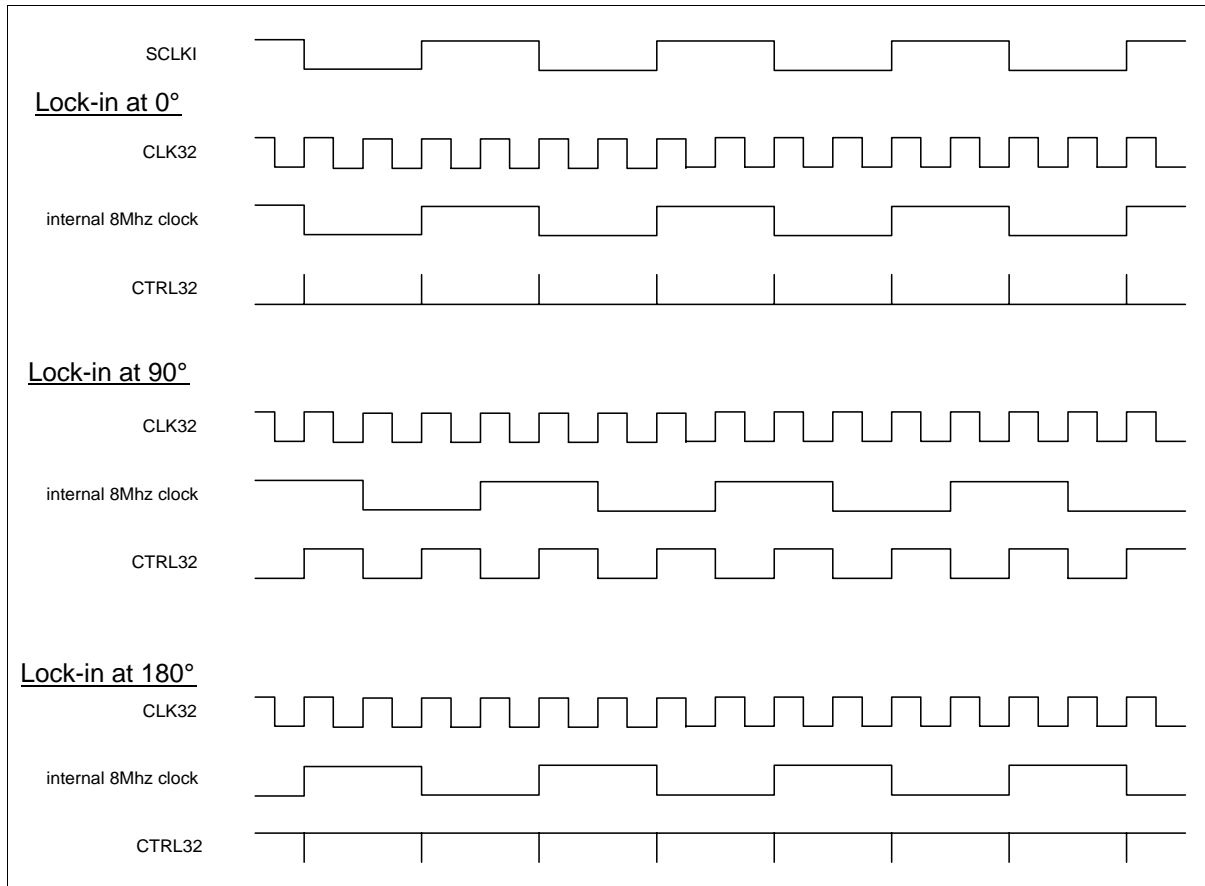


Figure 23 Clock Timing within External VCO Capture Range

In case a 32.768 MHz clock has to be generated and synchronized to the system clock at SCLKI, the signal at pin CTRL32 can be used to control an external VCO. The output at CTRL32 is the signal at SCLKI that is internally 'xored' with an internal 8.192 MHz clock that is derived from the signal pin CLK32 by division by 4. For proper operation of the SIDEK the system clock SCLKI and the internal 8.192 MHz clock must lock in within the capture range from 0° to 180°. CTRL32 can be inverted by bit CONFCC.INVCTRL32 for use of VCOs that increase the frequency with falling voltage.

The internal 8.192 MHz clock can be monitored at pin SCLKO with a delay of three CLK32 periods plus internal signal delay if pin CLK32SEL is set to logic '1'.

4.3.5 Serial Interface (Controlling and Monitoring) Timing

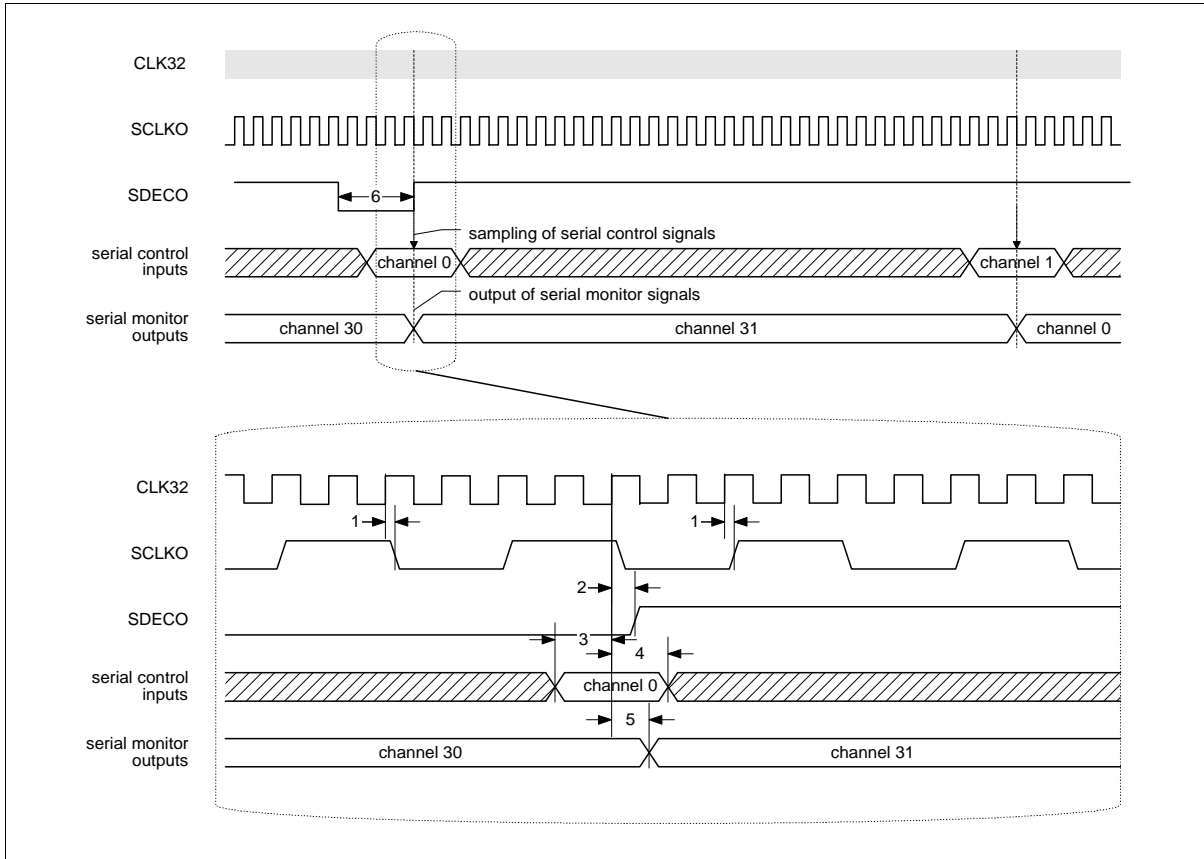


Figure 24 Serial Interface (Controlling and Monitoring) Timing

Table 16 Serial Interface (Controlling and Monitoring) Timing (preliminary)

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_sdeco_delay	SDECO output delay after CLK32 ↑	0	30	ns
2	t_sctr_setup	Serial control signal setup time before sampling with CLK32 ↑	15		ns
3	t_sctr_hold	Serial control signal hold time after sampling with CLK32 ↑	15		ns

Operational Description

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
4	t_smon_delay	Serial monitor signal output delay after CLK32 ↑	0	30	ns
5		SDECO duration	16 * CLK32 period		

4.3.6 UCC Interface Signal Timing and Frame Alignment

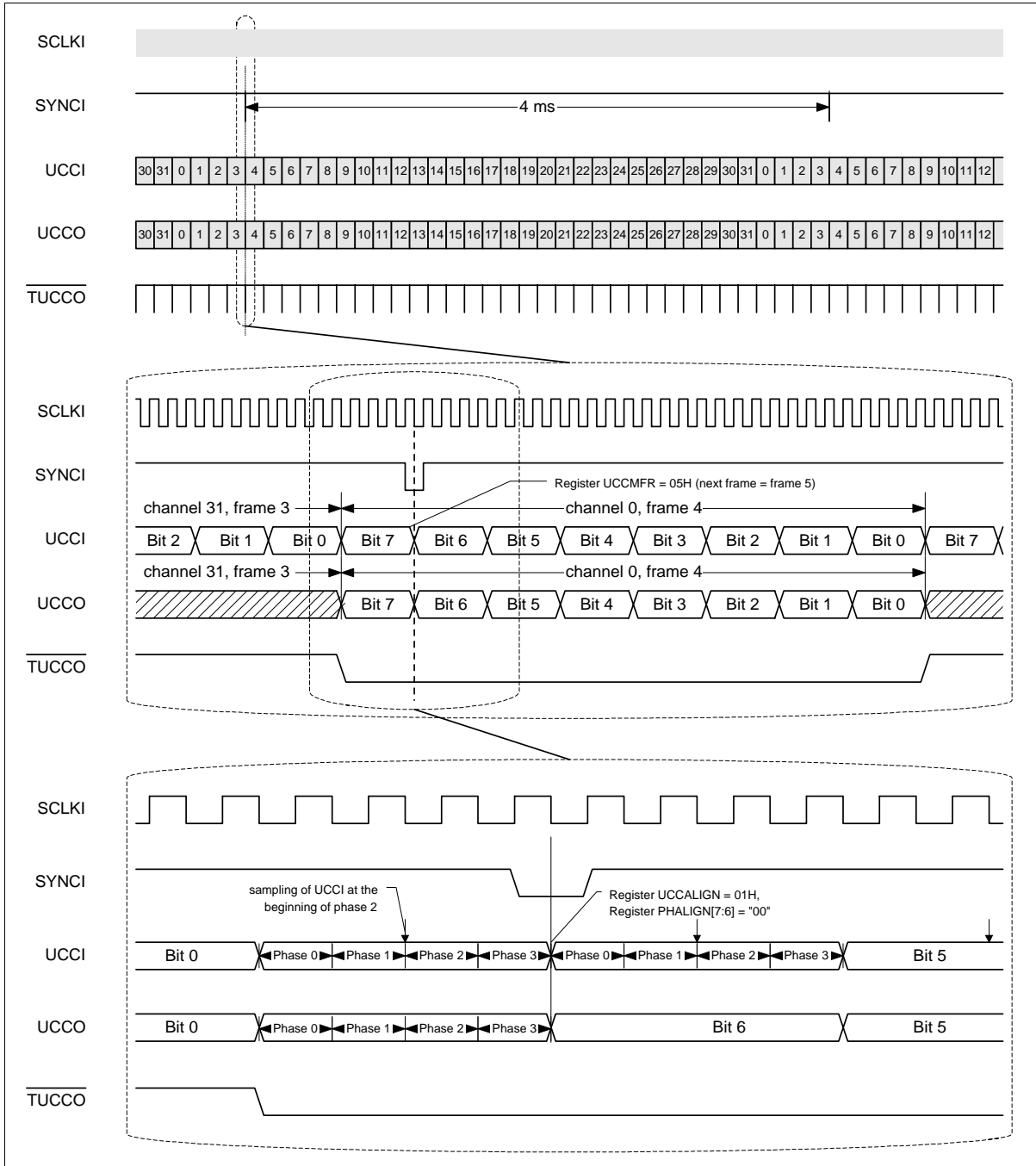


Figure 25 UCC Interface Signal Timing and Frame Alignment

Note: Above values are examples only. For the use of the UCC Interface a SYNCI signal with a period of 4 ms (equivalent to one multiframe) must be applied to the SIDEC. UCC frame and multiframe alignment with respect to the first detection of an active SYNCI

Operational Description

with the falling edge of SCLKI can be configured by writing to the registers UCCALIGN and UCCMFR. For finer adjustments, the valid bit phase of the UCC signals at the first detection of an active SYNCI with the falling edge of SCLKI can be configured by writing to the two MSBs of register PHALIGN.

The configured frame and bit phase alignment always denotes the beginning of the ideal bit phase (no signal delay) at the falling edge of SCLKI. If SYNCI is sampled with the falling edge of SCLKI (CONFCC.SSCLKEDGE='0') this edge is the synchronization point for PCM and UCC signals. If SYNCI is sampled with the rising edge of SCLKI (CONFCC.SSCLKEDGE='1') the next falling SCLKI edge is the synchronization point for PCM and UCC signals. This behavior is identical to the PCM signal behavior and illustrated in **Figure 21** in **Chapter 4.3.2**

UCC inputs are always sampled with the falling edge of SCLKI at the beginning of bit phase 2, UCCO and $\overline{\text{TUCCO}}$ are clocked out with the falling edge of SCLKI at the beginning of bit phase 0. The value of register UCCMFR denotes the frame number of the next complete frame that starts with phase 0, bit 7, channel 0 **after** the first detection of an active SYNCI with the falling edge of SCLKI (see figure below).

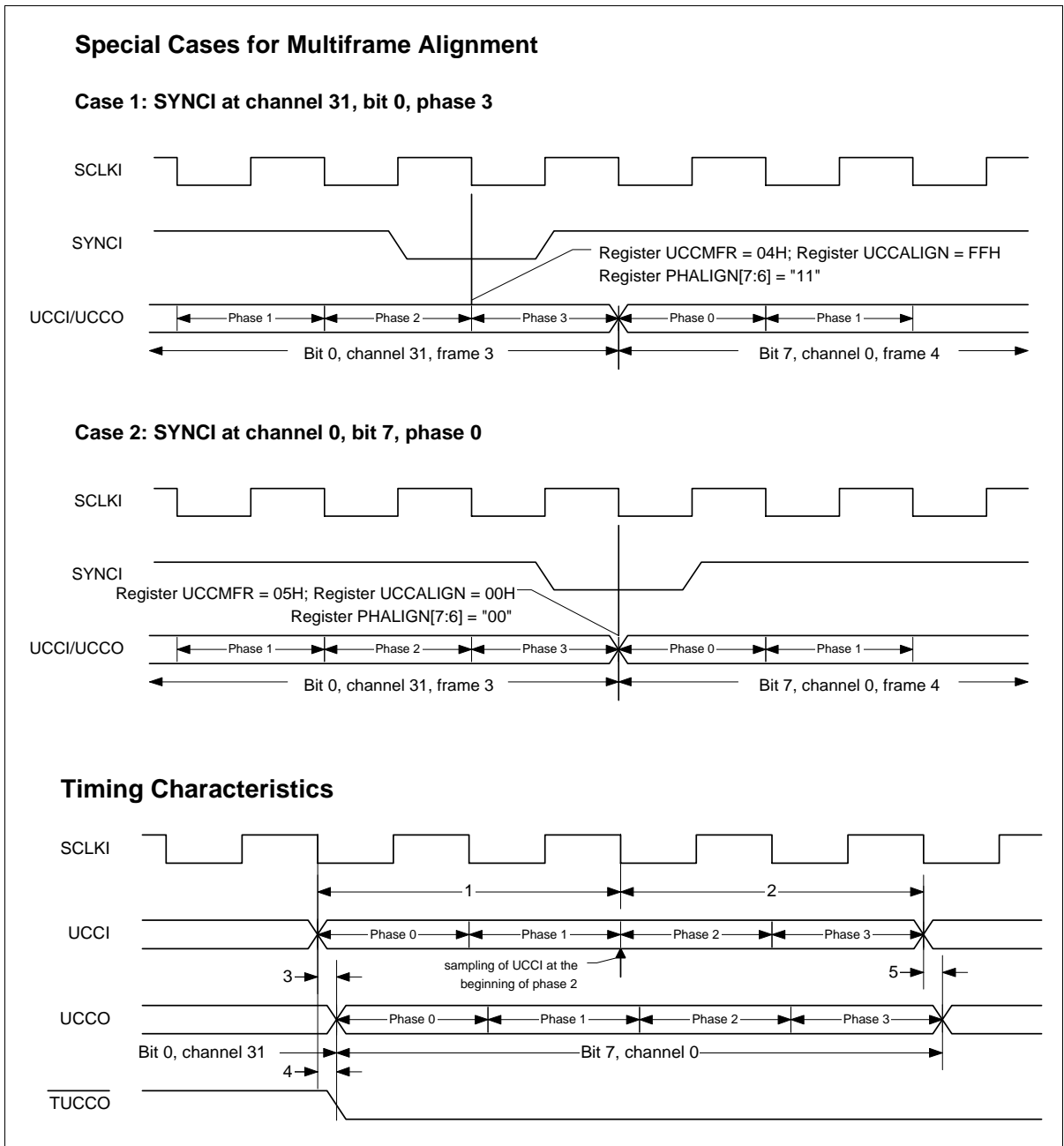


Figure 26 Special Cases for Multiframe Alignment and Timing Characteristics

Table 17 UCC Interface Signal Timing and Frame Alignment (preliminary)

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_ucci_setup	UCCI input setup time before sampling with SCLKI ↓	15		ns
2	t_ucci_hold	UCCI input hold time after sampling with SCLKI ↓	15		ns
3	t_ucco_delay	UCCO output delay after SCLKI ↓	0	30	ns
4	t_tucco_delay	$\overline{\text{TUCCO}}$ output delay after SCLKI ↓	0	30	ns
5	t_ucc_reflect_delay	Propagation delay from UCCI to UCCO for UCC reflect mode	0	30	ns

4.3.7 Speech Highway Control Signals for CAS in T1 Systems

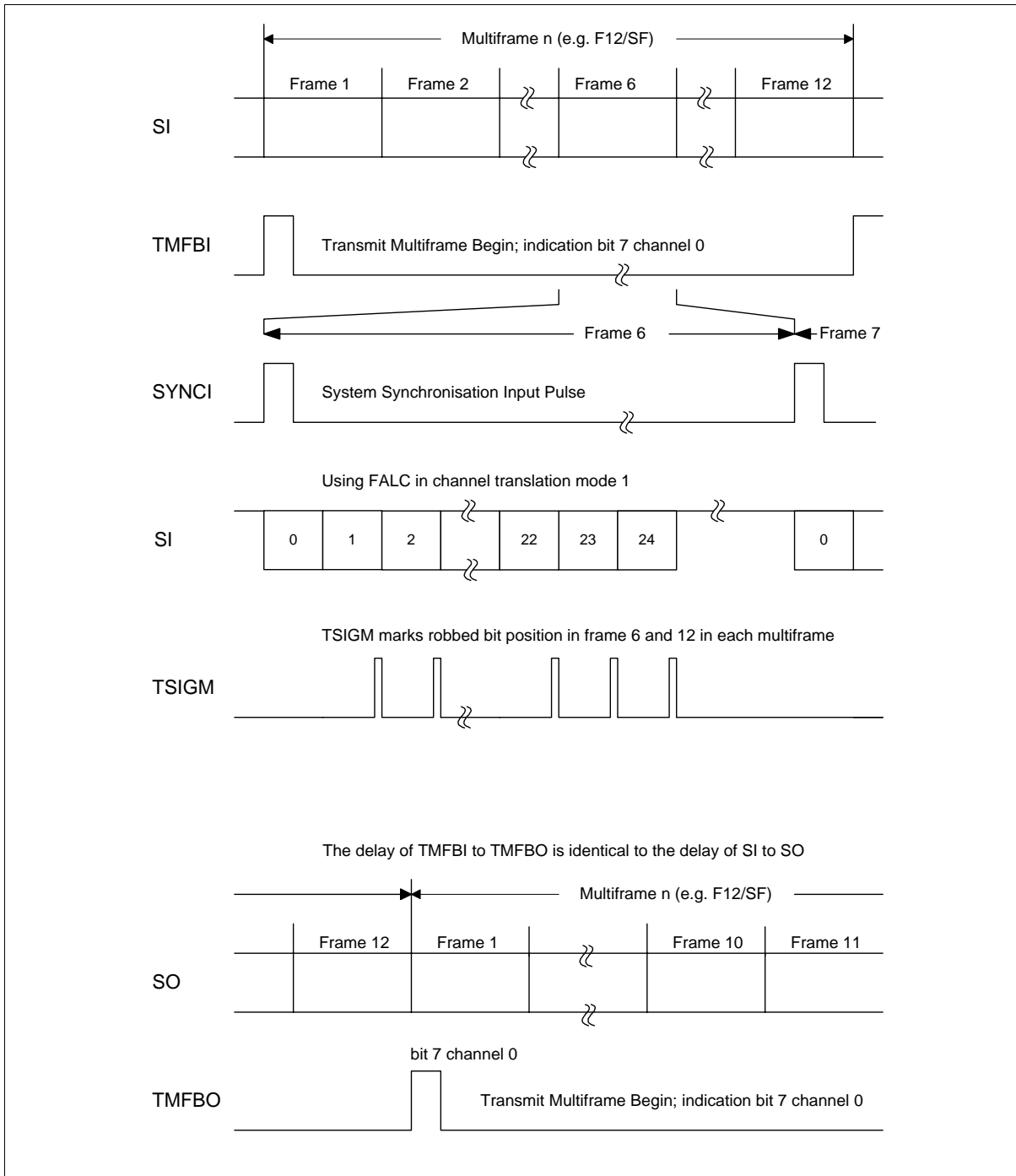


Figure 27 Timing of Supporting signals for CAS-BR Applications

4.3.8 Microprocessor Interface

The SIDEC Microprocessor Interface supports both, SIEMENS/Intel and Motorola mode. In each mode the address can be provided either through the multiplexed address/data or a parallel address bus. In multiplexed mode the address is always sampled with the falling edge of the address latch enable signal on the lower 7 bits of the multiplexed address/data bus. hence, addresses from 00H to 7FH are possible.

Read and write access in Intel mode is controlled by the assigned read and write signals. In Motorola mode it is provided by the data strobe and read/write signal.

The chip select signal is internally simply 'ored' with the read and write signal in Intel mode and with the data strobe signal in Motorola mode, thus enabling register access through chip select controlled Microprocessor cycles.

For fast processors there is also a ready/acknowledgment signal provided in order to eliminate the need for processor configured wait state insertion.

To write a value in a write protected register the value 95H needs to be written in the register Write Protection.

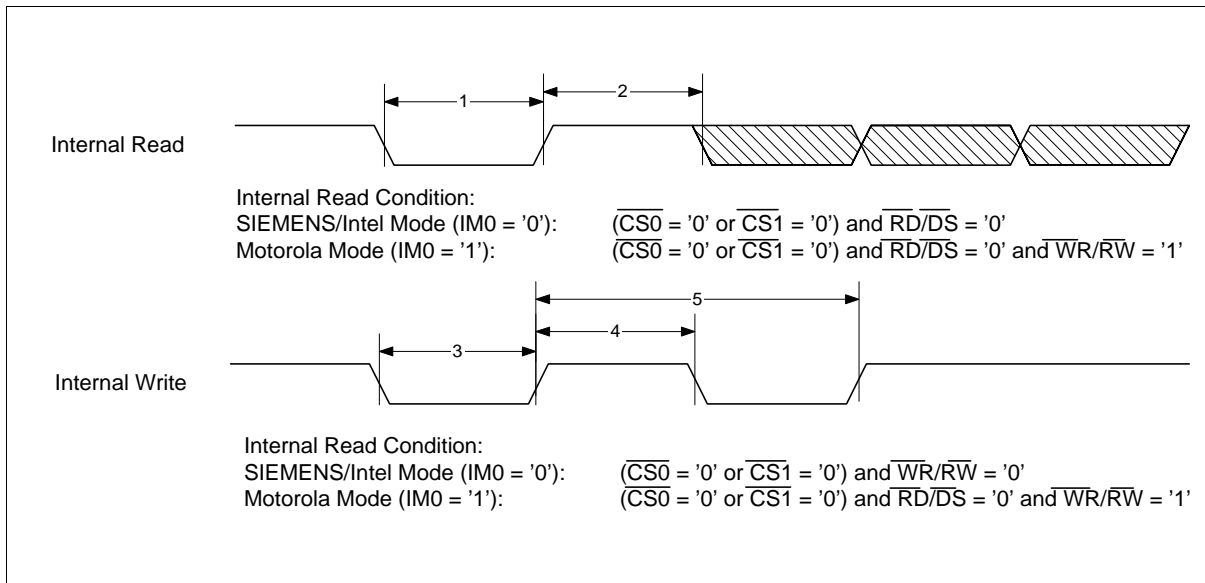


Figure 28 Internal Read Signal and Internal Write Signal

Table 18 Timing of (preliminary) Internal Read Signal and Internal Write Signal

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Active time	40		ns
2	Inactive time	40		ns
3	Active time	40		ns
4	Inactive time	40		ns
5	Interval between two active rising write edges	120		ns

The written value of a register will be valid for read back 120 ns after rising edge of the $\overline{WR/RW}$ signal.

4.3.8.1 Intel Mode (IM0='0')

a) Multiplexed Mode (IM1='0')

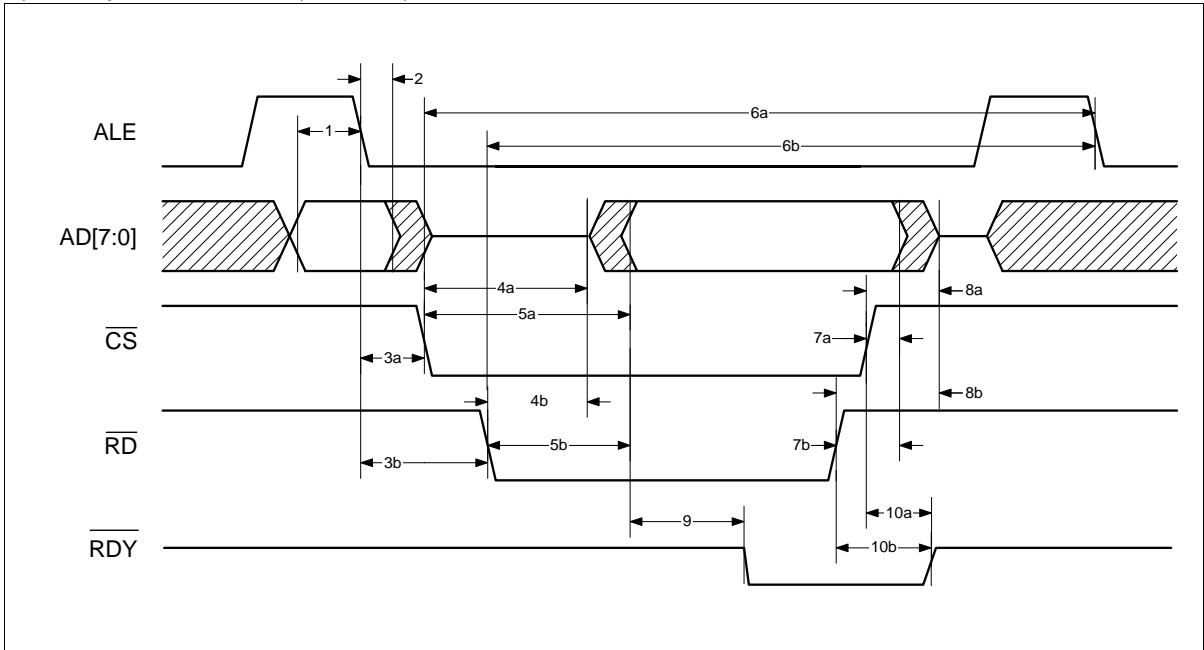


Figure 29 Read Timing in Multiplexed Intel Mode (IM0='0', IM1='0')

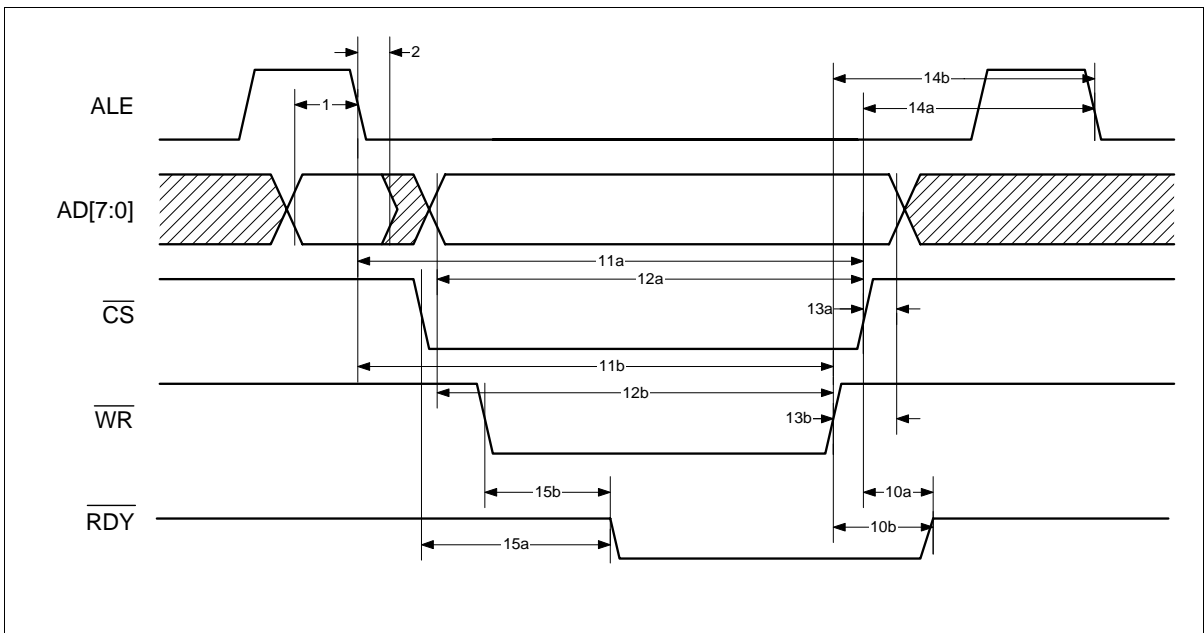


Figure 30 Write Timing in Multiplexed Intel Mode (IM0='0', IM1='0')

b) Demultiplexed Mode (IM1='1')

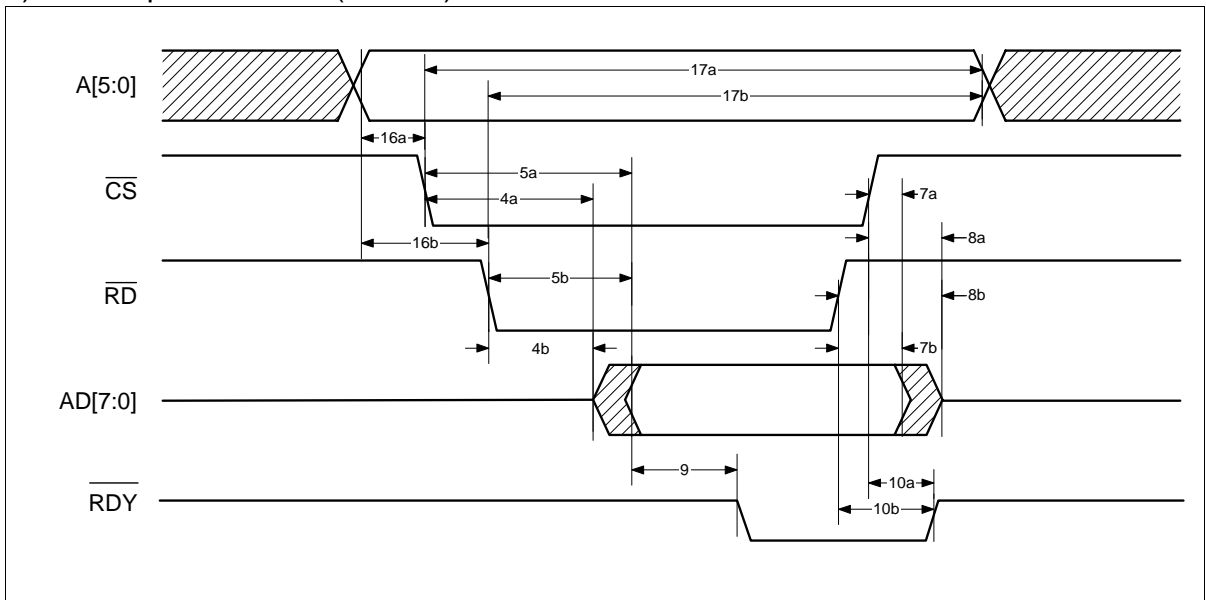


Figure 31 Read Timing in Demultiplexed Intel Mode (IM0='0', IM1='1')

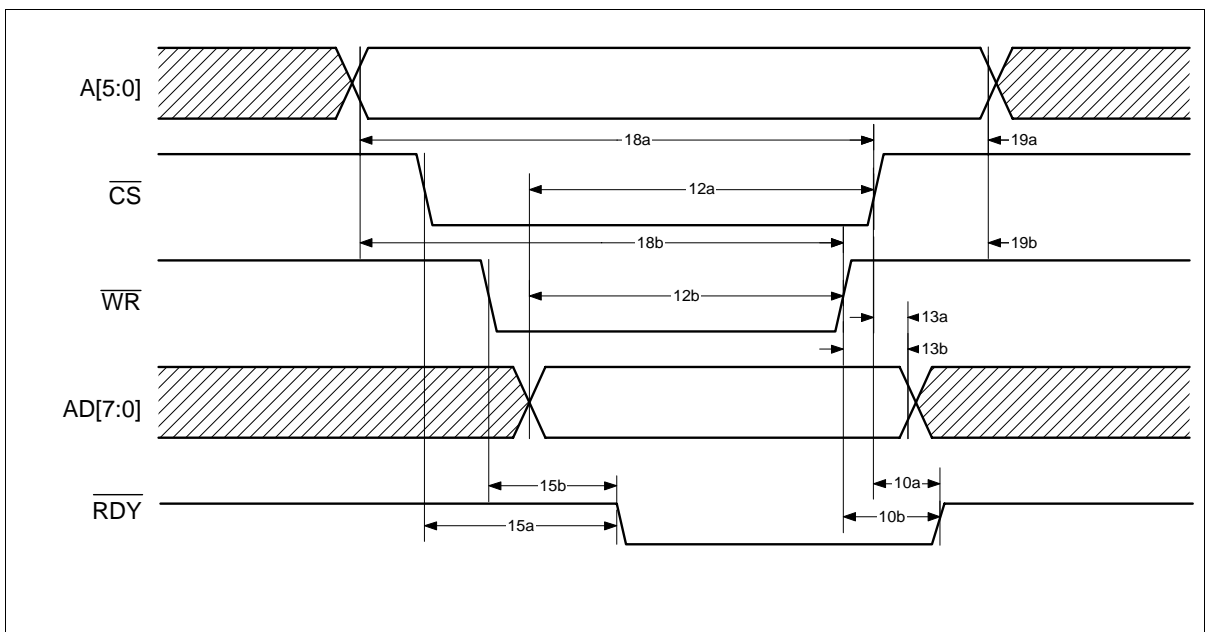


Figure 32 Write Timing in Demultiplexed Intel Mode (IM0='0', IM1='1')

4.3.8.2 Motorola Mode (IM0='1')

a) Multiplexed Mode (IM1='0')

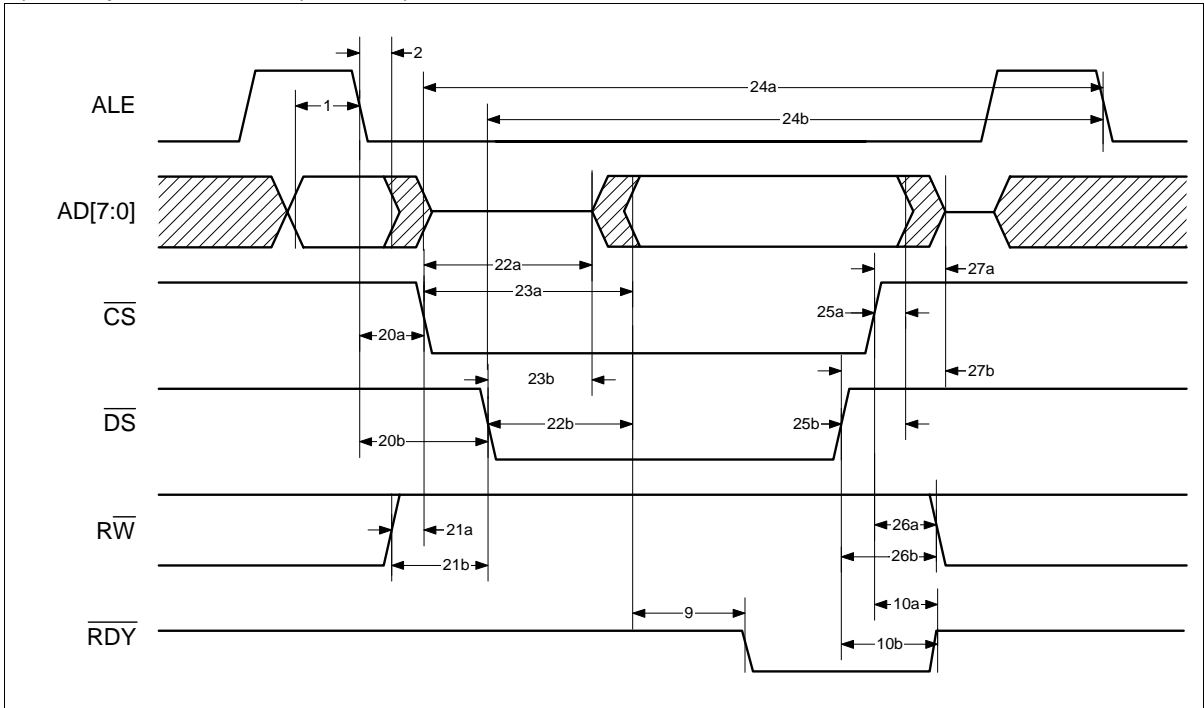


Figure 33 Read Timing in Multiplexed Motorola Mode (IM0='1', IM1='0')

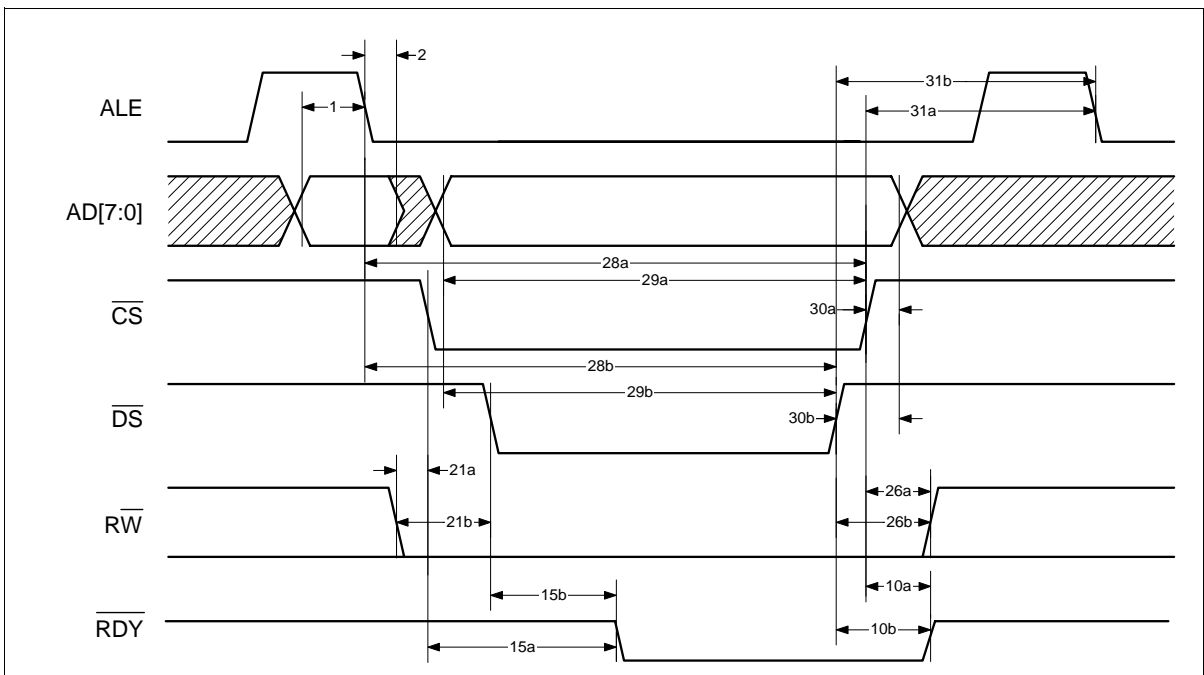


Figure 34 Write Timing in Multiplexed Motorola Mode (IM0='1', IM1='0')

b) Demultiplexed Mode (IM1='1')

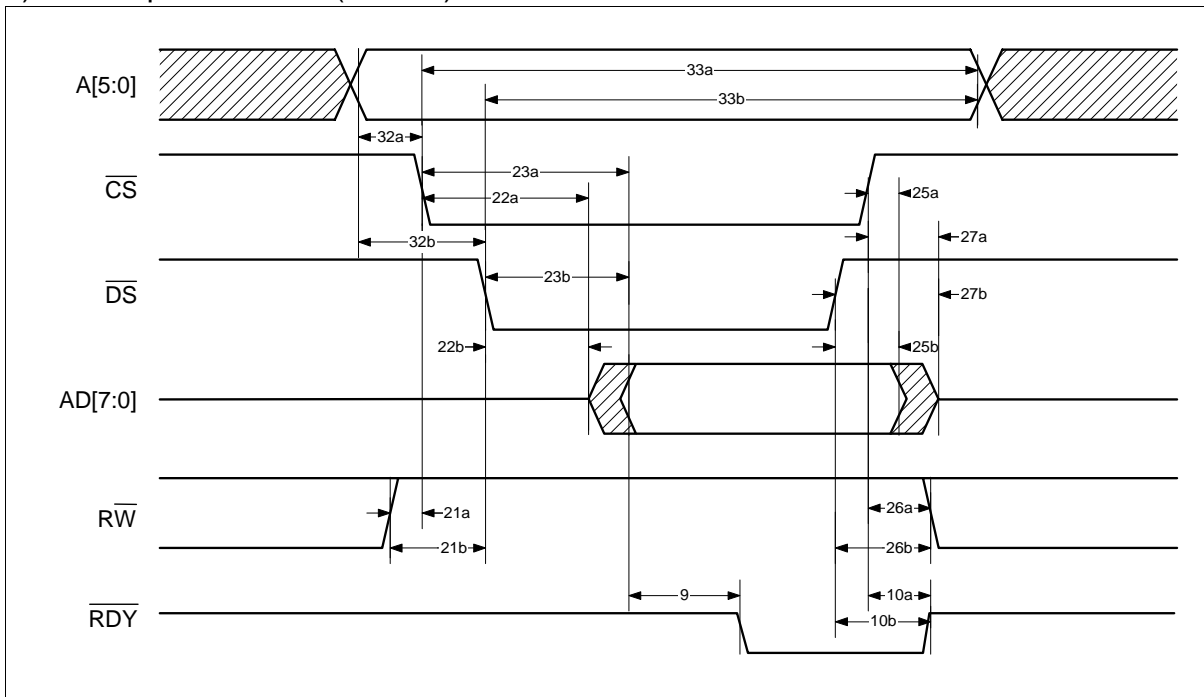


Figure 35 Read Timing in Demultiplexed Motorola Mode (IM0='1', IM1='1')

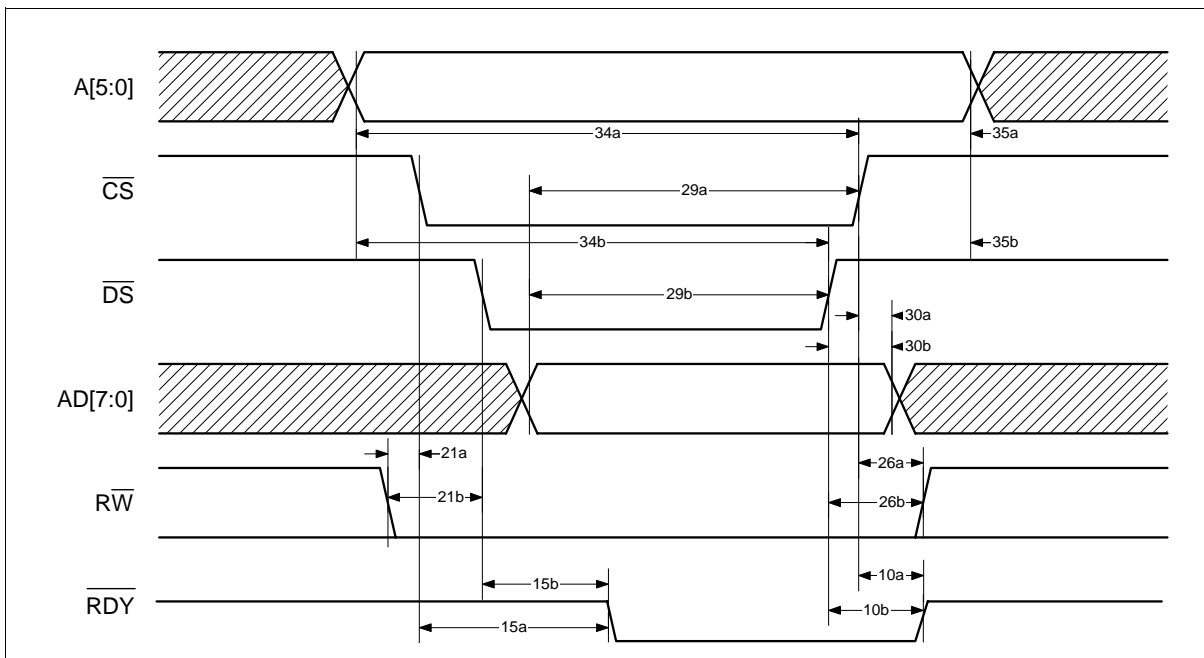


Figure 36 Write Timing in Demultiplexed Motorola Mode (IM0='1', IM1='1')

Table 19 Microprocessor Interface Timing for Figure 29 to Figure 36 (preliminary)

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Address setup before ALE falling edge	15		ns
2	Address hold after ALE falling edge	10		ns
3a	ALE falling edge before CS active if RD asserted	0		ns
3b	ALE falling edge before RD active if CS asserted	0		ns
4a	AD output after CS active if RD asserted	30	90	ns
4b	AD output after RD active if CS asserted	30	90	ns
5a	Read data valid after CS active if RD asserted	30	90	ns
5b	Read data valid after RD active if CS asserted	30	90	ns
6a	ALE rising edge after CS active if RD asserted	100		ns
6b	ALE rising edge after CS active if RD asserted	100		ns
7a	Read data hold after CS inactive if RD asserted	0		ns
7b	Read data hold after RD inactive if CS asserted	0		ns
8a	AD tristate after CS inactive if RD asserted	0	25	ns
8b	AD tristate after RD inactive if CS asserted	0	25	ns
9	RDY asserted after read data valid	15	50	ns
10a	RDY tristate after CS inactive if RD, WR or DS asserted	0	20	ns
10b	RDY tristate after RD, WR or DS inactive if CS asserted	0	20	ns
11a	ALE falling edge before CS rising edge if WR asserted	25		ns

Operational Description

No.	Parameter	Limit Values		Unit
		min.	max.	
11b	ALE falling edge before WR rising edge if CS asserted	25		ns
12a	Write data setup before CS rising edge if WR asserted	25		ns
12b	Write data setup before WR rising edge if CS asserted	25		ns
13a	Write data hold after CS rising edge if WR asserted	20		ns
13b	Write data hold after WR rising edge if CS asserted	20		ns
14a	CS rising edge before ALE falling edge if WR asserted	20		ns
14b	WR rising edge before ALE falling edge if CS asserted	20		ns
15a	RDY asserted after CS active if WR asserted or DS asserted and $\overline{RW}='0'$	30	90	ns
15b	RDY asserted, if CS asserted, after WR active or DS active and $\overline{RW}='0'$	30	90	ns
16a	Address valid before CS active if RD asserted	0		ns
16b	Address valid before RD active if CS asserted	0		ns
17a	Address hold after CS active if RD asserted	100		ns
17b	Address hold after RD active if CS asserted	100		ns
18a	Address setup before CS rising edge if WR asserted	25		ns
18b	Address setup before WR rising edge if CS asserted	25		ns
19a	Address hold after CS rising edge if WR asserted	20		ns
19b	Address hold after WR rising edge if CS asserted	20		ns
20a	ALE falling edge before CS active if DS asserted and $\overline{RW} = '1'$	0		ns

Operational Description

No.	Parameter	Limit Values		Unit
		min.	max.	
20b	ALE falling edge before DS active if CS asserted and $\overline{RW} = '1'$	0		ns
21a	\overline{RW} setup before CS active if DS asserted	10		ns
21b	\overline{RW} setup before DS active if CS asserted	10		ns
22a	\overline{AD} output after CS active if DS asserted and $\overline{RW} = '1'$	30	90	ns
22b	\overline{AD} output after DS active if CS asserted and $\overline{RW} = '1'$	30	90	ns
23a	Read data valid after CS active if DS asserted and $\overline{RW} = '1'$	30	90	ns
23b	Read data valid after DS active if CS asserted and $\overline{RW} = '1'$	30	90	ns
24a	ALE rising edge after CS active if DS asserted and $\overline{RW} = '1'$	100		ns
24b	ALE rising edge after DS active if CS asserted and $\overline{RW} = '1'$	100		ns
25a	Read data hold after CS inactive if DS asserted and $\overline{RW} = '1'$	0		ns
25b	Read data hold after DS inactive if CS asserted and $\overline{RW} = '1'$	0		ns
26a	\overline{RW} hold after CS inactive if DS asserted	10		ns
26b	\overline{RW} hold after DS inactive if CS asserted	10		ns
27a	AD tristate after CS inactive if DS asserted and $\overline{RW} = '1'$	0	25	ns
27b	AD tristate after DS inactive if CS asserted and $\overline{RW} = '1'$	0	25	ns
28a	ALE falling edge before CS rising edge if DS asserted and $\overline{RW} = '0'$	25		ns
28b	ALE falling edge before DS rising edge if CS asserted and $\overline{RW} = '0'$	25		ns
29a	Write data setup before CS rising edge if DS asserted and $\overline{RW} = '0'$	20		ns
29b	Write data setup before DS rising edge if CS asserted and $\overline{RW} = '0'$	20		ns

Operational Description

No.	Parameter	Limit Values		Unit
		min.	max.	
30a	Write data hold <u>after</u> CS rising edge if DS asserted and $\overline{RW} = '0'$	20		ns
30b	Write data hold <u>after</u> DS rising edge if CS asserted and $\overline{RW} = '0'$	20		ns
31a	CS rising edge <u>before</u> ALE falling edge if DS asserted and $\overline{RW} = '0'$	20		ns
31b	DS rising edge <u>before</u> ALE falling edge if CS asserted and $\overline{RW} = '0'$	20		ns
32a	Address valid <u>before</u> CS active if DS asserted and $\overline{RW} = '1'$	0		ns
32b	Address valid <u>before</u> DS active if CS asserted and $\overline{RW} = '1'$	0		ns
33a	Address <u>hold</u> after CS active if DS asserted and $\overline{RW} = '1'$	100		ns
33b	Address <u>hold</u> after DS active if CS asserted and $\overline{RW} = '1'$	100		ns
34a	Address setup <u>before</u> CS rising edge if DS asserted and $\overline{RW} = '0'$	25		ns
34b	Address setup <u>before</u> DS rising edge if CS asserted and $\overline{RW} = '0'$	25		ns
35a	Address hold <u>after</u> CS rising edge if DS asserted and $\overline{RW} = '0'$	20		ns
35b	Address hold <u>after</u> DS rising edge if CS asserted and $\overline{RW} = '0'$	20		ns

4.3.9 JTAG Timing

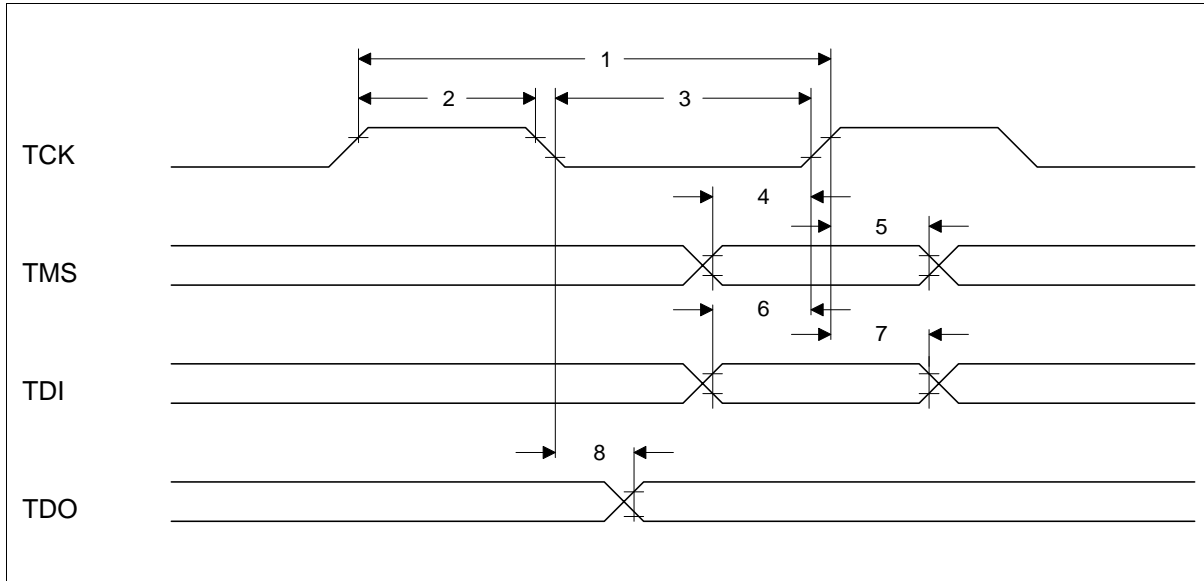


Figure 37 JTAG Boundary Scan Timing

Table 20 JTAG Boundary Scan Timing

No.	Name	Parameter	Limit Values		Unit
			min.	max.	
1	t_tck_period	TCK period	250		ns
2	t_tck_high	TCK high time	80		ns
3	t_tck_low	TCK low time	80		ns
4	t_tms_setup	TMS setup time	40		ns
5	t_tms_hold	TMS hold time	40		ns
6	t_tdi_setup	TDI setup time	40		ns
7	t_tdi_hold	TDI hold time	40		ns
8	t_tck_tdo_fall	TDO valid delay		100	ns

5 Register Overview

The following table lists all registers. The table displays the register name, the abbreviation, the reset value and the read/write mode. The registers are sorted by addresses. Please ask your local Infineon representative to obtain a Data Sheet with detailed register description.

Addr.	Short Name	Full name	R/W	Res. value
00H	NOTEBOOK	Notebook	R/W	00H
01H	WP	Write Protection	W	NOT 95H
02H	WDG1	Watchdog 1	W	
03H	WDG2	Watchdog 2	W	
04H	WDG3	Watchdog 3	W	
05H	UPIO	μ P-I/O-Pin extension	R/W	0FH
06H	PCMCTRL	PCM Bypass and loop Control	W	00H
07H	IRMASK	Interrupt Mask	W	7FH
08H	IRREQ	Interrupt-Request	R	
09H	CLKSTAT	Clock-Status	R	
0AH	RAMBIST	RAMBIST	R/W	00H
0BH	CONFCC	Configuration of Clock Control unit	W	00H
0CH	FSLIPIV	Frame slip safety interval	W	28H
0DH	RIALIGN	Receive input frame alignment	W	00H
0EH	SIALIGN	Send input frame alignment	W	00H
0FH	SOALIGN	Send output frame alignment	W	00H
10H	UCCALIGN	UCC frame alignment, write protected	W	00H
11H	PHALIGN	Bit Phase alignment for RI, SI, SO and UCC	W	00H
12H	CONFSCU1	Configuration of speech control unit 1	W	69H
13H	CONFSCU2	Configuration of speech control unit 2	W	97H
14H	CONFSCU3	Configuration of speech control unit 3	W	A4H
15H	CONFSCU4	Configuration of speech control unit 4	W	A7H
16H	CONFSCU5	Configuration of speech control unit 5	W	84H
17H	CONFSCU6	Configuration of speech control unit 6	W	2AH

Register Overview

Addr.	Short Name	Full name	R/W	Res. value
18H	CONFSCU7	Configuration of speech control unit 7	W	8AH
19H	CONFSCU8	Configuration of speech control unit 8	W	EEH
1AH	CONFSCU9	Configuration of speech control unit 9	W	44H
1BH	CONFSCU10	Configuration of speech control unit 10	W	C0H
1CH	CONFPSD	Configuration of 2100 Hz tone phase shift detector	W	43H
1DH	CONFSS7	Configuration of SS7 continuity check tone detection	W	00H
1EH	MONSIL	Monitor send input level	R	
1FH	MONSOL	Monitor send output level	R	
20H	MONRIL	Monitor of receive input level	R	
21H	MONOFSI	Monitor offset in send path input	R	
22H	MONOFSO	Monitor offset in send path output	R	
23H	MONAEL	Monitor artificial echo level	R	
24H	MONBNL	Monitor background noise level	R	
25H	MONERL	Monitor Echo return loss	R	
26H	MONCL	Monitor combined loss without NLP	R	
27H	MONNLPThL	Monitor NLP threshold level	R	
28H	MONOCDT	Monitor overcompensation and double talk hang-over time	R	
29H	MONSI	Monitor send input signal (A-/μ-Law encoded)	R	
2AH	MONSO	Monitor send output signal (A-/μ-Law encoded)	R	
2BH	MONRI	Monitor of receive input signal (A-/μ-Law encoded)	R	
2CH	MONSTAT1	Monitor of internal/external control states 1	R	
2DH	MONSTAT2	Monitor of internal/external control states 2	R	
2EH	MONSTAT3	Monitor of internal/external control states 3	R	

Register Overview

Addr.	Short Name	Full name	R/W	Res. value
2FH	CTRLTSMON	Control of TS to be monitored	W	00H
30H	CONFPCM	Global Configuration of PCM outputs	W	03H
31H	CONFTS16	Configuration of TS16 CAS Evaluation for E1 frames	W	12H
32H	CONFIDLE	Configuration of IDLE Detection	W	1DH
33H	IDLEMASK	IDLE detection bit compare MASK	W	00H
34H	IDLEPATTERN	Idlepattern	W	55H
35H	ATE	Address of Test-channel	W	00H
36H	SFATSES	Super frame alarm and requested timeslot en/disable status	R	
37H	TESTTIMER	μ P Test and Timer	W	00H
38H	CTRLTEST	Control of test channel	W	00H
39H	TSGSPP	Test signal generator for send path pattern	W	55H
3AH	TSGRPP	Test signal generator for receive path pattern	W	55H
3BH	HTIM	High-Byte for Timer	W	00H
3CH	LTIM	Low-Byte for Timer	W	00H
3DH	SOTP	Send path output test pattern	R	
3EH	TESTSTAT	Background test status signals	R	
3FH	CONFLAW	Global configuration of PCM encoding law	W	00H
40H	CHCTRL0	Individual channel control 0	W	00H
41H	CHCTRL1	Individual channel control 1	W	00H
42H	CHCTRL2	Individual channel control 2	W	00H
43H	CHCTRL3	Individual channel control 3	W	00H
44H	CHCTRL4	Individual channel control 4	W	00H
45H	CHCTRL5	Individual channel control 5	W	00H
46H	CHCTRL6	Individual channel control 6	W	00H
47H	CHCTRL7	Individual channel control 7	W	00H
48H	CHCTRL8	Individual channel control 8	W	00H
49H	CHCTRL9	Individual channel control 9	W	00H

Register Overview

Addr.	Short Name	Full name	R/W	Res. value
4AH	CHCTRL10	Individual channel control 10	W	00H
4BH	CHCTRL11	Individual channel control 11	W	00H
4CH	CHCTRL12	Individual channel control 12	W	00H
4DH	CHCTRL13	Individual channel control 13	W	00H
4EH	CHCTRL14	Individual channel control 14	W	00H
4FH	CHCTRL15	Individual channel control 15	W	00H
50H	CHCTRL16	Individual channel control 16	W	00H
51H	CHCTRL17	Individual channel control 17	W	00H
52H	CHCTRL18	Individual channel control 18	W	00H
53H	CHCTRL19	Individual channel control 19	W	00H
54H	CHCTRL20	Individual channel control 20	W	00H
55H	CHCTRL21	Individual channel control 21	W	00H
56H	CHCTRL22	Individual channel control 22	W	00H
57H	CHCTRL23	Individual channel control 23	W	00H
58H	CHCTRL24	Individual channel control 24	W	00H
59H	CHCTRL25	Individual channel control 25	W	00H
5AH	CHCTRL26	Individual channel control 26	W	00H
5BH	CHCTRL27	Individual channel control 27	W	00H
5CH	CHCTRL28	Individual channel control 28	W	00H
5DH	CHCTRL29	Individual channel control 29	W	00H
5EH	CHCTRL30	Individual channel control 30	W	00H
5FH	CHCTRL31	Individual channel control 31	W	00H
60H	CONFUCC	Configuration of UCC Interface	W	00H
61H	UCCMFR	UCC Multiframe Alignment	W	00H
62H	UCCFRS	Selection of the special UCC Frame FRS	W	00H
63H	WRUCC	Write/Read UCC I	W	00H
64H	DORAM	Data Output RAM	W	00H
65H	IMASKFRS	Interrupt Mask for the special UCC frame FRS	W	00H

Register Overview

Addr.	Short Name	Full name	R/W	Res. value
66H	IMASKFRN	Interrupt Mask for channel individual UCC frames (FRN)	W	00H
67H	DIRAM	requested Data Input RAM value	R	
68H	UCCOLD	Changed UCC input data old value	R	
69H	UCCNEW	Changed UCC input data new value	R	
6AH	UCCSTAT	UCC status	R	
6BH	SCMASK	Serial Control Interface Mask	W	3FH
6CH	CONFFLEX SCTR	Configuration of the flexible serial control signal	W	00H
6DH	CONFFLEXUCC	Configuration of the flexible UCC control bit (FX-Bit)	W	00H
6EH	STATUS	Status	R	
6FH	CONFFLEXMON	Configuration of Flexible Monitor Signals	W	FEH
70H	ASTOC	AFI Saw-Tooth and Offset Characteristic	W	00H
71H	AFSTC	AFI Filter Spring Timer Configuration	W	44H
72H	AEEPDP	AFI End Echo Path Delay	W	0FH
73H	AVDDI	AFI Voice Detection, Detection Intervals	W	77H
74H	AVDHG	AFI Voice Detection, Hysteresis and Gap	W	74H
75H	AVDCI	AFI Voice Detection Count Init	W	85H
76H	VDFCTRL	Voice Detection Freeze Control	W	B4H
77H	ATMAT	AFI Turbo Mode Activation Threshold	W	08H
78H	AACSC	AFI Auxiliary Coefficient Supervision Configuration	W	00H
79H	ACONF	AFI Configuration	W	10H
7AH	AFCMC	AFI Filter Coefficients Monitoring Control	W	00H
7BH	AFCD1	AFI Filter Coefficient Data 1	R	
7CH	AFCD2	AFI Filter Coefficient Data 2	R	
7DH	AFCD3	AFI Filter Coefficient Data 3	R	

6 SIDEC Performance

This section describes the preliminary performance of the SIDEC. The measurements are based on the preliminary emulation results. The test, signals and methods are described in ITU G.168. For the measurements a regular analog hybrid with 6 dB echo return loss is used. No significant difference for high dispersion hybrids is expected, since the SIDEC evaluates not only a "echo window" but the complete echo path delay time.

6.1 Test No.1 - Steady state residual and returned echo level test

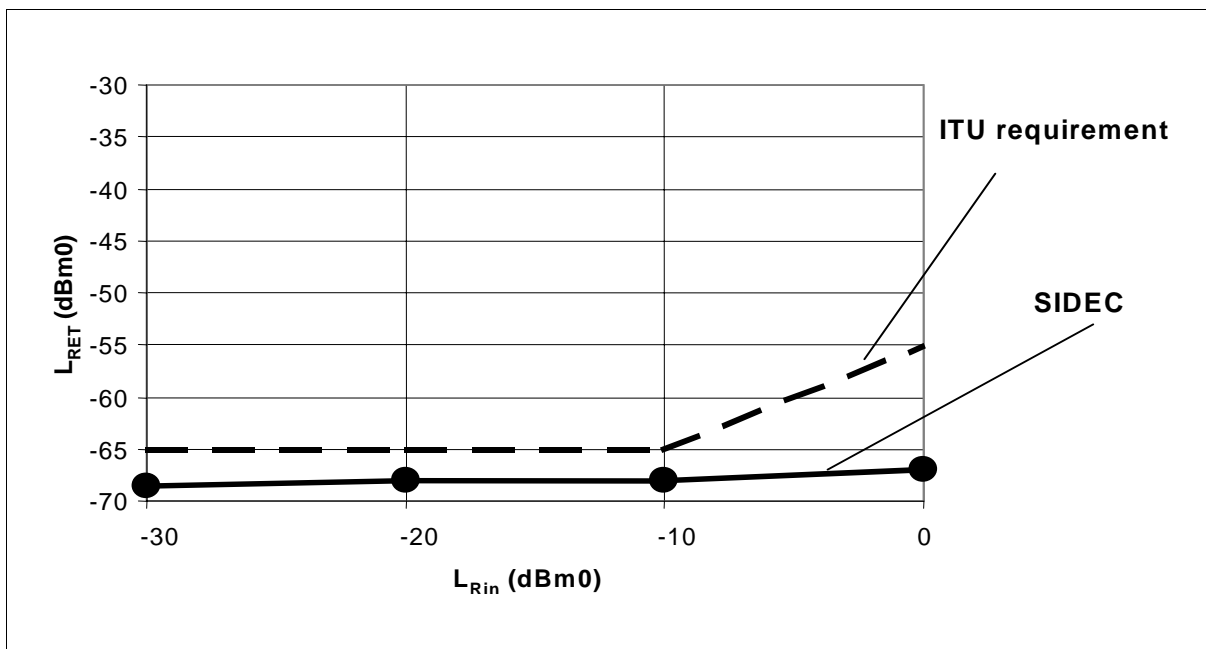


Figure 38 SIDEC steady state behavior with NLP enabled

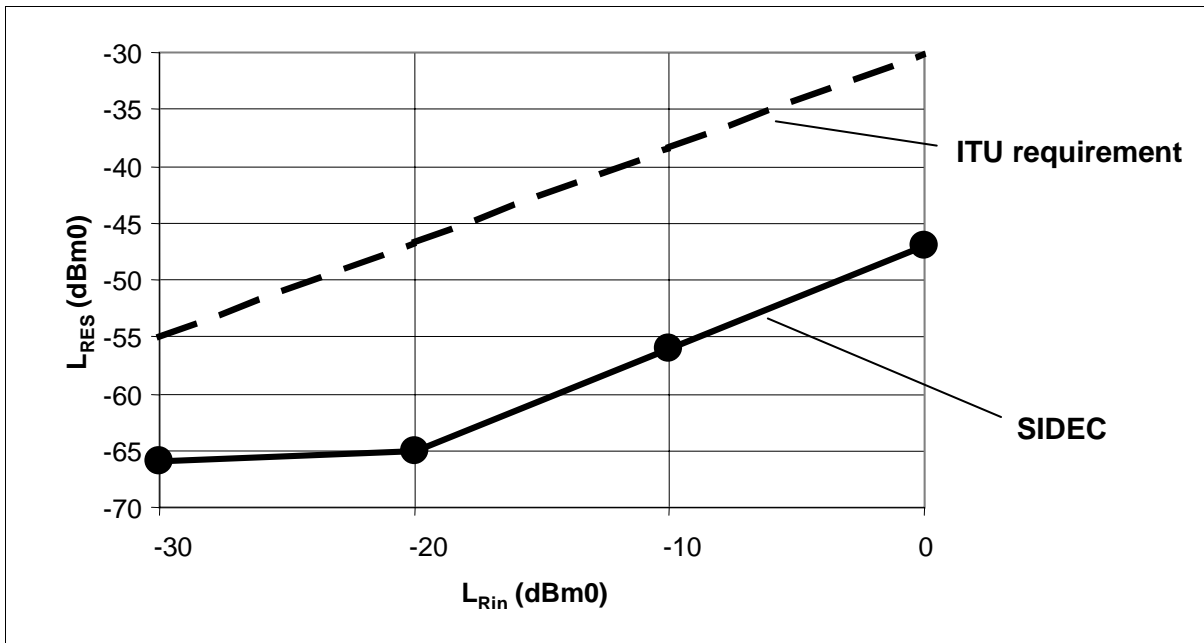


Figure 39 SIDEC steady state behavior with NLP disabled

6.2 Test No. 2 - Convergence and steady state residual and returned echo level test

6.2.1 Test 2A: Convergence test with NLP enabled

Receive Level R_{in}	Time until A_{COM} =			
	16 dB (CONV)		Boundary value of Figure 38	
	Requirement ITU G.168	measured value	Requirement ITU G.168	measured value
0 dBm0	< 1 s	200 ms	< 1 s	670 ms
-10 dBm0	< 1 s	150 ms	< 1 s	520 ms
-20 dBm0	< 1 s	150 ms	< 1 s	410 ms
-30 dBm0	< 1 s	150 ms	< 1 s	450 ms

6.2.2 Test 2B: Convergence test with NLP disabled

Receive Level R_{in}	Time until A_{COM} =			
	16 dB (CONV)		Boundary value of Figure 39	
	Requirement ITU G.168	measured value	Requirement ITU G.168	measured value
0 dBm0	< 1 s	200 ms	< 10 s	520 ms
-10 dBm0	< 1 s	200 ms	< 10 s	600 ms
-20 dBm0	< 1 s	400 ms	< 10 s	1300 ms
-30 dBm0	< 1 s	400 ms	< 10 s	1200 ms

6.2.3 Test 2C: Convergence test in the presence of background noise

For this test the NLP is enabled and the convergence time is $t_d = 1$ s.

Receive Level R_{in}	Transmit Noise Level	Residual output level L_{RES}	
		Requirement ITU G.168	measured value
0 dBm0	-30 dBm0	-30 dBm0	-67 dBm0
-10 dBm0	-30 dBm0	-30 dBm0	-66 dBm0
-20 dBm0	-35 dBm0	-35 dBm0	-66 dBm0
-25 dBm0	-40 dBm0	-40 dBm0	-64 dBm0

6.3 Test No. 3 - Performance under conditions of double talk

6.3.1 Test 3A: Double talk test with low near end levels

For this test the NLP is disabled and the convergence time is $t_d = 5$ s.

Receive Level R_{in}	Transmit Noise Level	Residual output level L_{RES}	
		Requirement ITU G.168	measured value
0 dBm0	-15 dBm0	< -15 dBm0	-31 dBm0
-10 dBm0	-25 dBm0	< -25 dBm0	-43 dBm0
-20 dBm0	-35 dBm0	< -35 dBm0	-56 dBm0
-25 dBm0	-40 dBm0	< -40 dBm0	-56 dBm0

6.3.2 Test 3B: Double talk test with high near end levels

For this test the NLP is disabled and the testtime is > 5 s.

Receive Level R_{in}	Transmit Noise Level	Residual output level L_{RES}	
		Requirement ITU G.168	measured value
0 dBm0	0 dBm0	< -30 dBm0	-51 dBm0
-10 dBm0	-10 dBm0	< -38 dBm0	-55 dBm0
-20 dBm0	-20 dBm0	< -47 dBm0	-62 dBm0
-25 dBm0	-30 dBm0	< -55 dBm0	-66 dBm0

6.3.3 Test 3C: Double talk under simulated conversion

This test is under study and most values are not defined

6.4 Test No. 4 - Leak rate test

During this test the H-Register is frozen. Therefore, no divergence occurs.

6.5 Infinite return loss convergence test

The previous echo return loss is 6 dB at an analog hybrid. The NLP is disabled and the measurement is made 500 ms after interrupting the end echo path.

Receive Level R_{in}	Residual output level L_{RES}	
	Requirement ITU G.168	measured value
0 dBm0	< TBD dBm0	-76 dBm0
-10 dBm0	< TBD dBm0	-76 dBm0
-20 dBm0	< TBD dBm0	-67 dBm0
-25 dBm0	< TBD dBm0	-67 dBm0

6.6 Non divergence on narrow band signals

This test is under study and the most values are not defined.

6.7 Stability Test

Receive Level R_{in}	Residual output level L_{RES}	
	Requirement ITU G.168	measured value
+3 dBm0	< -27.5 dBm0	-28 dBm0
0 dBm0	< -30 dBm0	-31 dBm0
-10 dBm0	< -38 dBm0	-41 dBm0
-20 dBm0	< -47 dBm0	-51 dBm0
-30 dBm0	< -55 dBm0	- 61 dBm0

6.8 Test No. 8 - Non convergence of the canceller on specific ITU-T No. 5, 6 and 7 in band signaling and continuity check tones

The SIDEC incorporate a 2010 Hz tone detector to allow a continuity check in System 6 and 7. In many applications a disabling control via the switch is possible. In this case this function has to be switched off (reset value, Register CONFSS7 = 00H).

Operating level / Non operating level:	> -31dBm0 / < -34dBm0
Operating frequency:	1968Hz...2032Hz
Operating time for disabling	12ms + guard time adjusted in BYNR7[3:0]
Operating time for H-Register-Reset	12ms + guard time adjusted in D!SNR7[3:0]
None operating frequency:	0...1945 and 2055Hz...4000Hz
Release time:	10ms

6.9 Test No. 9 - Comfort noise test

The SIDEC is fitted with a circuit which is in compliance with this requirement, but most subscribers prefer the solution which limit the send in signal (noise from the near end + echo) to the noise level which was measured before (Reset value).

6.10 Test No. 10 - Cancellor operation on the calling/caller station side

These tests are checked and are "OK"

Features of the 2100Hz tone disabler:

Operating frequency	2065 Hz - 2140 Hz
Not operating frequency	< 2000 Hz, > 2180 Hz
Holding Band	390 Hz - 3000 Hz
Operating level / Not operating level	> -31 dBm0 / < -34 dBm0
Operate time / Not operating time	> 260 ms / < 200 ms
Hold time / Release time	> 210 ms / < 270 ms
Guard band noise level to inhibit the operating	> signal level
Maximum noise level for operation	< signal level - 5 dB
False operation due to speech/data signals	< 10/100h

Features of the phase reversal enhancement:

Operating frequency	2010Hz +/- 21Hz
Operating phase / Not operating phase	> +/-155° / < +/- 110°

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit	
Ambient temperature under bias	PEB PEF	T_A T_A	0 to 70 – 40 to 85	°C °C
Storage temperature		T_{stg}	– 65 to 125	°C
IC supply voltage		V_{DD}	0 to 3.6	V
Voltage on any functional pin (not V_{DD} and not V_{SS}) with respect to ground		V_S	-0.4 to 5.5	V
ESD robustness ¹⁾ HBM: 1.5 kΩ, 100 pF		$V_{ESD,HBM}$	2000	V

¹⁾ According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{DD}	3.0	3.6	V	
Ground	V_{SS}	0	0	V	

Note: In the operating range, the functions given in the circuit description are fulfilled.

7.3 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	-0.4	0.8	V	1)
Input high voltage	V_{IH}	2.0	5.5	V	
Output low voltage	V_{OL}		0.45	V	$I_{OL} = 4 \text{ mA}$ ²⁾ $I_{OL} = 2.5 \text{ mA}$ ³⁾
Output high voltage	V_{OH}	2.4		V	$I_{OH} = -1.0 \text{ mA}$
Avg. power supply current	$I_{CC} (AV)$		300	mA	$V_{DD} = 3.3 \text{ V}$, $T_A = 25 \text{ }^\circ\text{C}$:
Input leakage current	I_{IL}		5	μA	$V_{DD} = 3.3 \text{ V}$, GND = 0 V; all other pins are floating; $V_{IN} = 0 \text{ V}$,
Output leakage current	I_{OZ}		5	μA	$V_{DD} = 3.3 \text{ V}$, GND = 0 V; $V_{OUT} = 0 \text{ V}$,

1) Permanent exposure to negative input voltages may result in minor degradation of lifetime

2) Apply to the following O or I/O pins:

UPIO0, UPIO1, UPIO2, UPIO3, AD[0:6], $\overline{\text{RDY}}$, $\overline{\text{UPRES}}$, $\overline{\text{INT}}$, RO, SO, TMFBO, CLK40, SYNCO, SCLKO, SDECO, UCCO, TUCCO

3) Apply to all the I/O and O pins that do not appear in the list in note 2))

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25^\circ\text{C}$ and the given supply voltage.

7.4 AC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{il}		0.45	V	1)
Input high voltage	V_{ih}	2.4		V	

Electrical Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Output low voltage	V_{ol}		0.8	V	$I_{ol} = 4 \text{ mA}$ ²⁾ $I_{ol} = 2.5 \text{ mA}$ ³⁾
Output high voltage	V_{oh}	2.0		V	$I_{ol} = -1.0 \text{ mA}$

1) Permanent exposure to negative input voltages may result in minor degradation of lifetime

2) Apply to the following O or I/O pins:

UPIO0, UPIO1, UPIO2, UPIO3, AD[0:6], $\overline{\text{RDY}}$, $\overline{\text{UPRES}}$, $\overline{\text{UPRES}}$, $\overline{\text{INT}}$, RO, SO, TMFBO, CLK40, SYNC0, SCLK0, SDECO, UCCO, $\overline{\text{TUCCO}}$

3) Apply to all the I/O and O pins that do not appear in the list in note 2))

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25^\circ\text{C}$ and the given supply voltage.

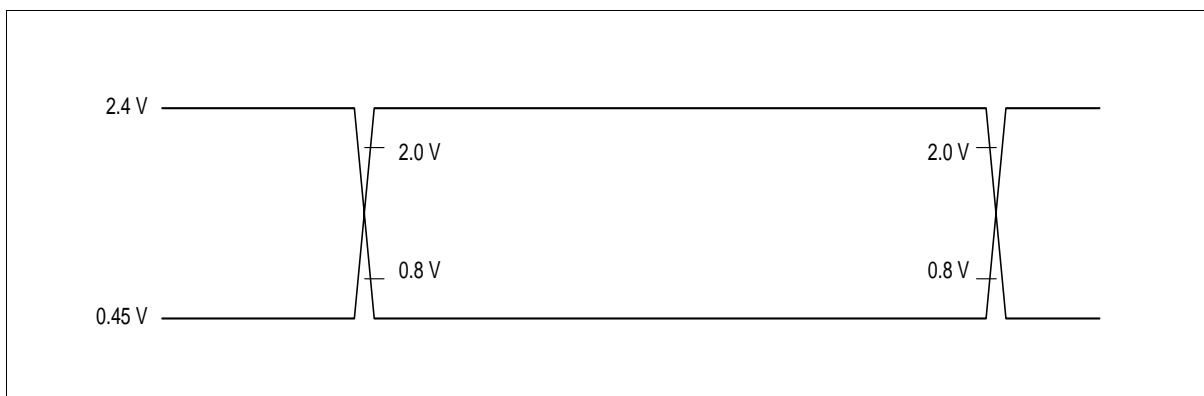
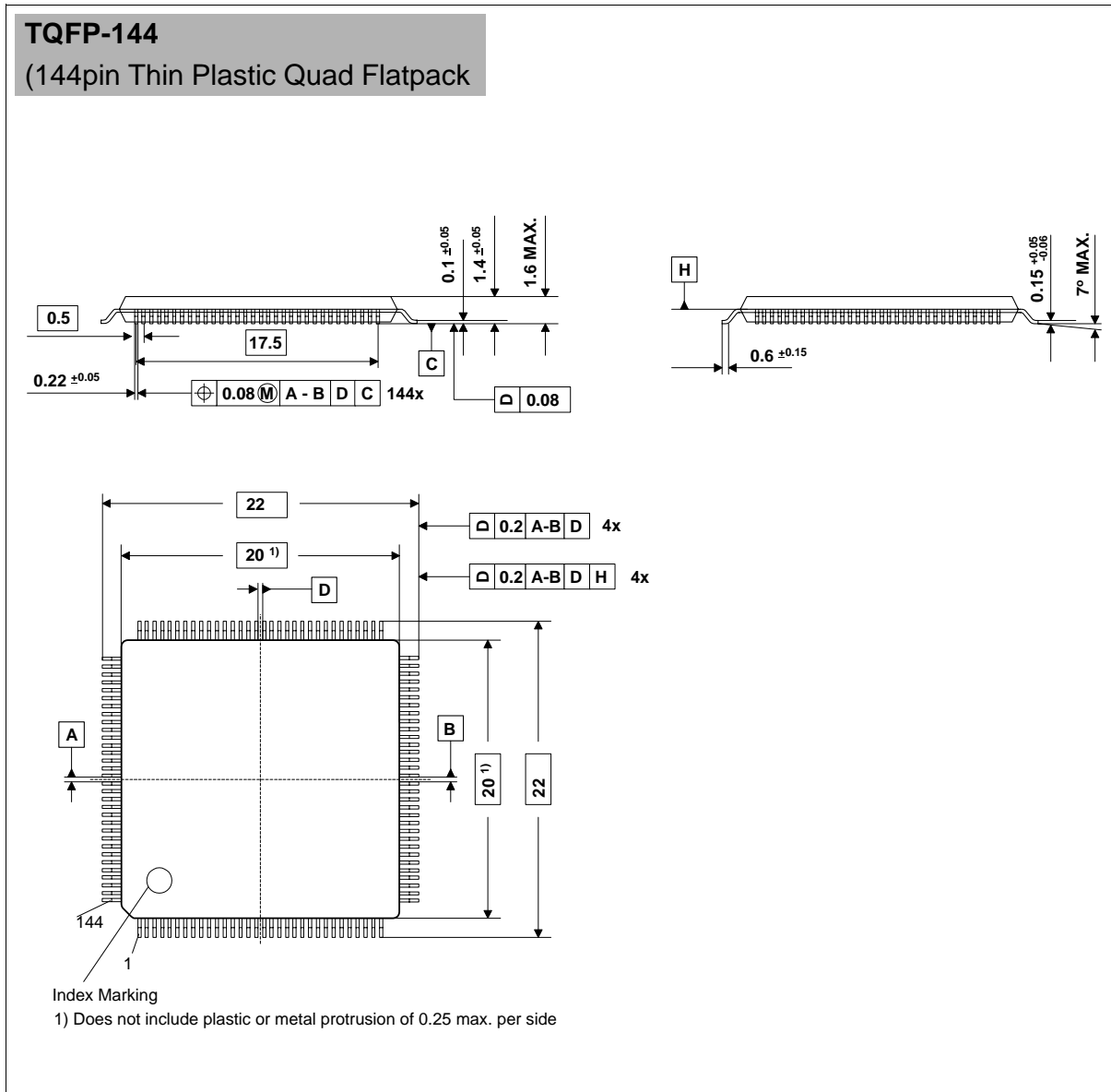


Figure 40 Input/Output Waveforms for AC-Tests

7.5 Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Clock input capacitance	C_{XIN}		10	pF	$f_C = 1 \text{ MHz}$ The pins, which are not under test, are connected to GND
Clock output capacitance	C_{XOUT}		10	pF	
Input capacitance	C_{IN}		10	pF	
Output capacitance	C_{OUT}		10	pF	

8 Package Outlines



Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

9 Glossary

acoustic echo

Acoustic echoes consist of reflected signals caused by acoustic environments, e.g. hands-free phones which are connected with a 2-wire circuit to a hybrid. An echo path is introduced by the acoustic path from earphone to microphone.

combined loss (A_{COM})

The sum of echo return loss, echo return loss enhancement and non-linear processing loss (if present). This loss relates L_{Rin} to L_{RET} by:

$$L_{\text{RET}} = L_{\text{Rin}} - A_{\text{COM}}, \text{ where:}$$
$$A_{\text{COM}} = A_{\text{ECHO}} + A_{\text{CANC}} + A_{\text{NLP}}$$

comfort noise

Insertion of pseudo-random noise during the silent interval when the NLP operates or allowance of some of the background or idle channel noise to pass through the NLP in order to prevent the annoyance of intervals of speech with background noise followed by intervals of silence.

composite echo

Composite echoes consist of the electric echoes and acoustic echoes caused by reflected signals at hybrids and acoustic environments, e.g. hands-free telephones.

convergence

The process of developing a model of the echo path which will be used in the echo estimator to produce the estimate of the circuit echo.

convergence time

For a defined echo path, the interval between the instant a defined test signal is applied to the receive-in port of an echo canceller with the estimated echo path impulse response initially set to zero, and the instant the returned echo level at the send-out port reaches a defined level.

echo canceller

A voice-operated device placed in the 4-wire portion of a circuit and used for reducing near-end echo present on the send path by subtracting an estimation of that echo from the near-end echo (see **Figure 41**)

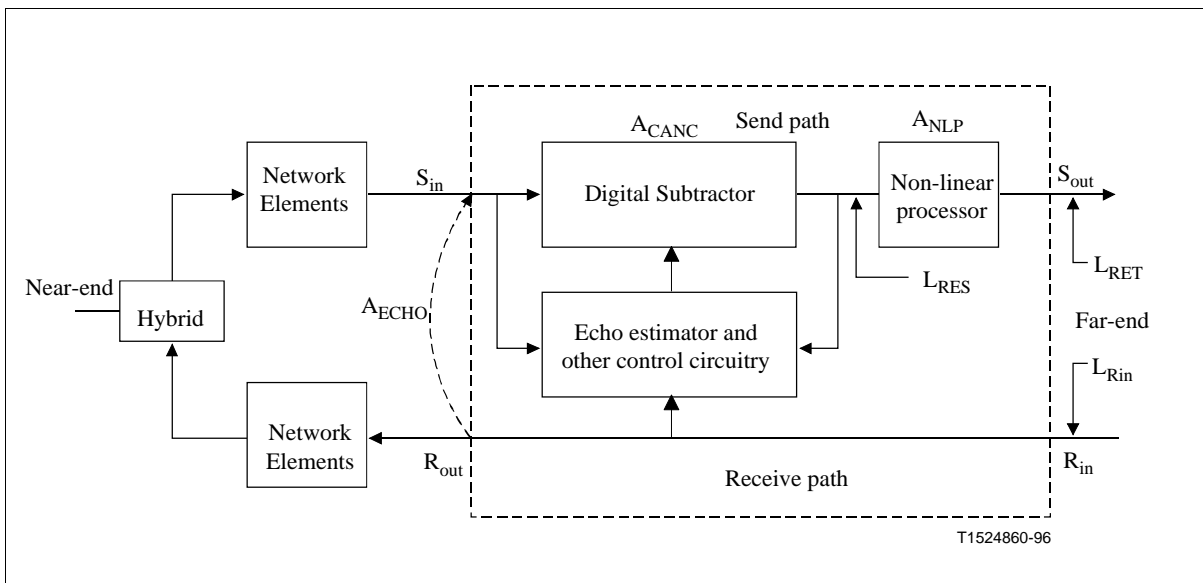


Figure 41 Location of levels and loss of an echo canceller

echo path

The transmission path between R_{out} and S_{in} of an echo canceller. This term is intended to describe the signal path of the echo.

echo path capacity

The maximum echo path delay for which an echo canceller is designed to operate.

echo path delay (t_d)

The delay from the R_{out} port to the S_{in} port due to the delays inherent in the echo path transmission facilities including dispersion time due to the network elements. In case of multiple echo paths, all delays and dispersions of any individual echo path are included. The dispersion time, which varies with different networks, is required to accommodate the band-limiting, and hybrid transit effects.

echo return loss (ERL) (A_{ECHO})

The attenuation of a signal from the receive-out port (R_{out}) to the send-in port (S_{in}) of an echo canceller, due to transmission and hybrid loss, i.e. the loss in the (near-end) echo path.

echo return loss enhancement (ERLE) (A_{CANC})

The attenuation of the echo signal as it passes through the send path of an echo canceller. This definition specifically excludes any non-linear processing on the output of the canceller to provide for further attenuation.

electric echo

Electric echoes consist of reflected signals caused by the near-end impedance mismatch, e.g. at a 2-wire/4-wire conversion unit (hybrid).

far end

The side of an echo canceller which does not contain the echo path on which the echo canceller is intended to operate.

H register

The register within the echo canceller which stores the impulse response model of the echo path.

leak time

The interval between the instant a test signal is removed from the receive-in port of a fully-converged echo canceller and the instant the echo path model in the echo canceller changes such that, when a test signal is reapplied to R_{in} with the convergence circuitry inhibited, the returned echo is at a defined level.

This definition refers to echo cancellers employing, for example, leaky integrators in the convergence circuitry.

near-end

The side of an echo canceller which contains the echo path on which the echo canceller is intended to operate. This includes all transmission facilities and equipment (including the hybrid and terminating telephone set) which is included in the echo path.

non-linear processor (NLP)

A device having a defined suppression threshold level and in which:

- a) signals having a level detected as being below the threshold are suppressed; and
- b) signals having a level detected as being above the threshold are passed although the signal may be distorted.

NOTE 1 – The precise operation of a NLP depends upon the detection and control algorithm used.

NOTE 2 – An example of a NLP is an analogue center clipper in which all signal levels below a defined threshold are forced to some minimum value.

non-linear processing loss (A_{NLP})

Additional attenuation of residual echo level by a NLP placed in the send path of an echo canceller.

pure delay (t_r)

The delay from the R_{out} port to the S_{in} port due to the delays inherent in the near-end echo path transmission facilities, not including dispersion time due to the network elements. In this case, the transit time directly across the hybrid is assumed to be zero (see **Figure 42**).

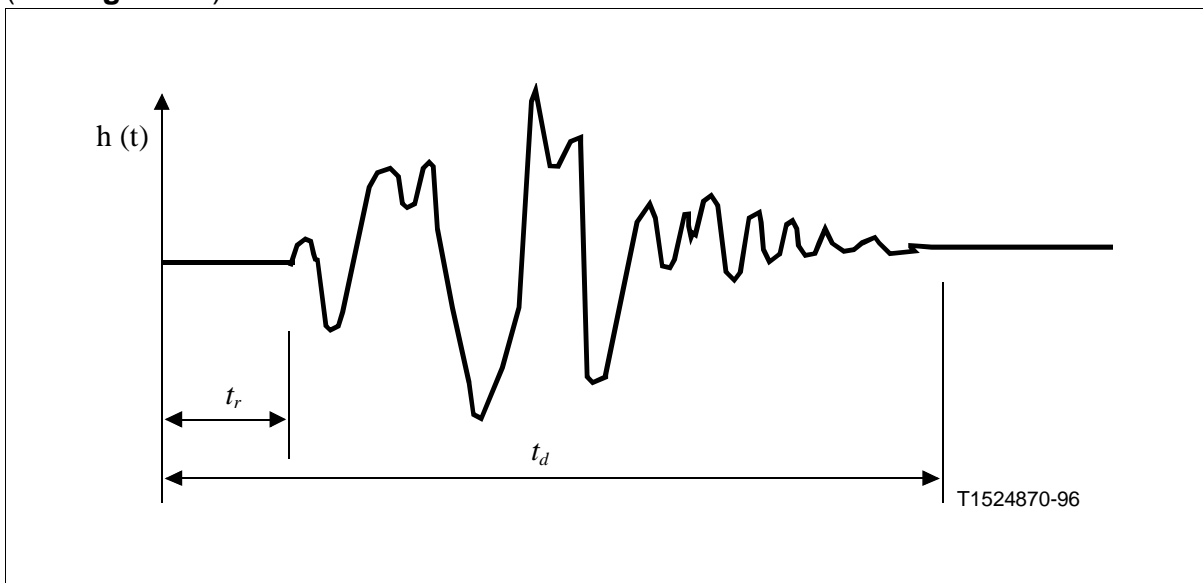


Figure 42 Example of an impulse response of an echo path

residual echo level (L_{RES})

The level of the echo signal which remains at the send-out port of an operating echo canceller after imperfect cancellation of the circuit echo. It is related to the receive-in signal L_{Rin} by:

$$L_{RES} = L_{RIN} - A_{ECHO} - A_{CANC}$$

Any non-linear processing is not included.

returned echo level (L_{RET})

The level of the signal at the send-out port of an operating echo canceller which will be returned to the talker. The attenuation of a NLP is included, if one is normally present. L_{RET} is related to L_{Rin} by:

$$L_{\text{RET}} = L_{\text{RIN}} - (A_{\text{ECHO}} + A_{\text{CANC}} + A_{\text{NLP}})$$

If non-linear processing is not present, note that $L_{\text{RES}} = L_{\text{RET}}$.

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