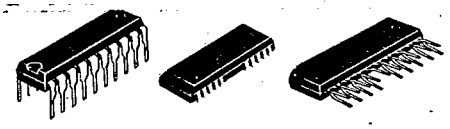


M5M44C258P, J, L-10, -12, -15

T-46-23-17

STATIC CLOUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

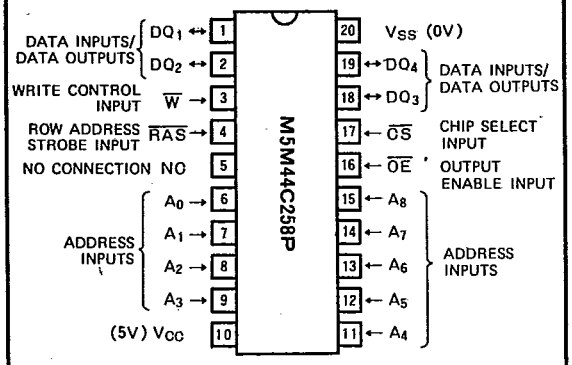
Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access time (max. ns)	$\overline{OE}$ access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ.mW)
M5M44C258 P/J/L-10	100	25	50	25	190	300
M5M44C258 P/J/L-12	120	30	55	30	220	250
M5M44C258 P/J/L-15	150	40	70	40	260	200

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low standby power dissipation
  5.5mW (Max) . . . . . CMOS Input level
- Low operating power dissipation
  M5M44C258P, J, L-10 . . . . . 413mW (Max)
  M5M44C258P, J, L-12 . . . . . 358mW (Max)
  M5M44C258P, J, L-15 . . . . . 303mW (Max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and $\overline{OE}$ control output buffer impedance
- Read-Modify-write, $\overline{RAS}$-only refresh, Static column mode capabilities
- $\overline{CS}$ before $\overline{RAS}$ refresh mode capability
- $\overline{CS}$ controlled output allows hidden refresh
- Wide $\overline{RAS}$ pulse width for Static column mode . . . . . 50μs max

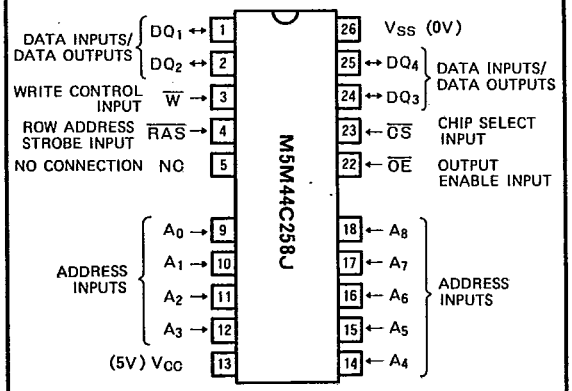
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

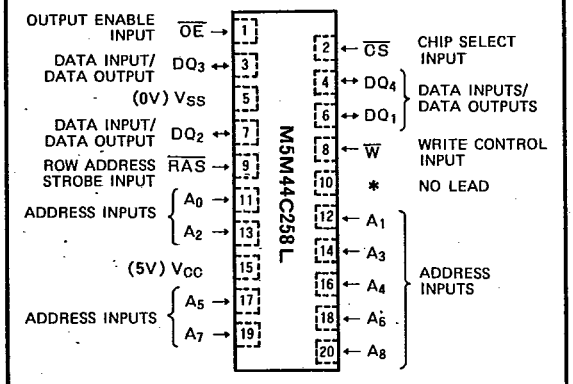
PIN CONFIGURATION (TOP VIEW)



Outline 20P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L (ZIP)

MITSUBISHI ELECTRIC

STATIC CLOUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

T-46-23-17

FUNCTION

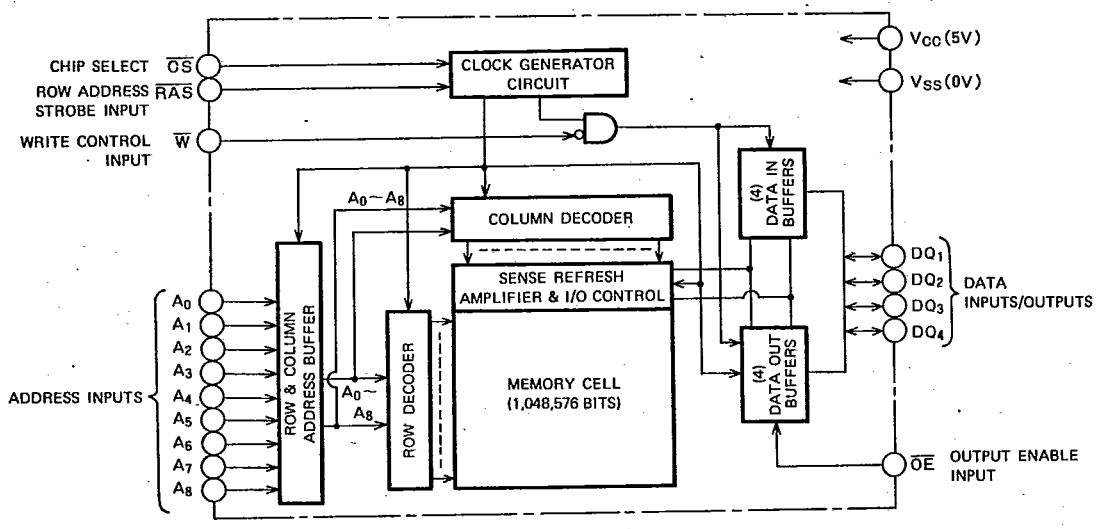
The M5M44C258P, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., static column mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Note.
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open
Static column mode is identical except early write.

BLOCK DIAGRAM



STATIC CLOUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

T-46-23-17

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−2mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IH}≦6.5V, Other inputs pins =0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M44C258-10	$\overline{RAS}$, $\overline{OS}$ cycling $t_{RC}=t_{WC}$= min, output open			75	mA
		M5M44C258-12				65	
		M5M44C258-15				55	
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}=\overline{CS}=V_{IH}$, output open			2	mA
			$\overline{RAS}=\overline{CS}=\overline{OE}$≧$V_{CC}$−0.5, output open			1	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M44C258-10	$\overline{RAS}$ cycling, $\overline{CS}=V_{IH}$ t_{RC}= min, output open			75	mA
		M5M44C258-12				65	
		M5M44C258-15				55	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44C258-10	$\overline{CS}$ before $\overline{RAS}$ refresh cycling t_{RC}= min, output open			75	mA
		M5M44C258-12				65	
		M5M44C258-15				55	
$I_{CC7(AV)}$	Average supply current from V_{CC}, Static Column mode (Note 3, 4)	M5M44C258-10	$\overline{RAS}=V_{IL}$, Column address cycling t_{SC}= min, output open			65	mA
		M5M44C258-12				55	
		M5M44C258-15				45	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, and $I_{CC6(AV)}$ and $I_{CC7(AV)}$ are dependent on cycle rate, maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC7(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	$V_I=V_{SS}$ f=1MHz V_i=25mVrms			6	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CS})}$	Input capacitance, $\overline{CS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance data ports				7	pF

SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			M5M44C258-10		M5M44C258-12		M5M44C258-15		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CS}$	(Note 6, 7)		25		30		40	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		100		120		150	ns
t_{CAA}	Column Address access time	(Note 6, 9)		50		55		70	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		25		30		40	ns
t_{WRA}	Access time from $\overline{W}$ high	(Note 6)		60		65		80	ns
t_{OFF}	Output disable time after $\overline{CS}$ high	(Note 10)	0	20	0	25	0	30	ns
t_{CLZ}	Output low impedance time from $\overline{CS}$ low	(Note 6)	5		5		5		ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 10)	0	20	0	25	0	30	ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assume that $t_{RCD} \geqq t_{RCD(max)}$, $t_{RAD} \leqq t_{RAD(max)}$.
8: Assume that $t_{RCD} \leqq t_{RCD(max)}$, $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than $t_{RCD(max)}$ or $t_{RAD(max)}$ then t_{RAC} will increase by the amount that t_{RCD} or t_{RAD} exceeds $t_{RCD(max)}$ or $t_{RAD(max)}$.
9: Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.
10: $t_{OFF(max)}$ and $t_{dis(OE)(max)}$ define the time at which the output achieves the high impedance state ($|I_{OUT}| \leqq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Static Column Cycles)

(T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, See notes 11, 12)

Symbol	Parameter		Limits						Unit
			M5M44C258-10		M5M44C258-12		M5M44C258-15		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		80		90		100		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CS}$ low	(Note 13)	20	75	25	90	30	110	ns
t_{CRP}	Delay time, $\overline{CS}$ high to $\overline{RAS}$ low	(Note 14)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width	(Note 15)	25		30		35		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	50	20	65	25	80	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CS}$ low		0		0		0		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		20		ns
t_{CAH}	Column address hold time after $\overline{CS}$ low or $\overline{W}$ low		20		20		25		ns
t_T	Transition time	(Note 17)	3	50	3	50	3	50	ns

Note 11: The timing requirements are assumed t_T = 5ns.
12: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
13: $t_{RCD(max)}$ is specified as a reference point only; If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is $t_{RCD} + t_{CAC}$. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH} + 2t_T + t_{ASC}$.
14: t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CS}$ cycles.
15: $t_{CPN(min)}$ is specified as $t_{CPN(min)} = t_{RCD(min)} + t_{CRP(min)} - t_T$ except for t_{CP} of static column mode cycle.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle.
17: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44C258-10		M5M44C258-12		M5M44C258-15		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	25		30		40		ns
t_{RCS}	Read setup time before $\overline{CS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CS}$ high (Note 18)	10		10		10		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 18)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	50		55		70		ns
t_{AH}	Column address hold time after $\overline{RAS}$ high	15		15		15		ns
t_{RPC}	Precharge to $\overline{CS}$ active time	0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CS}$ low	25		30		40		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	20		25		30		ns
$t_{h(OECH)}$	$\overline{CS}$ hold time after $\overline{OE}$ low	25		30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	25		30		40		ns

Note 18: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44C258-10		M5M44C258-12		M5M44C258-15		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	190		220		260		ns
t_{RAS}	$\overline{RAS}$ low pulse width	100	10000	120	10000	150	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	25	10000	30	10000	40	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	100		120		150		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	25		30		40		ns
t_{CWL}	$\overline{CS}$ hold time after write low	25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	25		30		35		ns
t_{WH}	Write command hold time for output disable	0		0		0		ns
t_{WCS}	Write setup time before $\overline{CS}$ low (Note 20)	−5		−5		−5		ns
t_{WCH}	Write hold time after $\overline{CS}$ low	20		25		30		ns
t_{WOR}	Write hold time after $\overline{RAS}$ low	95		115		140		ns
t_{AH}	Column address hold time after $\overline{RAS}$ high	15		15		15		ns
t_{WP}	Write pulse width	20		25		30		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CS}$ low	20		25		30		ns
t_{AWR}	Address hold time after $\overline{RAS}$ low	95		110		135		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	95		115		140		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	20		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low	20		25		30		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44C258-10		M5M44C258-12		M5M44C258-15		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 19)	245		285		335		ns
t_{RAS}	$\overline{RAS}$ low pulse width		155	10000	185	10000	225	10000	ns
t_{CS}	$\overline{CS}$ low pulse width		80	10000	95	10000	115	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low		155		185		225		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low		80		95		115		ns
t_{RCS}	Read setup time before $\overline{CS}$ low		0		0		0		ns
t_{CWD}	Delay time, $\overline{CS}$ low to write low	(Note 20)	50		60		75		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low	(Note 20)	125		150		185		ns
t_{CWL}	$\overline{CS}$ hold time after write low		25		30		35		ns
t_{RWL}	$\overline{RAS}$ hold time after write low		25		30		35		ns
t_{WP}	Write pulse width		20		25		30		ns
t_{DS}	Data setup time		0		0		0		ns
t_{DH}	Data hold time after write low		20		25		30		ns
t_{AWD}	Delay time, address to write low	(Note 20)	75		85		105		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CS}$ low		25		30		40		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		20		25		30		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low		20		25		30		ns

Note 19: t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$.

20: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the DQ (at access time and until $\overline{CS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Static Column Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

Symbol	Parameter		Limits						Unit
			M5M44C258-10		M5M44C258-12		M5M44C258-15		
			Min	Max	Min	Max	Min	Max	
t_{RSC}	SC read cycle time		55		60		75		ns
t_{WSC}	SC write cycle time		55		60		75		ns
t_{RWSC}	SC R/W, R/M/W, cycle time		115		130		155		ns
t_{RAS}	$\overline{RAS}$ low pulse width		155	50000	180	50000	225	50000	ns
t_{CS}	$\overline{CS}$ low pulse width		25	10000	30	10000	40	10000	ns
t_{CP}	$\overline{CS}$ high pulse width		15		15		20		ns
t_{RSW}	Delay time, $\overline{RAS}$ to 2nd Write low		115		135		165		ns
t_{WI}	Write invalid time		15		15		20		ns
t_{WHRW}	Write high pulse width for R/W, R/M/W, cycle		85		95		115		ns
t_{WH}	Write command hold time for output disable		0		0		0		ns
t_{AOH}	Data hold time from address change		10		10		10		ns
t_{WAD}	Delay time write to address change	(Note 21)	−10	10	−10	10	−10	10	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low		25		30		40		ns
$t_{h(WHOE)}$	$\overline{OE}$ hold time after write high		60		65		80		ns

Note 21: $t_{WAD(max)}$ is specified as a reference point only. If $t_{WAD} \geq t_{WAD(max)}$, access time is assumed by t_{CAA}.

$\overline{CS}$ before $\overline{RAS}$ Refresh Cycle

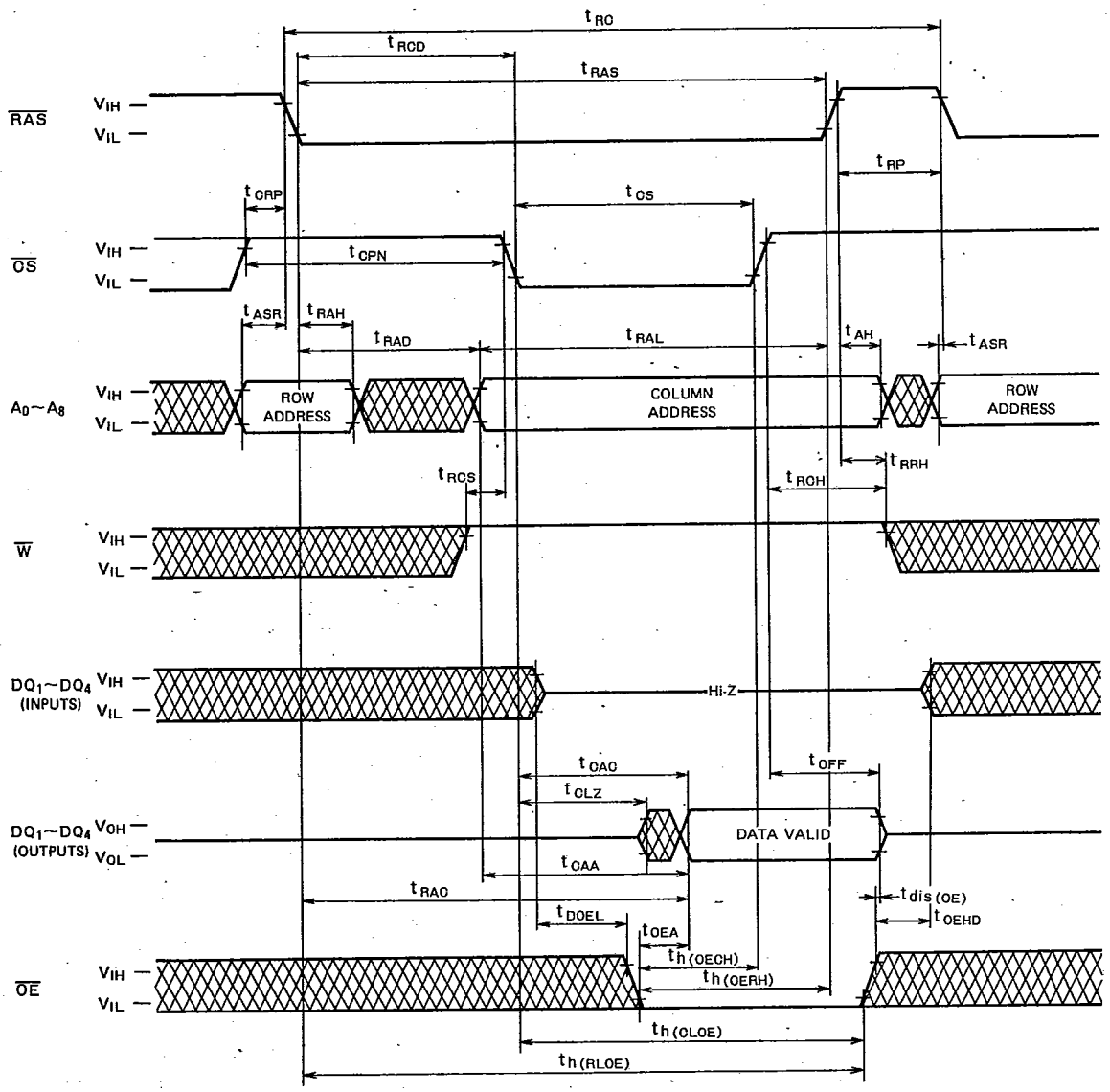
Symbol	Parameter	Limits						Unit
		M5M44C258-10		M5M44C258-12		M5M44C258-15		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh	20		25		30		ns
t_{RPC}	Precharge to $\overline{CS}$ active time	0		0		0		ns

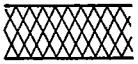
Note 22: Eight or more $\overline{CS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CS}$ before $\overline{RAS}$ refresh mode.

T-46-23-17

Timing Diagrams (Note 23)

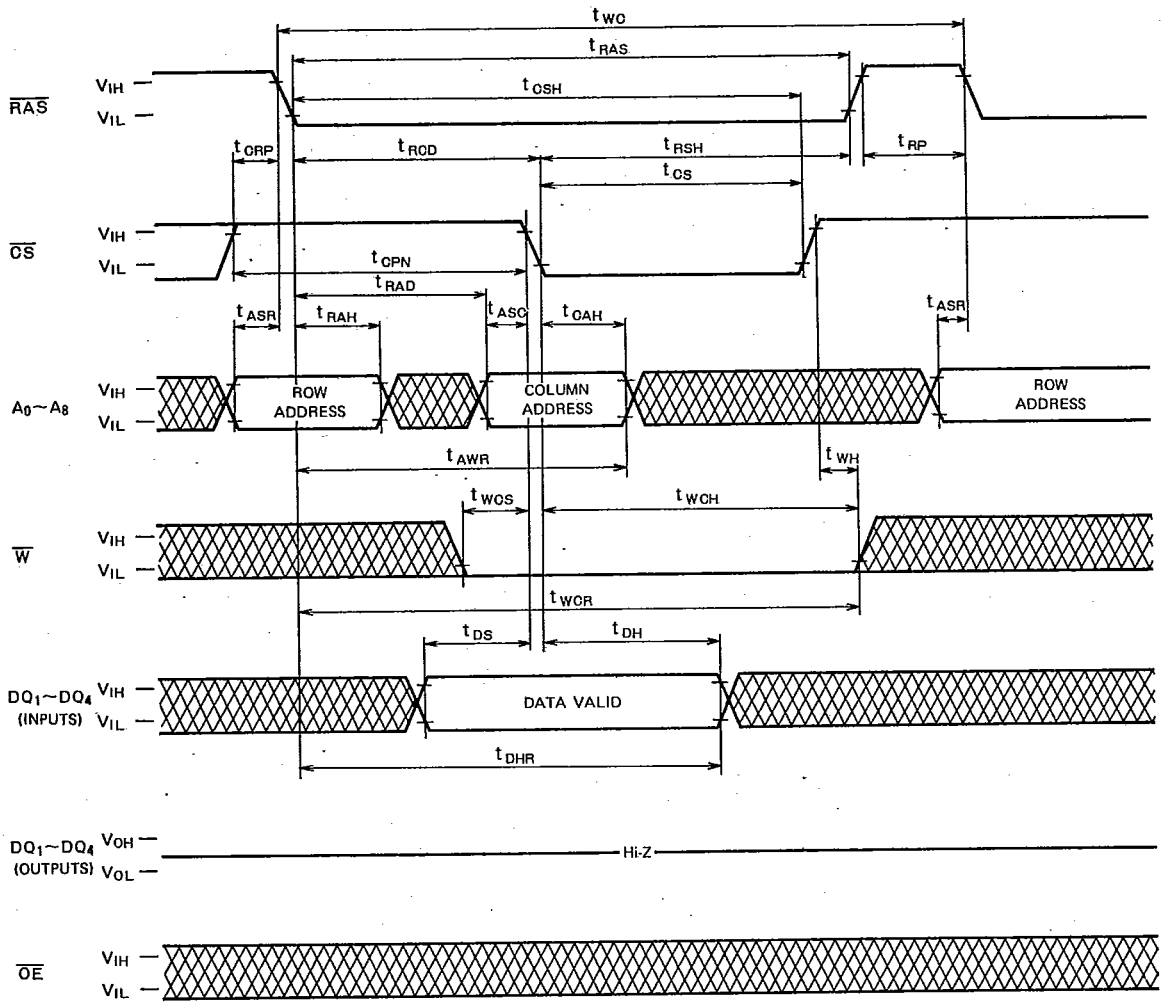
Read Cycle



Note 23  Indicates the don't care input.

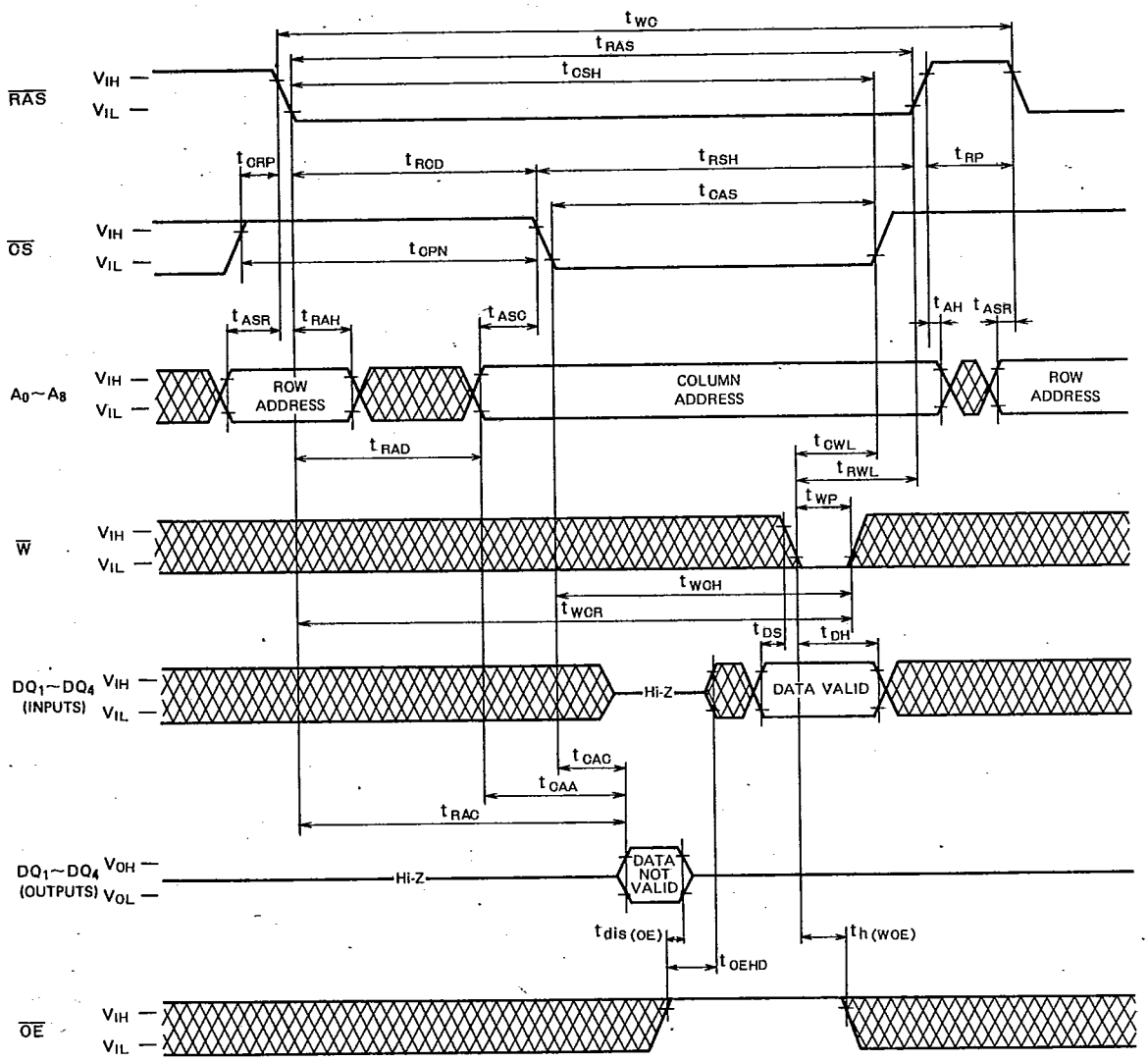
T-46-23-17

Write Cycle (Early write)



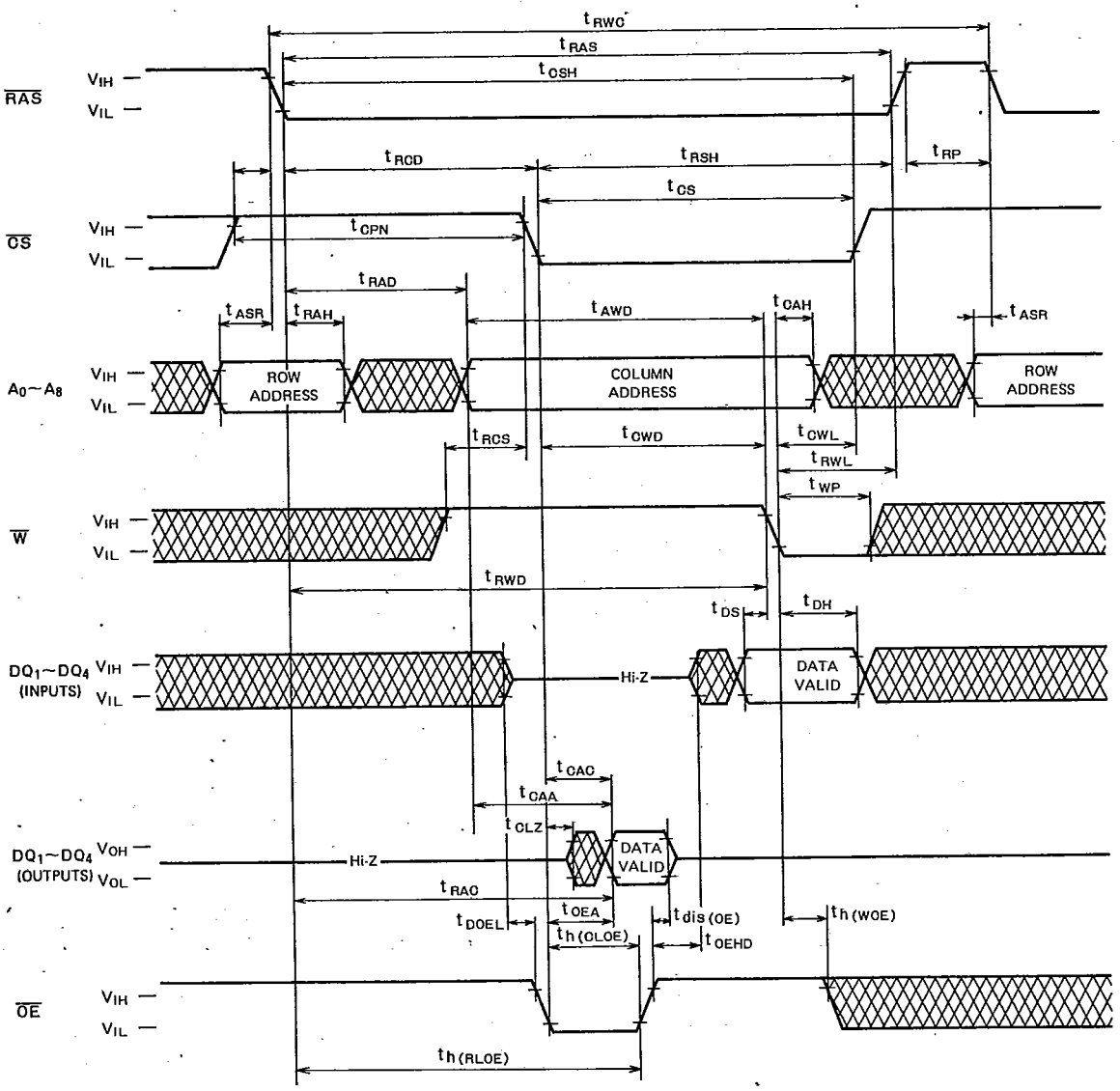
T-46-23-17

Write Cycle (Delayed Write)

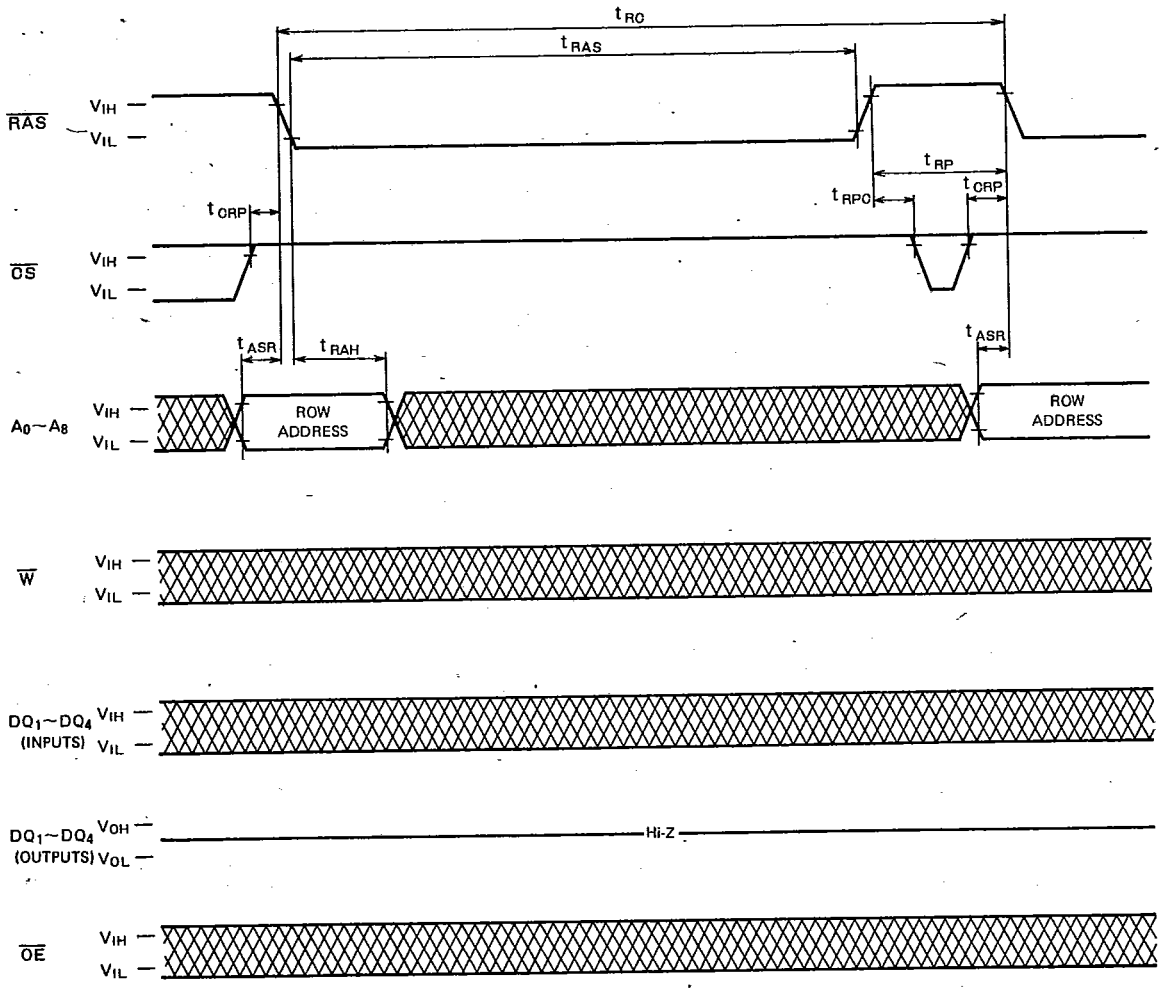


T-46-23-17

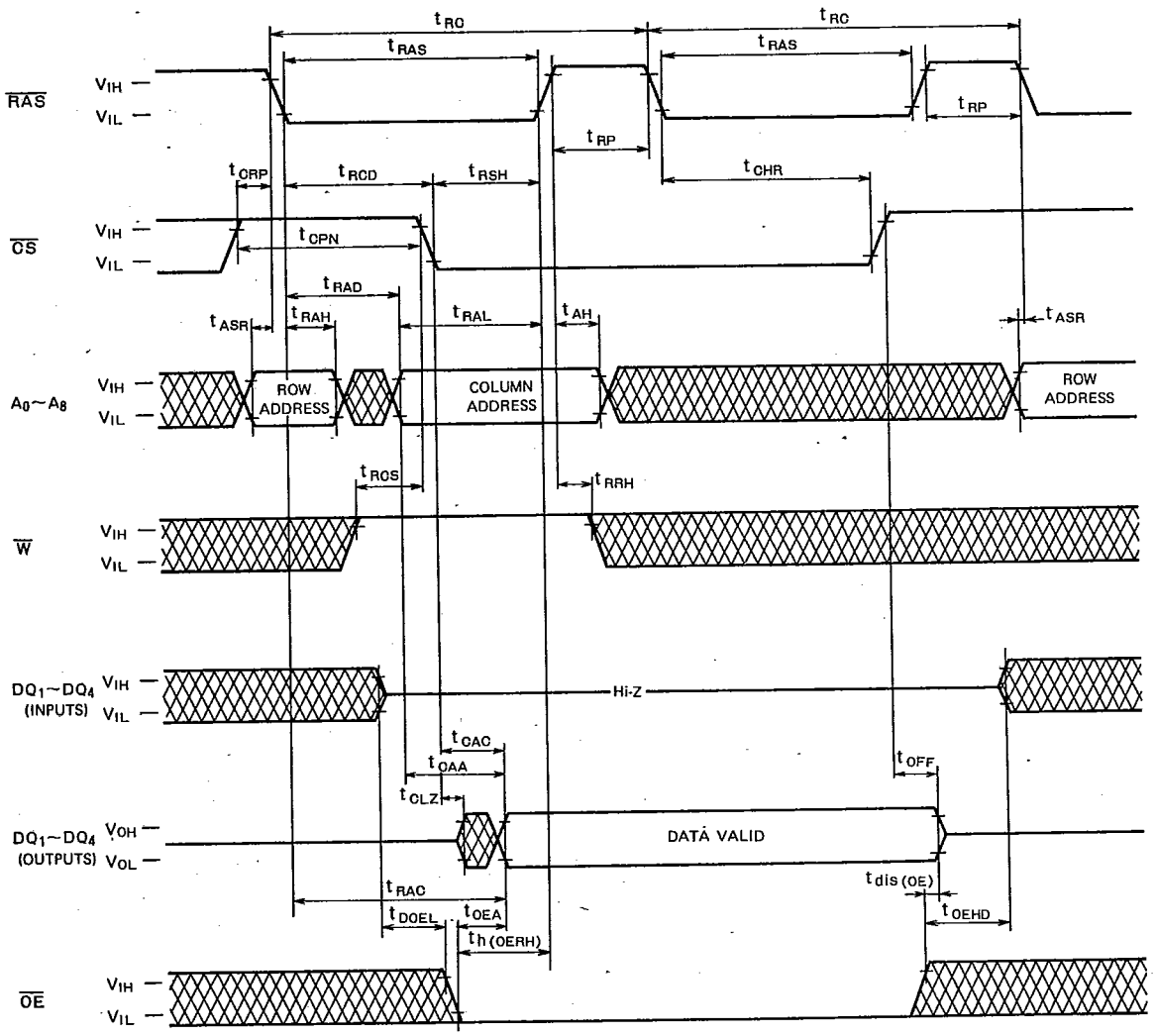
Read-Write, Read-Modify-Write Cycle



RAS-only Refresh Cycle

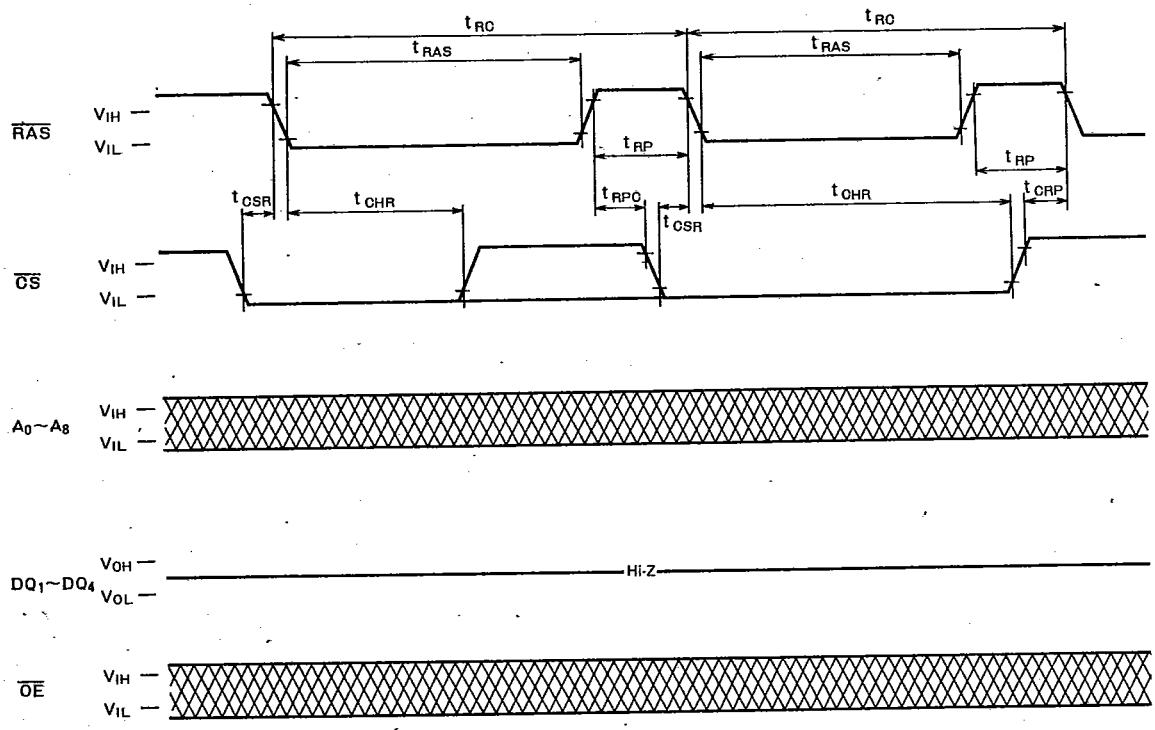


Hidden Refresh Cycle

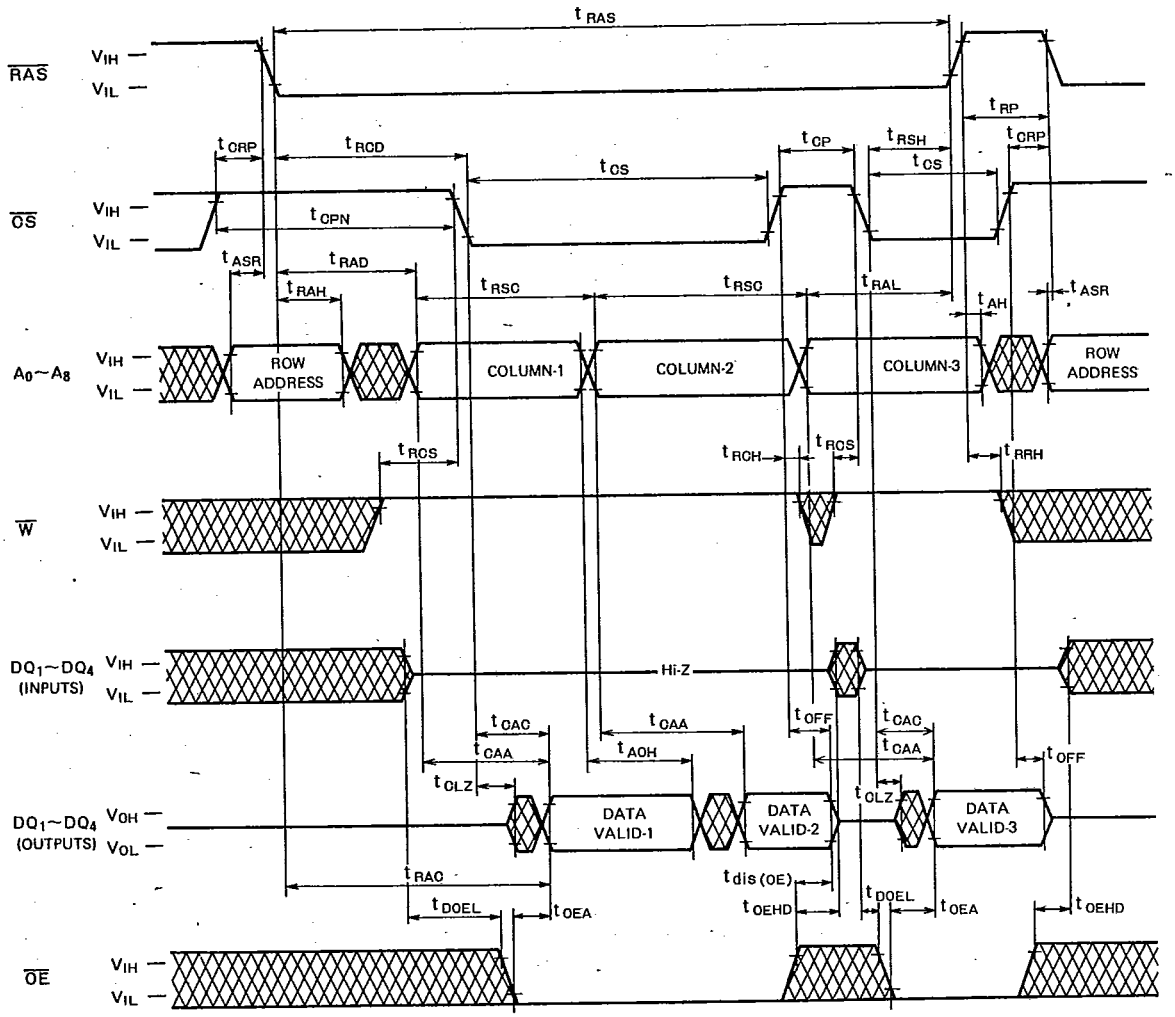


T-46-23-17

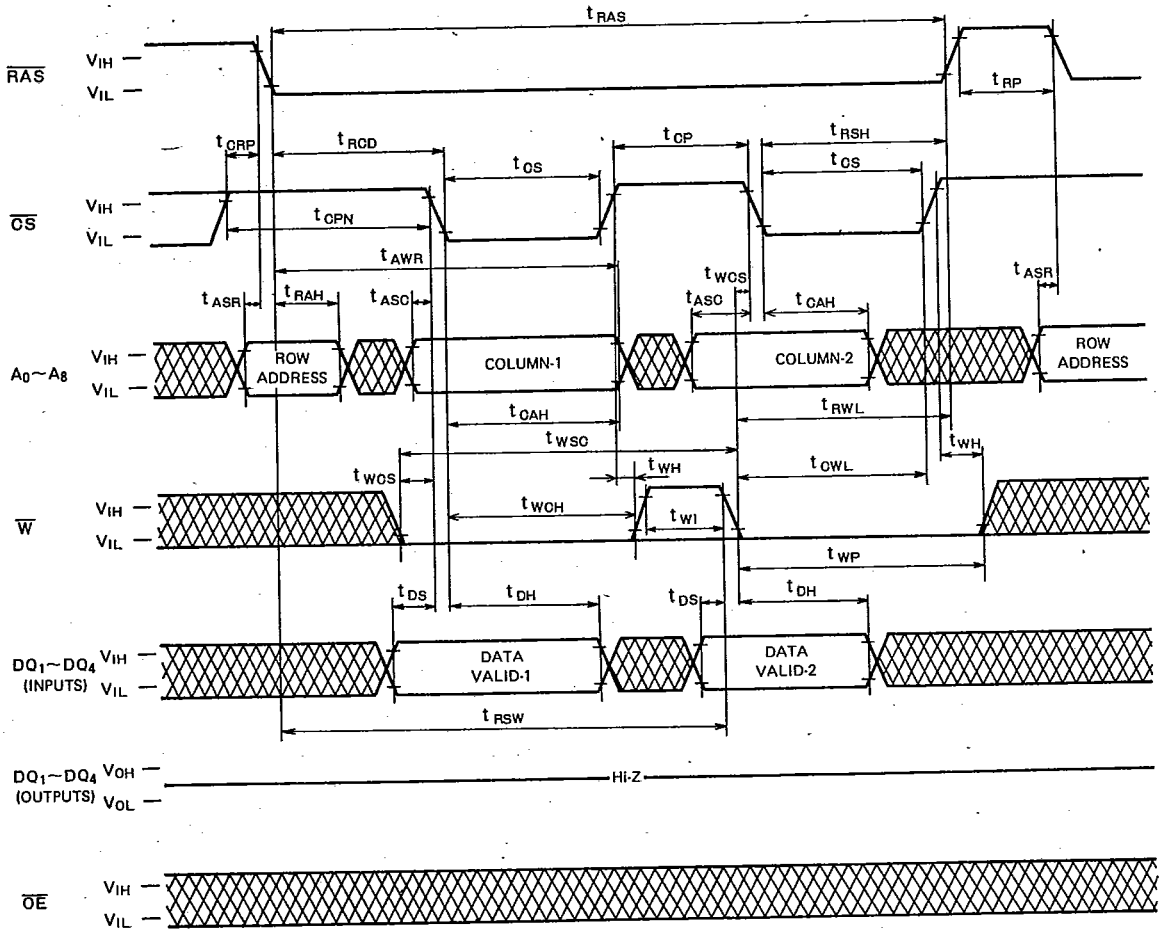
$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



Static Column Mode Read Cycle



Static Column Mode Early Write Cycle



Static Column Mode Read-Write, Read-Modify-Write Cycle