VTC Inc.
Value the Customer™

VM5252015FC

20-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER WITH SERVO WRITE

950801

ADVANCE INFORMATION

August,1995

FEATURES

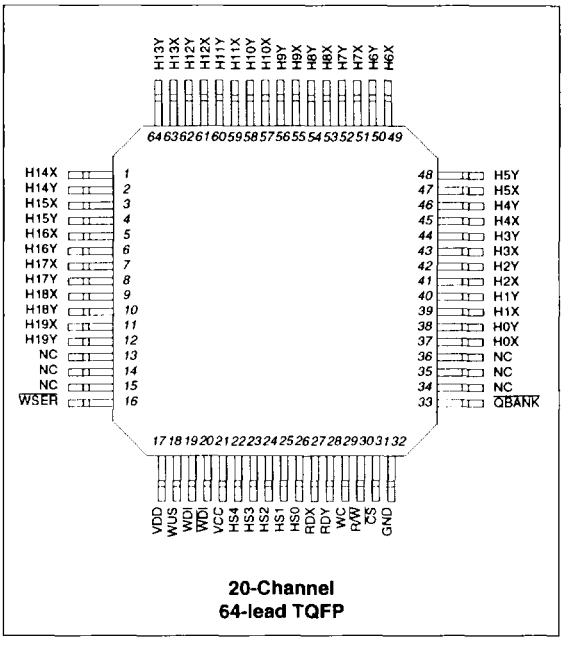
- High Performance
  - Rise/Fall Times = 4.0 ns Typical into 0.5 µH
  - Input Capacitance = 9 pF Typical
  - Input Noise = 0.6 nV/√Hz Typical
  - Head Inductance Range = 0.2 – 1.5 µH Optimized for 0.5µH
  - Voltage Gain = 150 V/V
- PECL Write Data Lines
- Write Current Range 5 – 35 mA
- Operates From +5V/+12V and +5V/+7V in Servo Mode
- Power Supply Fault Protection
- Servo Write Two Banks of Ten Channels or Four Banks of Five Channels
- No Write Data Flip-Flop

DESCRIPTION

The VM5252015FC is a high-performance, integrated read/write preamplifier designed for use with two-terminal, thin-film recording heads. The circuit contains read amplifiers and write drivers to address twenty channels. Internal damping resistors provide different values of damping resistance between the read mode and write modes. When deselected, the circuit enters a low-power sleep mode. Current gain in the write mode is 20 and it is DAC or resistor-controllable. The power supply fault detect circuit shuts off write current in the event the power supply level drops below a unsafe threshold, thus protecting the data on the disk from any potential transients. If a line should open up, the mode select lines ($\overline{CS}$ and $R\overline{W}$) have internal pullup resistors to ensure the select lines will be forced into a high state to prevent the device from affecting data on the disk.

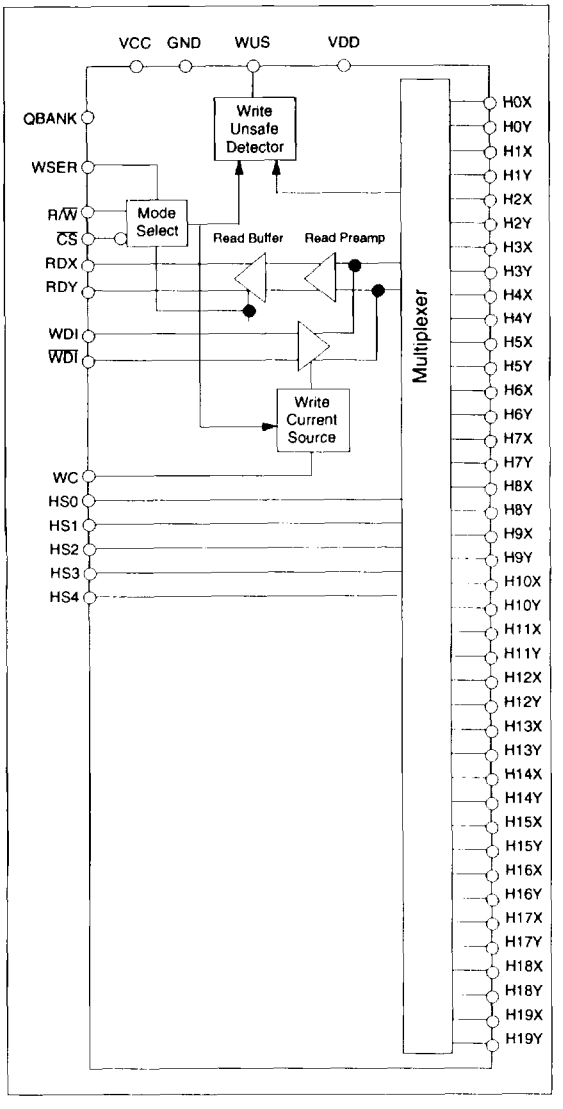
The part has a servo write mode for writing five or ten channels at a time.

CONNECTION DIAGRAM



20-Channel
64-lead TQFP

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD} ..... -0.3V to +13.5V
- V_{CC} ..... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:
- Digital Input Voltage V_{IN} ..... -0.3V to (V_{CC} + 0.3)V
- Head Port Voltage V_H ..... -0.3V to (V_{CC} + 0.3)V
- WUS Pin Voltage Range V_{WUS} .....-0.3V to +13.5V

Output Current:
- RDX, RDY: I_O .....-10mA
- WUS: I_{WUS} ..... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range ..... -65° to 150°C

Thermal Characteristics, Θ_{JA}:
- 64-lead TQFP ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD} ..... 12V ± 10%
- V_{CC} ..... 5V ± 10%

Junction Temperature .....0°C to 125°C

CIRCUIT OPERATION

The VM5252015FC addresses up to ten two-terminal thin-film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM5252015FC as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

The write current direction is controlled by the WDI and $\overline{WDI}$ pins. When WDI > $\overline{WDI}$ current flows into the "X" head port. Current flows in the opposite direction when the write data voltages are reversed.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 2.5V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 50/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM5252015FC because the internal 300Ω damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below with a high level on the open collector output pin, WUS.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device in servo mode (applicable when WUS is not used for servo selection)
- Device not selected

Two negative write data transitions, after the fault is corrected, may be required to clear the WUS flag.

Write Servo Mode

In this mode, the operation is the same as described above except that five or ten channels are written at the same time. Two options are available for servo mode control. The first is to use pin WSER to control when the device is in servo mode (pull WSER low to enable the servo write feature). The second option is to use the WUS external resistor to control servo mode. In either case servo mode must be preceded by lowering VDD to 7V ±10%. To select servo using the WUS resistor the following procedure is used:

1. Lower VDD to 7V ±10%
2. Enter read mode via R/$\overline{W}$ high
3. WUS pull-up resistor should be tied at least 1.3V above VCC through a 1k resistor.

The device is now in servo mode with either five or ten heads writing at the same time. Upon entering write servo mode the VDD fault level will be lowered to a 5.8V threshold. To return to normal operations the following sequence is used:

1. Enter read mode
2. Return WUS resistor to VCC.
3. Raise VDD supply back to 12V ±10%
4. Drop the R/$\overline{W}$ line low

The $\overline{QBANK}$ pin is used to permit servo writing in four banks of five heads each. When $\overline{QBANK}$ is pulled low, the VM5252015FC enters quad bank select mode and HS0 and HS1 are used to select the active banks (heads 0 - 4 for HS0 = low and HS1 = low, heads 5 - 9 for HS0 = high and HS1 = low, heads 10 - 14 for HS0 = low and HS1 = high, and heads 15 - 19 for HS0 and HS1 = high). When $\overline{QBANK}$ is pulled high, the VM5252015FC enters dual bank select mode and HS0 is used to select the active banks (heads 0 - 9 for HS0 = low and heads 10 - 19 for HS0 = high). The bank selection scheme applies to either of the two servo selection methods (using WUS resistor or the WSER pin). The $\overline{QBANK}$ pin is available on all package types.

Read Mode

Read mode configures the VM5252015FC as a low-noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 35mW for a sleep mode. Multiple devices may have their read outputs wire OR'ed together and the write current programming resistor common to all devices

Table 25: Mode Select

R/$\overline{W}$	*$\overline{CS}$*	*MODE*
0	0	Write
1	0	Read
0	1	Idle
1	1	Idle

Table 26: Head Select

HS0	*HS1*	*HS2*	*HS3*	*HS4*	*HEAD*
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15
0	0	0	0	1	16
1	0	0	0	1	17
0	1	0	0	1	18
1	1	0	0	1	19

PIN DESCRIPTIONS

NAME	*I/O*	*DESCRIPTION*
HS0 - HS4	I*	Head Select: selects one of up to 19 heads. HS0 and HS1 also select which bank of heads is written to during servo write when $\overline{\text{QBANK}}$ is pulled low (heads 0 - 4 for HS0 and HS1 = low, heads 5 - 9 for HS0 = high and HS1 = low, heads 10 - 14 for HS0 = low and HS1 = high, and heads 15 - 19 for HS0 and HS1 = high). HS0 also selects which bank of heads is written to during servo write when $\overline{\text{QBANK}}$ is pulled high (heads 0 - 9 for HS0 = low and heads 10 - 19 for HS0 = high)
H0X - H19X H0Y - H19Y	I/O	X,Y Head Terminals
WDI, $\overline{\text{WDI}}$	I*	Write Data Input: Differential PECL input signal, negative transition toggles direction of head current
$\overline{\text{CS}}$	I	Chip Select: high level signal puts chip in sleep mode, low level wakes chip up
R/$\overline{\text{W}}$	I*	Read/Write Select: high level selects read mode, low level selects write mode
WUS	O*	Write Unsafe: open collector output: high level indicates writes unsafe condition
WC		Write Current Adjust: a resistor adjusts level of write current
RDX - RDY	O*	Read Data Output: differential output data
VCC		+5V Supply
GND		Ground
$\overline{\text{QBANK}}$		Quad Bank Select: low level selects four banks of heads for servo write (0 - 4, 5 - 9, 10 - 14 and 15 - 19); high level selects two banks of heads for servo write (0 - 9 and 10 - 19)
WSER		Servo Write: when pulled low, servo write feature is enabled on selected heads

* May be wire-ORed for multi-chip usage.

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCC Supply Current	I_{CC}	Read Mode		TBD	TBD	mA
		Write Mode		TBD	TBD	
		Idle Mode		TBD	TBD	
VDD Supply Current	I_{DD}	Read Mode		TBD	TBD	mA
		Write Mode		TBD	TBD	
		Idle Mode		TBD	TBD	
Power Dissipation (T_J = 125°C)	P_D	Read Mode		250	TBD	mW
		Write Mode: I_W = 20mA		650	TBD	
		Idle Mode		25	TBD	
Input Low Voltage	V_{IL}	TTL	-0.3		0.8	V
Input High Voltage	V_{IH}	TTL	2.0		V_{CC} +0.3	V
Input Low Current	I_{IL}	V_{IL} = 0.8V, TTL	-200			µA
Input High Current	I_{IH}	V_{IH} = 2.0V, TTL			100	µA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	V_{CC} - 1.0		V_{CC} - 0.7	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	V_{CC} - 1.9		V_{CC} - 1.6	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC}$ - 0.7V			100	µA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC}$ - 1.6V			80	µA
WUS Output Low Voltage	V_{OL}	I_{OL} = 4mA		0.35	0.5	V
VDD Fault Voltage	V_{DDF}		9.5	10	10.5	V
VDD Servo Mode Fault	V_{DDFS}		5.5	5.8	6.1	V
VCC Fault Voltage	V_{CCF}		3.8	4	4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, 0 < V_{CC} 3.8V, 0< V_{DD} < 9V	-200		+200	µA
		Write Mode, 0 < V_{CC} 5.5V, 0< V_{DD} < 13.2V	-200		+200	

WRITE SERVO CHARACTERISTICS

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply Current	I_{CC}	Servo Mode		TBD		mA
VDD Supply Current	I_{DD}	Servo Mode, V_{DD} = 7V ±10%		TBD		mA
Power Dissipation	P_D	Servo Mode @ I_W = 15mA		TBD		W
Servo Write Current Tolerance			-10		+10	%
Servo Write Current Range			5		15	mA
Rise/Fall Time		L_H = 0.5µH, I_W = 15mA, @ V_{DD} = 7V		7		ns
Asymmetry		L_H = 0, R_H = 0			0.5	ns
WDI Input			1		15	MHz

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX, RDY) = 1kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	120	150*	180	V/V
Bandwidth	BW	-1dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz		50		MHz
		-3dB, |Zs| < 5Ω, V_{IN} = 1mVp-p @300kHz		75		
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.60	0.75	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		9	14	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	380	750		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2	5		mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	50	60		dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	45	50		dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz, Selected Channels V_{IN} = 0mVp-p	45	50		dB
Output Offset Voltage	$\|V_{OS}\|$	V_{IN} = 0 on selected head, A_V = 150			150	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	V
		Write Mode	V_{CC} - 3.0	V_{CC} - 2.8	V_{CC} - 2.2	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			35	Ω
Output Current	I_O	AC coupled load, RDX to RDY	1.5			mA

* Nominal gain - other options available

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 0.5µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
WC Pin Voltage	V_{WC}			2.5		V
Write Current Voltage	V_{DH}	I_{WC} = 35mA	10	11	12	Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}			18	22	pF
Differential Output Resistance	R_{OUT}	Without damping resistor	3.2			kΩ
		With damping resistor		300		Ω
WDI Transition Frequency	f_{DATA}	WUS = low	1.0			MHz
Write Current Range	I_W	1430Ω, < R_{WC} < 5kΩ	5		35	mA
Write Current Tolerance	ΔI_W	I_W range 5mA to 35mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 0.5µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
R/$\overline{W}$ to Write Mode	t_{RW}	Delay to 90% of write current			0.2	µs
R/$\overline{W}$ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.5	µs
$\overline{CS}$ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, L_H = 0, R_H = 0			30	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, L_H = 0, R_H = 0		0.2	0.5	ns
Rise/Fall Time*	t_r/t_f	L_H = 0.5µH, I_W = 20mA		4		ns
Rise/Fall Time	t_r/t_f	(L_H = 0µH)		TBD		ns

*Rise/Fall time might vary according to customer rise fall/settle time trade off. Rise/Fall time and settle time will be selected for maximum bit cell.

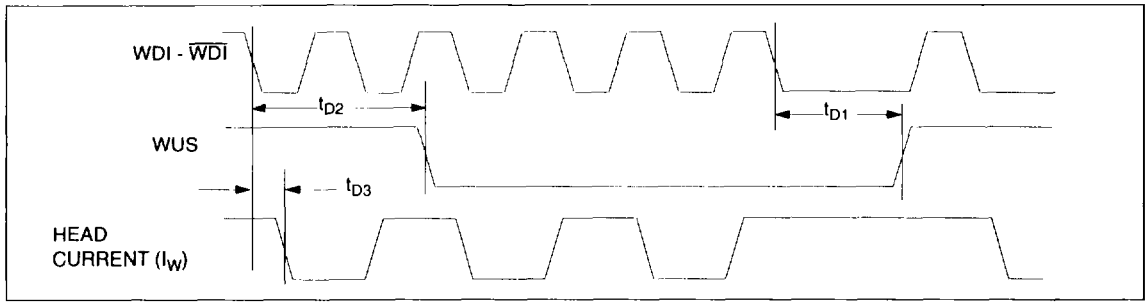


Figure 1: Write Mode Timing Diagram