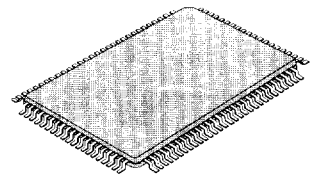
80-CHANNEL SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD

100 QFP



KS0083 is a graphic type LCD driver LSI which is fabricated by CMOS process for high voltage. In case of segment driver, can be selected 4 bit, 1 bit data transfer or chip select mode.

FUNCTION

- **DOT MATRIX LCD DRIVER with 80 channel output.**
- **Input/Output**
  - **— Output: 80 channel waveform for LCD driving**
  - **— Input: • parallel display data and control signal from controller**
    • bias voltage (V_3, V_4, V_{SS})

FEATURES

- **Power supply voltage: −5V ± 10%**
- **LCD driving voltage: −24V (typ).**
- **Interface**

type 1		type 2		type 3	
COM	SEG	COM	SEG	COM	SEG
KS0083	KS0083	KS0103	KS0083	KS0083	KS0104

- **100QFP and bare chip available**

BLOCK DIAGRAM

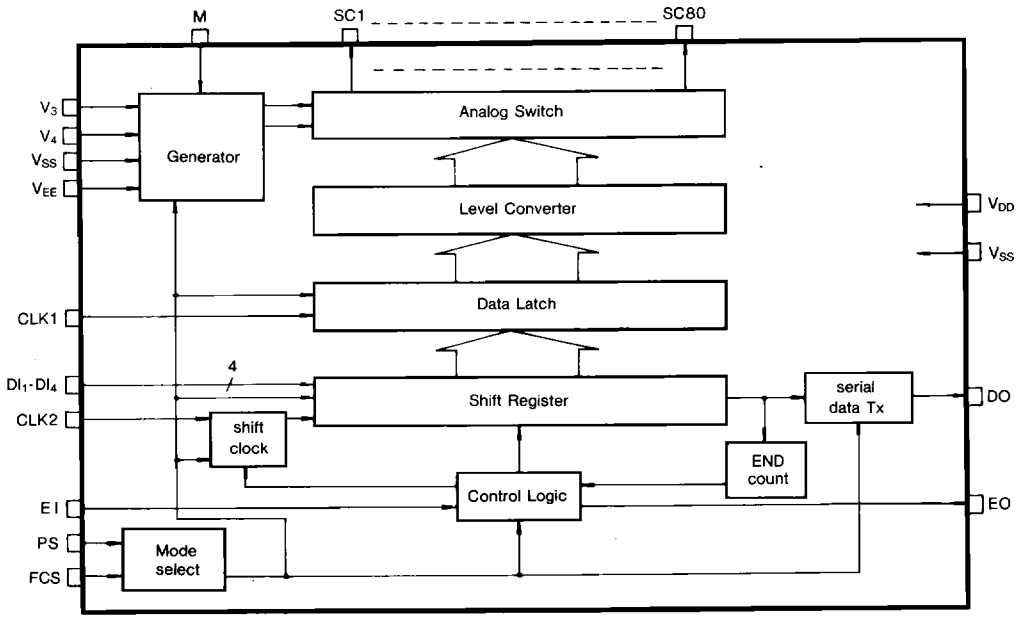


Fig. 1. KS0083 functional block diagram.

PIN CONFIGURATION

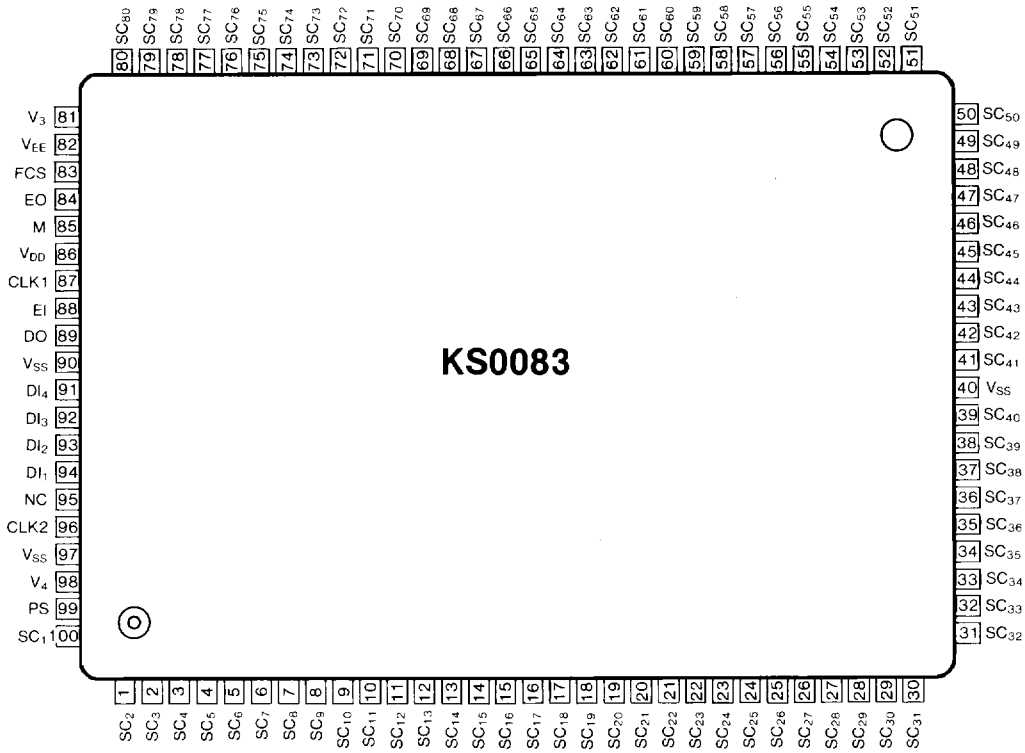


Fig. 2. 100 QFP Top View

PIN FUNCTIONAL DESCRIPTION

<table>
<tr><th>Pin (No.)</th><th>Input Output</th><th>Description</th><th>Interface</th></tr>
<tr><td>$SC_1 \sim SC_{80}$
(100, 1-39, 41-80)</td><td>Output</td><td>LCD driver output terminals (80 Channel)</td><td>LCD</td></tr>
<tr><td>Power supply V_{SS} (40,90,97)</td><td></td><td>GND (0V)</td><td>Power</td></tr>
<tr><td>Power supply V_{EE} (82)</td><td></td><td>LCD driving Voltage (−24V)</td><td>Supply</td></tr>
<tr><td>Power supply V_{DD} (86)</td><td></td><td>Internal Logic driving Voltage</td><td></td></tr>
<tr><td>V_3, V_4 (81, 98)</td><td></td><td>Bias Voltage input for LCD drive; Non-select Level (Must maintain $V_{SS}>V_3>V_4>V_{EE}$.)</td><td>Power</td></tr>
<tr><td>FCS, PS
(83, 99)</td><td>Input</td><td>Mode Select inputs. (refer to application circuit)
<table>
<tr><th>FCS</th><th>PS</th><th>Com/seg driver</th><th>Input mode</th><th>Chip select mode</th><th>Do Output</th></tr>
<tr><td>L</td><td>L</td><td>Segment driver</td><td>1 bit serial input</td><td>X</td><td>O</td></tr>
<tr><td>L</td><td>H</td><td>Segment driver</td><td>4 bit parallel input</td><td>O</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>Segment driver</td><td>1 bit serial input</td><td>O</td><td>H</td></tr>
<tr><td>H</td><td>H</td><td>Common driver</td><td>Serial input</td><td>X</td><td>O</td></tr>
</table>
— In case of serial input mode, DI_1 is data input pin and D_O is data output pin
— In case of 4 bit parallel input mode, Data input and output are;
<table>
<tr><td>DI_1</td><td>SC_1, SC_5, ... SC_{77}</td><td>DI_2</td><td>SC_2, SC_6, ... SC_{78}</td></tr>
<tr><td>DI_3</td><td>SC_3, SC_7, ... SC_{79}</td><td>DI_4</td><td>SC_4, SC_8, ... SC_{80}</td></tr>
</table>
— In case of the common driver, the data transfer clock is CLK_2
— Non-used data input pins are set to V_{SS} or V_{DD} to minimize current consumption</td><td></td></tr>
<tr><td>EO, EI
(84, 88)</td><td>input
output</td><td>Input/Output for Chip Select.
1) EO becomes low by (CLK_1, CLK_2) timing.
2) When "HIGH" data is inputted to EI, the device becomes select mode and reads input data at CLK_2 falling timing. Synchronized at the fall of CLK_2. Input data is shifted.
3) After reading 80 input data (equivalent to 80 CLK_2 clock cycle in the serial mode or 20 CLK_2 clock cycles in the 4 bit parallel mode), EO automatically becomes HIGH level and data reading is complete. EO is reset 1.5 cycles later.
4) When two or more devices are used in the chip select mode, EO of each stage is connected to EI of the next stage.
(1) EO of all device connected is reset and device becomes non-select state and waits for EI input after the previous 1).
(2) When "HIGH" level is input to the first EI in the cascade connection, the first device performs the operations in 2) and 3).
(3) When EI of the second device is connected to EO of the first device, the second device perform the operations 2) and 3) after the first device. This operation is repeated in the same method subsequently.</td><td>controller or KS0083</td></tr>
</table>

PIN FUNCTIONAL DESCRIPTION (continued)

Pin (No.)	Input Output	Description	Interface
M (85)	input	LCD waveform AC conversion signal input (segment signal drive mode): Latch data L (non-select) → M=L, SC=V_3; Latch data H (select) → M=H, SC=GND (common signal drive mode): Latch data L (non-select) → M=L, SC=V_3; Latch data H (select) → M=H, SC=V_{EE}	controller
CLK1 (87)	input	Clock pulse input terminal for data latch	controller
CLK2 (96)	input	Clock pulse input terminal for data shift	controller
DI_1-DI_4 (91-94)	input	Display data input from the LCD controller LSI. In case of the common driver mode or serial input mode, supply the input data to DI_1 and DI_2-DI_4 have to be set to V_{SS} level or V_{DD} level.	controller
DO (89)	output	DO is high level in the chip select made.	KS0083
NC		No Connection	NC

MAXIMUM ABSOLUTE LIMIT (T_a=25°C)

Characteristic		Symbol	Value	Unit
Supply voltage	Logic	V_{DD}	−7 to +0.3	V
	LCD drivers	V_{LCD}	−30 to +0.3	
Input voltage		V_{IN}	V_{DD}−0.3 to +0.3	
Operating temperature		T_{opr}	−20 to +70	°C
Storage temperature		T_{stg}	−55 to +150	

*Voltage greater than above may damage to the circuit.

Maximum absolute limits are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device beyond them is not implied. Long exposure to these conditions may affect device reliability.

DC CHARACTERISTICS (V_{DD} = −5V ± 10%, V_{SS} = 0V, V_{EE} = −24V ± 3V, T_a = 25°C)

Characteristic		Symbol	Test condition	Min	Typ	Max	Unit
Power supply current		I_{DD}	1 bit serial (3.3MHz)			5.0	mA
			4 bit parallel (2.0MHz)			10.0	mA
Input Voltage	High	V_{IH}	—	0.2V_{DD}			V
	Low	V_{IL}	—			0.8V_{DD}	V
Output Voltage	High	V_{OH}	I_{OH}=−0.4mA	−0.4			V
	Low	V_{OL}	I_{OL}=0.4mA			V_{DD}+0.4	V
Voltage descending (Vi-SCi)		V_{D1}	I_{ON}=1mA for one of SCi			1.0	V
		V_{D2}	I_{ON}=0.2mA for each SCi			1.5	V
Leakage Current	Input	I_{LI}	—			1.0	μA
	Output	I_{LO}	—			10.0	μA

AC CHARACTERISTICS

(V_{DD}= 5V±10%, V_{SS}=0V, V_{EE}=−24V±3V; T_a=+25°C)

(1) Segment driver1; 1 bit serial data input (PS=LOW, FCS=LOW) (refer to: fig. 3)

Characteristic		Symbol	Test condition	Min	Max	Unit
Clock cycle time		t_C		300		
Clock pulse width	High level	t_{WH}		130		
	Low level	t_{WL}		130		
Set up time D before CLK2↓		t_{SU}		70		
Hold time D after CLK2↓		t_h		50		
Clock margin time 1 (from CLK1↓ to CLK2↓)		t_{C1}		20		ns
Clock margin time 2 NOTE 1 (from CLK2↓ to CLK1↓)		t_{C2}		200		
Clock margin time 3 (from CLK2↑ to CLK1↑)		t_{C3}		20		
Clock rise/fall time		t_r,t_f			50	
Output Delay		t_D	C_L=15pF		230	
High level latch clock width		t_{CWH}		130	NOTE 2	
Overlap time of CLK2 "L" and CLK1 "H"		t_{OV}		130		

(2) segment driver; 4 bit data input (PS=High, FCS=LOW) (refer to: fig 4.)

Characteristic		Symbol	Test condition	Min	Max	Unit
Clock cycle time		t_C		500		
Clock pulse width	High level	t_{WH}		230		
	Low level	t_{WL}		230		
Set-up time D before CLK2↓		t_{SU}		70		
Hold time D after CLK2↓		t_h		50		
Clock margin time 1 (from CLK1↓ to CLK2↓)		t_{C1}		20		ns
Clock margin time 2 NOTE 1 (from CLK2↓ to CLK1↓)		t_{C2}		200		
Clock margin time 3 (from CLK2↑ to CLK1↑)		t_{C3}		20		
Clock rise/fall time		t_r, t_f			50	
Output Delay		t_D	C_L=15pF		230	
High level latch clock width		t_{LWH}		130	NOTE 2	
Overlap time of CLK2 "L" and CLK1 "H"		t_{OV}		130		

(3) Common Driver (PS=HIGH, FCS=HIGH) (refer to: fig 5)

Characteristic		Symbol	Test condition	Min	Max	Unit
Clock cycle time		t_C		1000		
Clock pulse width	High level	t_{WH}		130		
	Low level	t_{WL}		830		
Set-up time D before CLK↓		t_{SU}		70		ns
Hold time D after CLK↓		t_h		50		
Output Delay		t_D	CL=15pF		500	
Clock rise/fall time		t_r,t_f			50	

(4) segment driver 2; 1 bit serial data input (PS=LOW, FCS=HIGH) (refer to: fig 6)

Characteristic		Symbol	Test condition	Min	Max	Unit
Clock cycle time		t_C		380		
Clock pulse width	High level	t_{WH}		170		
	Low level	t_{WL}				
Set-up time D before CLK↑		t_{SU}		70		
Hold time D after CLK↑		t_h		50		
Clock margin time 1 (from CLK1↓ to CLK2↓)		t_{C1}		20		ns
Clock margin time 2 NOTE 1 (from CLK2↓ to CLK1↓)		t_{C2}		200		
Clock margin time 3 (from CLK2↑ to CLK1↑)		t_{C3}		20		
Clock rise/fall time		t_r,t_f			50	
Output delay		t_D	CL=15pF		230	
High level latch clock with		t_{LWH}		130	NOTE 2	
Overlap time of CLK2 "L" and CLK1 "H"		t_{OV}		130		

note (Input frequency, I/O reference level: 0.8 V_{DD}, 0.2 V_{DD})
1: Valid time (internal shift register)
2: $(t_C \times 1.5)-(t_{C1})-(t_{C3})-(t_r \times 3)$

TIMING DIAGRAM

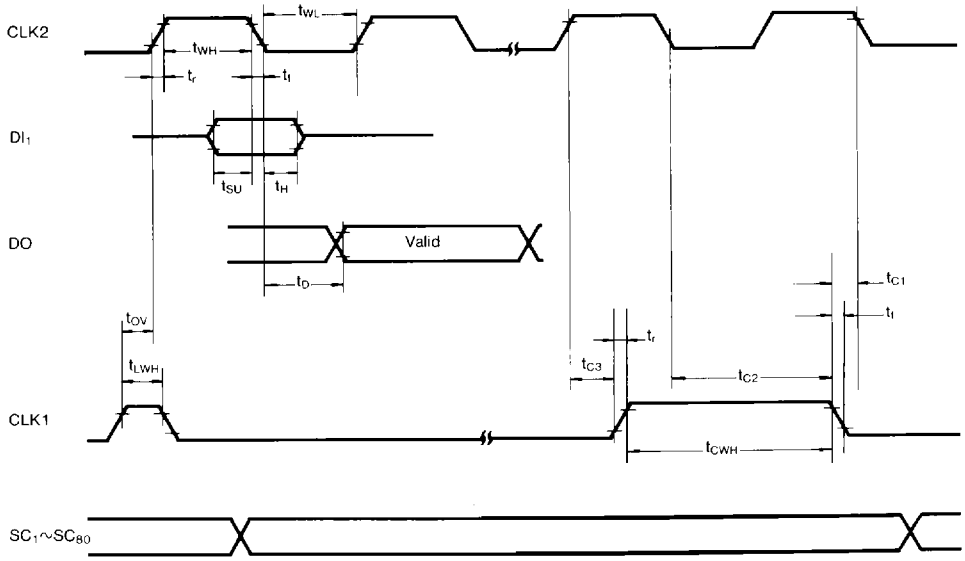


Fig. 3 Segment driver (1 bit serial input)

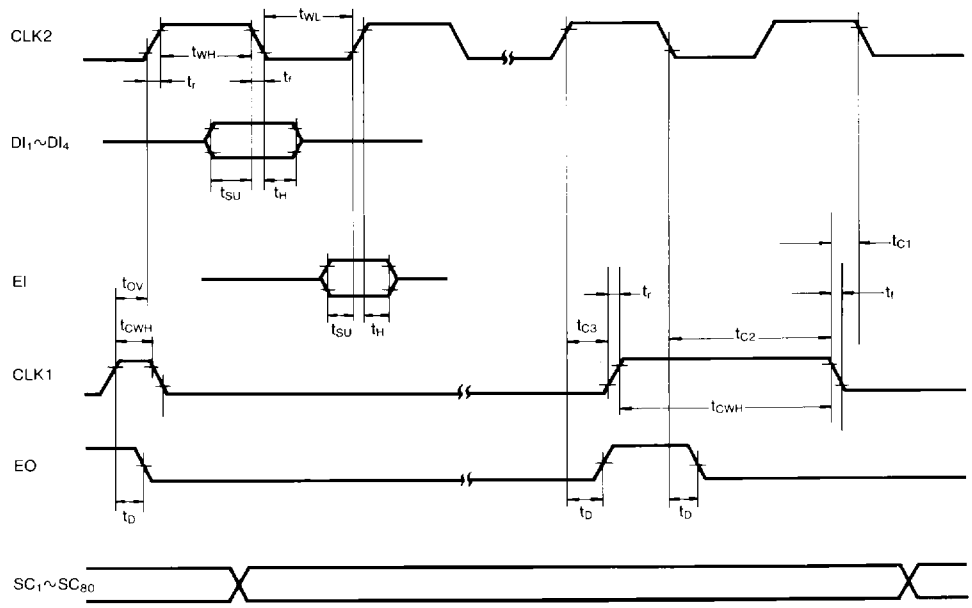


Fig. 4. 4-bit input segment driver

TIMING DIAGRAMS (Continued)

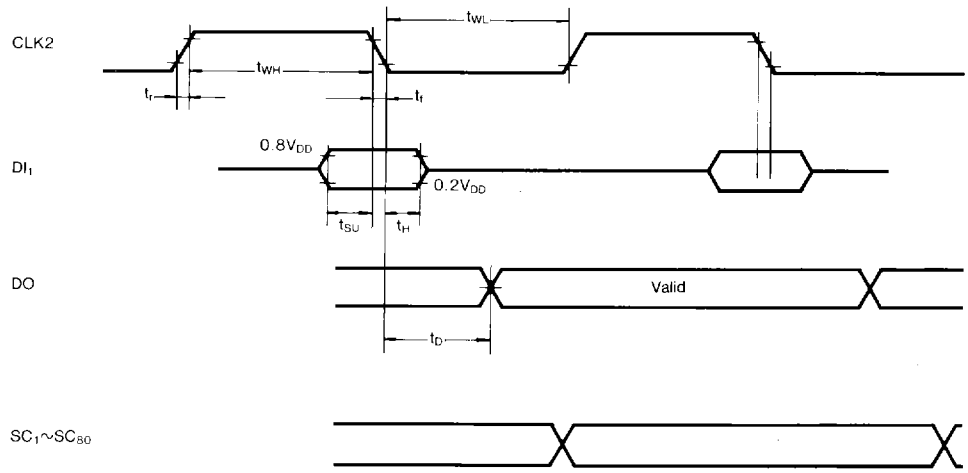


Fig. 5. Common driver

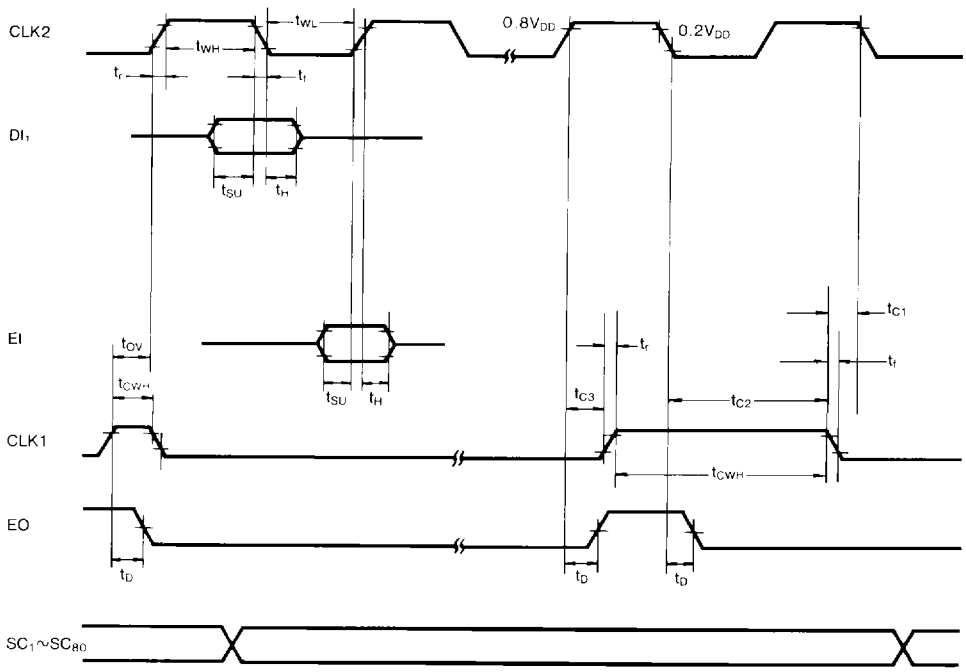
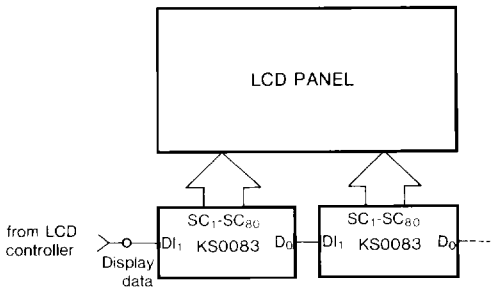


Fig. 6. Segment driver (1 bit serial data input)

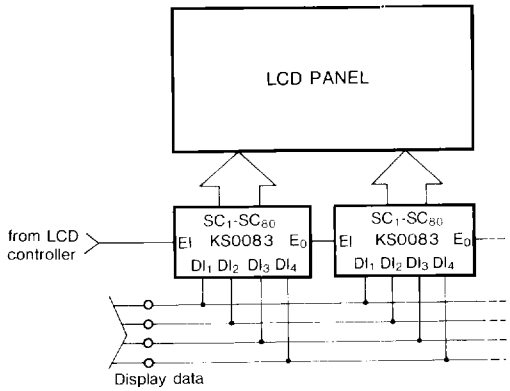
APPLICATION CIRCUIT

Mode Select

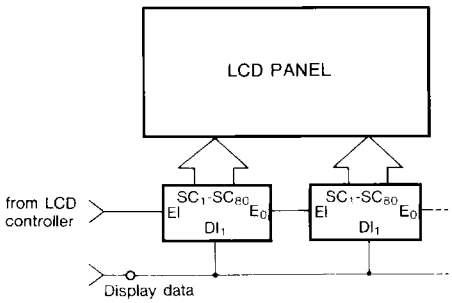
1. segment driver 1; 1 bit serial data input (FCS=L, PS=L)



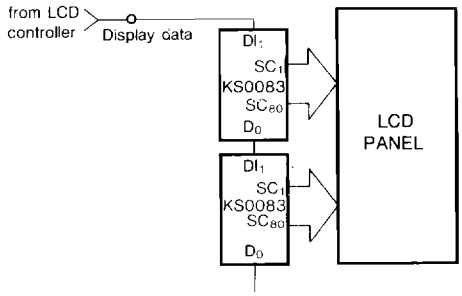
2. segment driver; 4 bit data input (FCS=L, PS=H)



3. segment driver 2; 1 bit serial data input (FCS=H, PS=L)



4. common driver (FCS=H, PS=H)



APPLICATION CIRCUIT