HARRIS SEMICONDUCTOR

HSP50215

August 1997

Digital UpConverter

Features

- Output Sample Rates Up to 52 MSPS; Input Data Rates Up to 13 MSPS
- I/Q Vector, FM, and Shaped FM Modulation Formats
- 32-Bit Programmable Carrier NCO; 30-Bit Programmable Symbol Timing NCO
- Programmable I and Q, 256 Tap, Shaping FIR Filters with Interpolation by 4, 8 or 16
- Interpolation Filter Up Samples Shaping Filter Output to Output Sample Rate Under NCO Control
- Processing Capable of >90dB SFDR
- Cascade Input for Multiple Channel Transmissions
- 16-Bit µProcessor Interface for Configuration and User Data Input

Applications

- Single or Multiple Channel Digital Software Radio Transmitters (Wide-Band or Narrow-Band)
- Base Station Transceivers
- Operates with HSP50214 in Software Radio Solutions
- Compatible with the HI5741 D/A Converter
- HSP50215EVAL Evaluation Board Available

Ordering Information

PART NUMBER	TEMP RANGE (^{o}C)	PACKAGE	PKG. NO
HSP50215VC	0 to 70	100 Ld MQFP	Q100.14x20

Description

The HSP50215 Digital UpConverter (DUC) is a QASK/FM modulator/FDM upconverter designed for high dynamic range applications such as cellular basestations. The DUC combines shaping and interpolation filters, a complex modulator, and Timing and Carrier NCO's into a single package. Each DUC can create a single FDM channel. Multiple DUC's can be cascaded digitally for multi-channel applications.

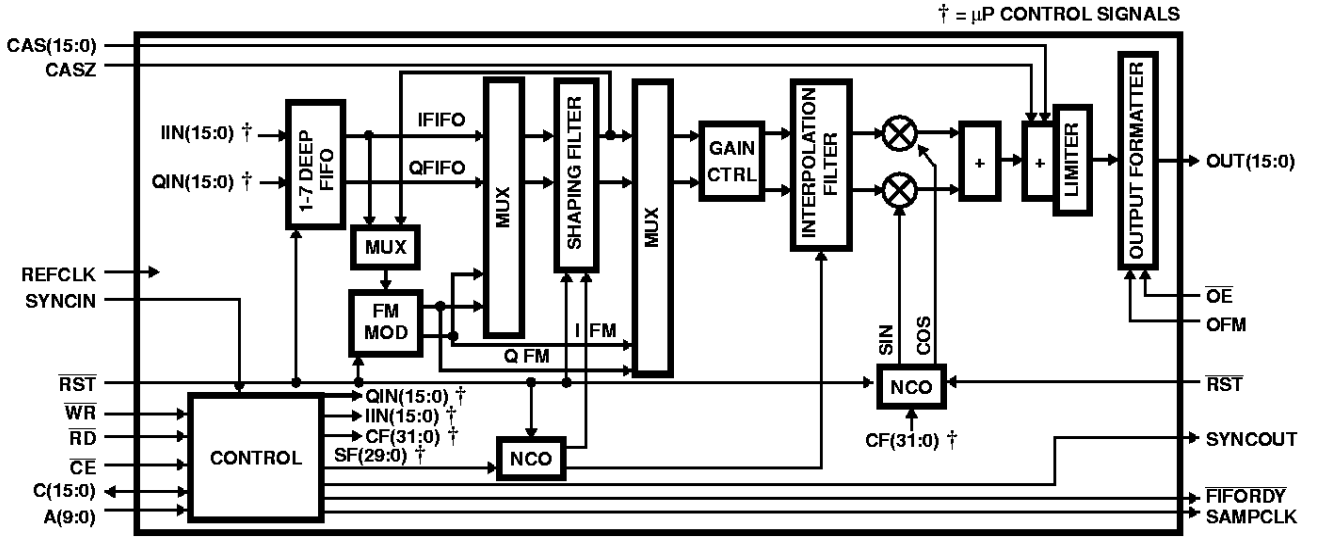
The HSP50215 supports both vector and FM modulation. In vector modulation mode, the DUC accepts 16-bit I and Q samples to generate virtually any quadrature AM or PM modulation format. The DUC also has two FM modulation modes. In the pre-filtered FM mode, the 16-bit frequency samples are pulse shaped/bandlimited prior to FM modulation. No bandlimiting filter follows the FM modulator. This FM mode is useful for GMSK type modulation formats. In the direct FM mode, the 16-bit frequency samples directly drive the FM modulator. The FM modulator output is filtered to limit the spectral occupancy. This FM mode is useful for analog FM or FSK modulation formats.

The DUC includes an NCO driven interpolation filter, which allows the input and output sample rate to have a non-integer or variable relationship. This re-sampling feature simplifies cascading modulators with sample rates that do not have harmonic or integer frequency relationships.

The DUC offers digital output spectral purity that exceeds 85dB at the maximum output sample rate of 52 MSPS, for input sample rates as high as 300 KSPS and can support input sample rates >1 MSPS with reduced purity.

A 16-bit microprocessor compatible interface is used to load configuration and baseband data. A programmable FIFO depth interrupt simplifies the interface to the I and Q input FIFOs.

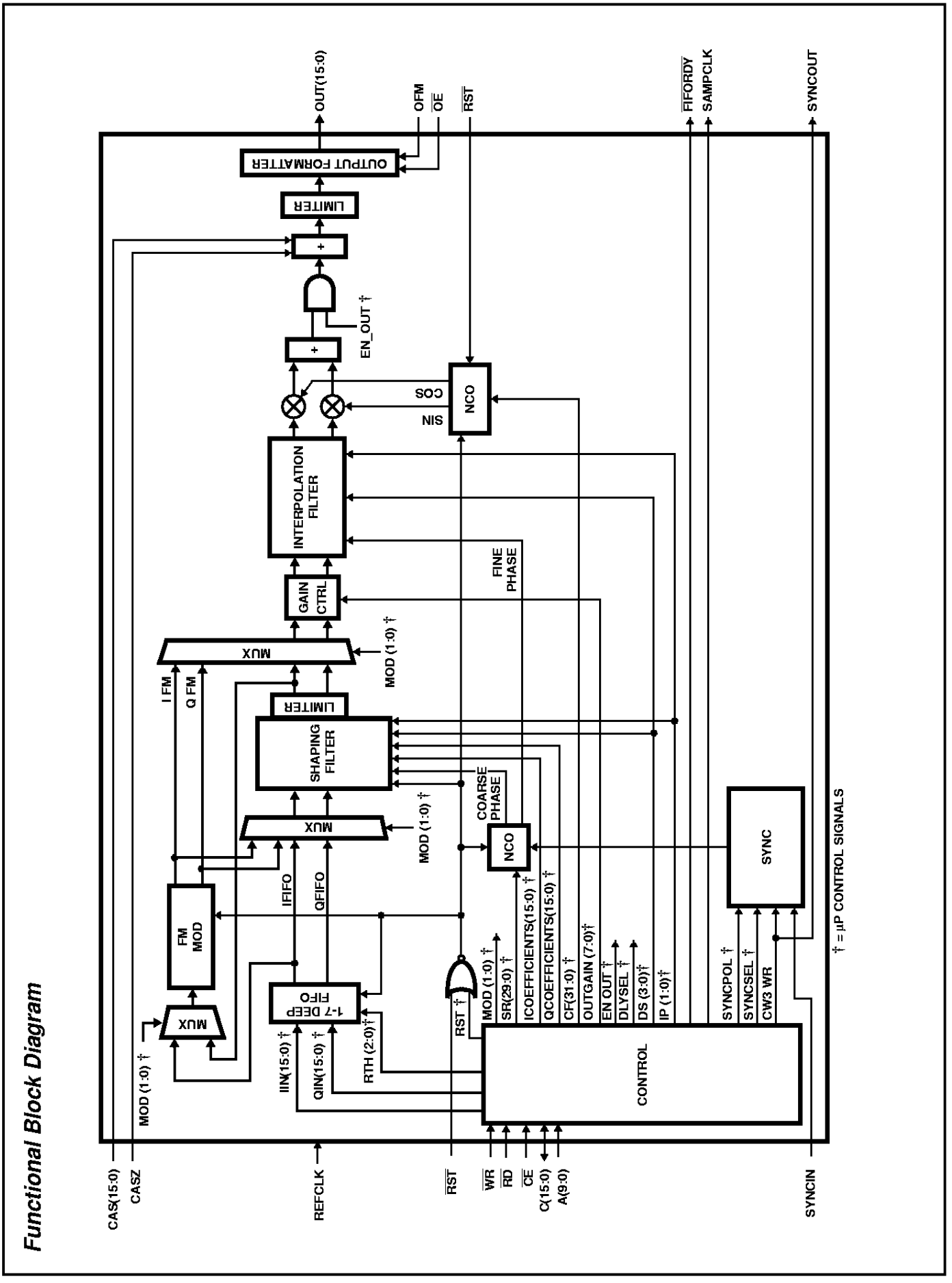
Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

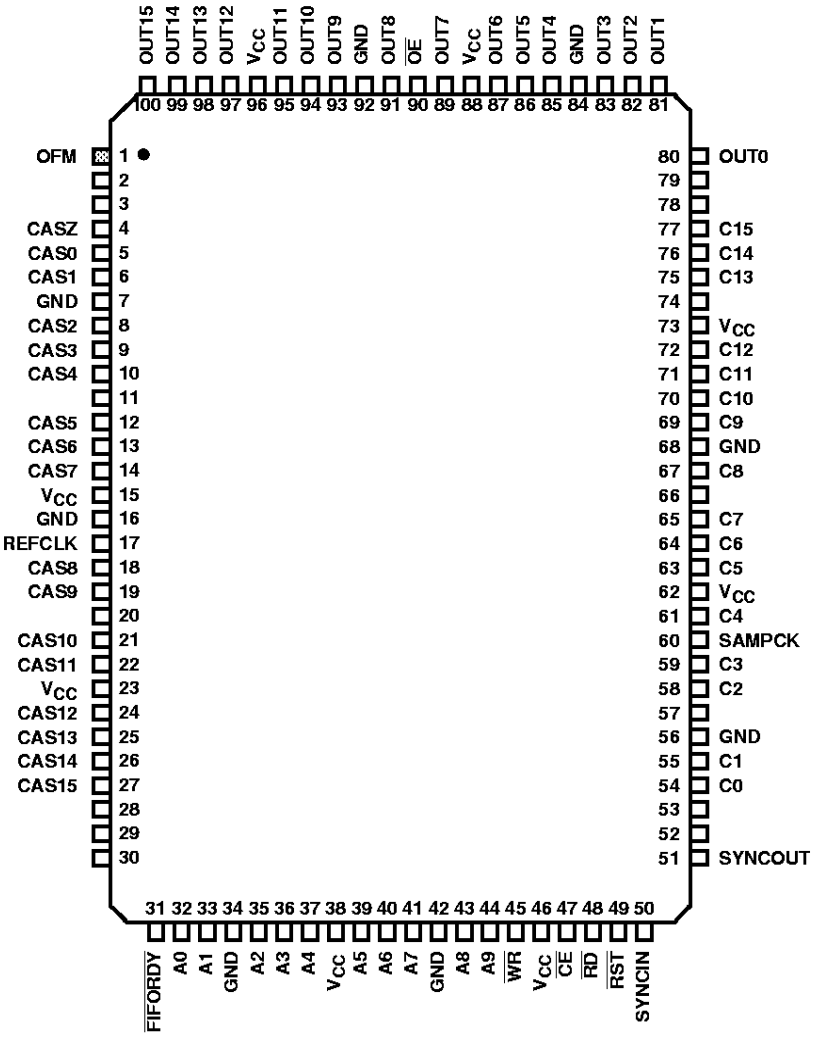
File Number **4346.1**

Functional Block Diagram



Pinout

100 LEAD MQFP
TOP VIEW



Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}	-	+5V Power supply input
GND	-	Power supply ground input
C(15:0)	I/O	µP bidirectional Data bus. The C(15:0) bus is used for loading the configuration data and sample vectors for modulation. C15 is the MSB.
A(9:0)	I	µP Address bus. The A(9:0) bus is used for addressing the proper registers for loading the configuration data and sample vectors for modulation. A9 is the MSB.
$\overline{WR}$	I	µP Write strobe. When $\overline{CE}$ is asserted, data on the C(15:0) data bus is loaded into the address location found on the A(9:0) bus on the rising edge of the $\overline{WR}$ signal. In some cases, there is an internal synchronization to the master clock that must be completed before the next data is written. See the µP interface section for more information.
$\overline{RD}$	I	µP Read control. When $\overline{RD}$ and $\overline{CE}$ are low, the data found in the address location defined by A(9:0) is routed to the C(15:0) µP data bus on the next rising edge of REFCLK.
$\overline{CE}$	I	µP Chip Enable. Used to gate the $\overline{WR}$ and $\overline{RD}$ µP interface control signals.
$\overline{FIFORDY}$	O	FIFO Ready. A $\overline{FIFORDY}$ assertion indicates that the I and Q FIFOs have reached the programmed FIFO depth and more samples are required to maintain that FIFO depth.
REFCLK	I	Reference clock. REFCLK is the master clock for the DUC. All timing is relative to the REFCLK rising edge. The frequency of the reference clock is denoted F_{CLK}.
CAS(15:0)	I	Cascade input bus. This input bus is used to cascade multiple parts by routing the digital modulated signal from one DUC into the output summer of a second DUC. CAS(15:0) is sampled on the rising edge of REFCLK. CAS15 is the MSB.
CASZ	I	Cascade input bus zero. When CASZ is asserted (pulled high), the part places zeroes on the CAS(15:0) data path. CASZ is asynchronous (not registered) to REFCLK and should not be changed on the fly.
OUT(15:0)	O	Output data bus. OUT(15:0) contains the digital modulated DUC output samples and is updated on the rising edge of the REFCLK. OUT15 is the MSB.
OFM	I	Output data bus format. When OFM is asserted (pulled high), the output bus format is 2's complement. When not asserted, the output format is offset binary. The OFM input is asynchronous (not registered) to REFCLK and should not be changed on the fly.
$\overline{OE}$	I	Output data bus enable. When $\overline{OE}$ is asserted (dropped low), the output data bus OUT(15:0) is enabled. When $\overline{OE}$ is not asserted (pulled high), the output data bus OUT(15:0) is placed in the high impedance state.
SYNCIN	I	Sync Input. The SYNCIN input is used to synchronize the processing of multiple parts. The SYNCOUT of one part acts as a master and is connected to the SYNCIN of all of the DUC's that are to by synchronized. The DUC can be programmed so that either rising or falling edge of this signal initiates the processing.
SYNCOUT	O	Sync Output. The SYNCOUT output is used to synchronize the processing of multiple parts. The SYNCOUT of one part acts as a master, and is connected to the SYNCIN of all of the DUC's that are to be synchronized.
SAMPCLK	O	Sample clock. This clock is provided to the data source to indicate when data is being transferred from the FIFO to the shaping filter. The SAMPCLK output is generated by the sample rate NCO when the digital filter takes a new sample. It has approximately 50% duty cycle. The sample is taken on the high-to-low transition. SAMPCLK may be used instead of $\overline{FIFORDY}$.
$\overline{RST}$	I	Reset. When the $\overline{RST}$ input is asserted (dropped low), the DUC is reset and all processing halts. The DUC may also be reset on µP command. Processing remains halted until a sync is generated either by µP command or assertion of SYNCIN. See the Reset section details of the specific functions halted by this control signal.

Functional Description

The HSP50215 Digital UpConverter (DUC) converts digital baseband data into modulated or frequency translated digital samples. The DUC can be configured to create any quadrature amplitude shift-keyed (QASK) data modulated signal, including QPSK, BPSK, and m-ary QAM. The DUC can also be configured to create both shaped and unfiltered FM signals. A minimum of 16 bits of resolution is maintained throughout the internal processing.

The DUC is configured via the 16-bit microprocessor data bus, using the address bus and $\overline{RD}$, $\overline{WR}$ and $\overline{CE}$ control signals. Configuration data that is loaded via this bus includes the 32-bit Sample Rate NCO center frequency, the 32-bit Carrier NCO center frequency, the modulation format, gain control, FIFO control, reset control and sync control. The I and Q baseband channels each have a 256 tap FIR filter whose coefficients and configuration are also programmed via the µP interface. Similarly, the control signals for the I and Q channel interpolation filters are programmed via the µP interface. Once the operational configuration for the device has been set, the 16-bit µP interface is used to input the I and Q data into the associated FIFOs.

The FIFOs provide the data interface between the µP and either the FM modulator or the shaping filters. Multiplexers route the I data to the FM modulator in the unfiltered FM mode and both I and Q to the 256 tap FIR shaping filters in the QASK mode. The shaping filter serves to both shape and interpolate the sample rate to 4, 8, or 16 times the input sample rate. The I shaping filter output can also be routed to the FM modulator for the pre-filtered FM mode. Multiplexers select either the FM modulator output or the shaping filter output to be scaled and routed to the interpolation filters.

The I and Q interpolation filters allow a non-integer increase in sample rate, up to the reference clock rate. The interpolation filter output data is upconverted or modulated by the Carrier NCO and multipliers. The modulated signal is added to modulated inputs from other cascaded DUC's. The output formatter sets the output buffer state and the output data format.

Programmable FIFO

The Programmable FIFOs provide a data storage and interface between the microprocessor data write holding register and the shaping filter or the FM modulator. Signal routing out of the FIFO is set by the modulation format. Each FIFO has seven 16-bit registers. Figure 1 shows the conceptual details of the I and Q FIFOs.

Data enters the FIFO with a write command to either Control Word 0 (for I data), or Control Word 1 (for Q data). This transfers data from the microprocessor holding register into the first 16-bit register of the FIFO. The FIFO counter is incremented every time data is written into the FIFO. Four REFCLK periods are required from the rising edge of a $\overline{WR}$ signal before another $\overline{WR}$ rising edge can occur, (i.e., before data can once again be written into either the I or Q FIFO). This limits the maximum data input (write) rate to 52MHz/4 = 13MHz. ***NOTE: This becomes 6.5 MSPS for quadrature modulations that must write an I and Q to input a symbol.*** The timing details of these FIFO registers are shown in Figure 2. While the data for the I and Q inputs are independent, the Write cycle limitations of the FIFO constrains the maximum input symbol rate of quadrature symbols (both I and Q data) as noted.

When the Shaping Filter requires another sample of data, a request is made to the FIFO for data and the FIFO counter is decremented. Figure 3 indicates the timing of a request for data from the Shaping filter to the actual appearance of data at the FIFO output. The FIFO has circuitry for detecting an empty FIFO as well as a full FIFO. An "empty" FIFO detection causes "zero" data to be entered into the shaping filter. A "full" FIFO detection prevents data from being pushed out of the FIFO before the filter requests it. Do not write to a full FIFO.

A programmable FIFO depth threshold sets when the $\overline{FIFORDY}$ signal is asserted, alerting the data source that more data is required. The $\overline{FIFORDY}$ signal assists a data source in maintaining the desired FIFO data depth. Control Word 18, bits 0-2 are used to set the data FIFO depth threshold for both I and Q inputs. ***NOTE: SAMPCLK may be used instead of $\overline{FIFORDY}$ to indicate that data is transferred from the FIFO to the shaping filter. See the Pin Description table.***

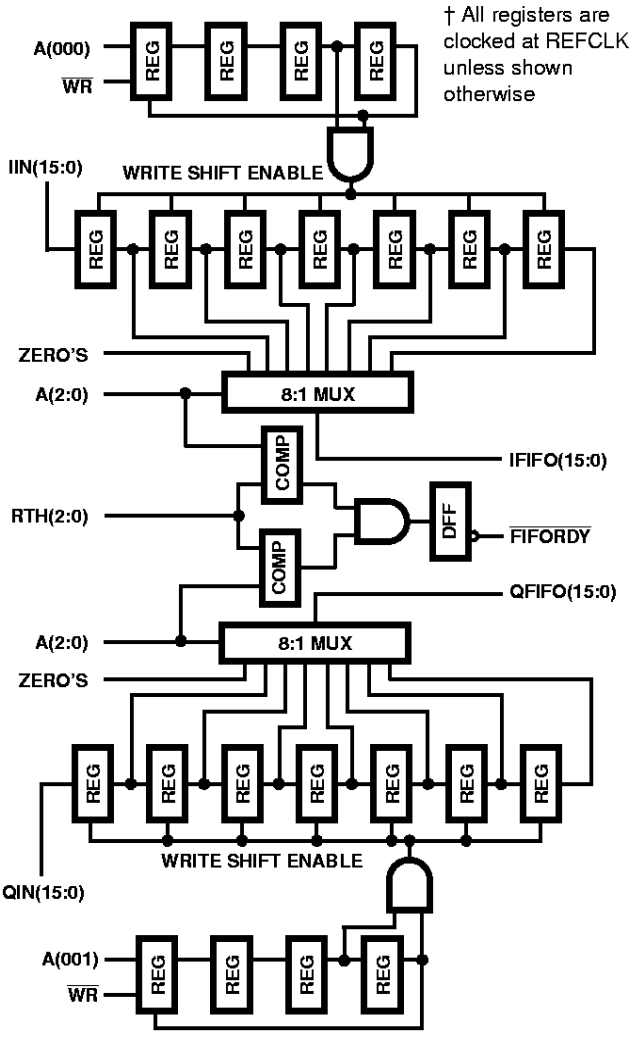


FIGURE 1. I AND Q FIFO BLOCK DIAGRAM

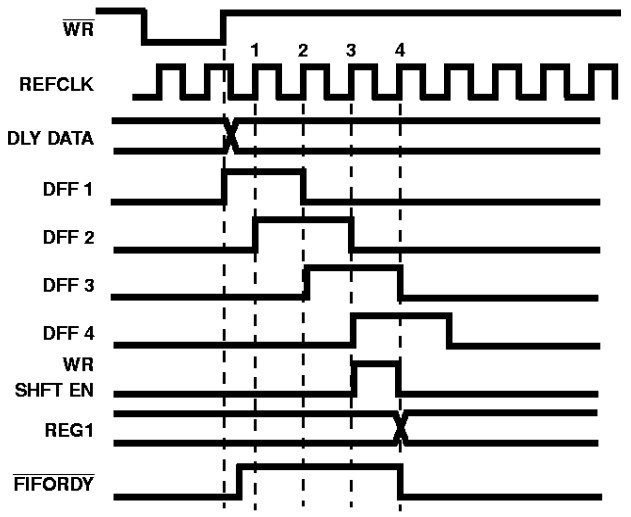


FIGURE 2. FIFORDY AND DATA DELAY TIMING

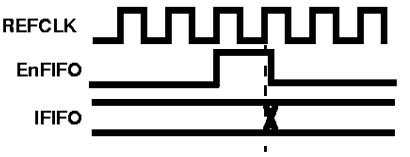


FIGURE 3. FIFO DATA AND ENABLE TIMING

Data Modulation Path

Three data path options are provided, one for each modulation format. The modulation format is selected using Control Word 16 (See the Microprocessor Write section). Control Word 16 bits (1:0) are defined as: 00:QASK, 01:FM with post-modulation filtering, and 10:FM with pre-modulation pulse shaping. These modulation paths are defined in the following subsections.

Modulation Mode 00 - QASK

This modulation mode configures the PUC as a BPSK, QPSK, OQPSK, MSK or m-QAM modulator. The data FIFO outputs are routed to the shaping filters. Here the samples are interpolated by 4, 8, or 16 and shaped using a FIR filter with up to a 256 taps. The filter impulse response can span 4-16 input samples. A half (input) sample delay can be set in the I channel for implementing OQPSK modulation. The output of the shaping filter is routed through a gain adjust multiplier and into the interpolation filter. The interpolation filter interpolates by a factor set in the resampling NCO. The output of the resampling filter is at the master clock frequency, REFCLK. The samples are then mixed with the carrier L.O. for quadrature upconversion. The output is then summed with the cascade input signal, saturated (in the case of overflow), and formatted for output.

Modulation Mode 01 - FM with Band Limiting Filter

This mode configures the PUC as an FM modulator with post-modulation filtering. This mode provides for FSK and FM modulation schemes. In this mode, the I input samples drive the frequency control section of a quadrature NCO to produce a zero frequency centered FM signal. Care must be taken to restrict the frequency and amplitude of the input data samples to valid NCO control ranges. The FM quadrature signals are then routed to the shaping FIR filter and into the interpolation filter for bandlimiting and sample rate adjustment to the master clock rate. The quadrature filtered FM signals are then upconverted to the carrier frequency by the carrier NCO and mixers. Note that for pulse shaping in this mode, any baseband filtering for bandlimiting must be provided prior to the PUC. The output is then summed with the cascade input signal, saturated (in the case of overflow), and formatted for output.

Modulation Mode 10 - FM with Pulse Shaping

This mode configures the PUC as an FM modulator with pre-modulation baseband pulse shaping. The data from the FIFO (I channel only) is routed to the FIR shaping filter. The FIR shaping filter output drives the frequency control section of a quadrature NCO to produce a zero I.F. FM signal. These FM modulated quadrature samples are then rate adjusted in the interpolation filter to the output sample rate. The baseband modulated signal is then upconverted to the carrier frequency by the carrier NCO and mixers. The output is then summed with the cascade input signal, saturated, and formatted for output.

FM Modulator

The FM modulator provides for frequency modulation of a programmable carrier center frequency by the PUC input data. The FM modulator is driven either directly by the PUC I input (Mode 1) or by the output of the FIR shaping filter (Mode 2). The modulating function, which is the input data to the FM Modulator, is defined as $d\phi(n)/dt$, where $\phi(nT)$ is the phase of a theoretical sinusoid described by

$$s(n) = A\cos[\phi(nT)] \quad \text{(EQ. 1)}$$

Figure 4 illustrates the conceptual design of the FM modulator. The input to the FM modulator, $d\phi(n)/dt$, is integrated via the carrier NCO accumulator. The NCO accumulator output represents phase and is used to address a SIN/COS generator, synthesizing a sinusoid of the form described in Equation 1. The phase term of the NCO is 16 bits. Sixteen bits of the phase word are routed to the SIN/COS generator. Sixteen bits of resolution are provided on the Sine and Cosine outputs.

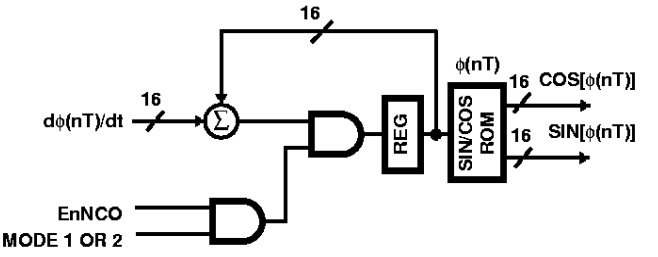


FIGURE 4. FM MODULATOR BLOCK DIAGRAM

The transfer function of the FM modulator is defined by the number of degrees variation per sample value, $d\phi(nT)/dt$, where $d\phi(nT)/dt$ is a 16-bit, twos complement, fractionally notated frequency control word with a range from $-F_{SAMP}/2$

to $+F_{SAMP}/2$. F_{SAMP} is defined as the sample rate into FM modulator. The maximum phase step that can occur in one clock is ±180 degrees. Table 1 provides the change in phase weighting of the input bits.

TABLE 1. FM MODULATOR TRANSFER FUNCTION

dϕ(nT)/dt	DEGREES/SAMPLE
1000 0000 0000 0000	-180
0000 0000 0000 0000	0
0111 1111 0000 0000	~+180

FM Modulator Application Issues

In Mode 01, care must be taken to ensure that the input samples are sufficiently bandlimited prior to being input to the PUC because the shaping filter has a limited capability to band limit. Also, when designing a Bessel Filter with the 256 tap FIR filter, watch that the modulation index does not produce excessive Bessel spurs.

In Mode 10, the amplitude out of the shaping filter needs to be limited in order to prevent frequency excursions that cannot be filtered out in the interpolation filter. The quality of the FM signal is affected by the amplitude slew rate out of the shaping filter. As a rule of thumb, limiting this slew rate to less than 1/8 the sample rate will minimize this distortion.

Shaping Filter

The shaping filter provides the necessary pulse shaping required on the input data to implement various quadrature ASK and shaped FM modulation formats. Two identical shaping filters (one each for the I and Q channels) are provided. The filters can implement a 4-16 input sample span impulse response using up to 256 taps with 16 bits of resolution in the coefficients.

The range of valid digital values for the coefficients is from 8001 to 7FFF. The value 8000 is not allowed. The coefficient format is 2's complement. The span of the Impulse response of the polyphase filter can be from 4-16 samples. The desired sample span value minus one is programmed into the Data Samples (DS) field in Control Word 19, bits 2-5. The filter has a programmable interpolation rate (IP) of 4, 8, or 16. This interpolation rate is programmed by Control Address 19, bits 0 and 1. Thus, the required number of coefficients (or filter span) becomes

$$\#\ \text{Coefficients} = (DS)(IP) \quad \text{(EQ. 2)}$$

with 256 being the maximum number of coefficients.

Note that

$$REFCLK > (DS)(IP)(F_{FS}) \quad \text{(EQ. 3)}$$

where F_{FS} is the sample rate of the filter. For 16 sample polyphase filter, the total impulse response is 64, 128 or 256 filter taps for interpolation rates of 4, 8 or 16, respectively. The filter structure precludes coefficient re-use for symmetric filters, so both asymmetric and symmetric filters have up to 256 taps available and are loaded in identical manner.

The maximum filter input rate is:

$$F_{CLK}/[(IP)(DS)] \quad \text{(EQ. 4)}$$

where F_{CLK} is the frequency of the reference clock, IP is the shaping filter interpolate rate; and DS is the number of data samples in the filter span. For example, if F_{CLK} = 52MHz, the filter span is 16 samples, and the interpolation rate is 16, then the maximum FIR input sample rate, F_{FS}, is 52/256 = 203kHz. Table 2 shows several examples of calculations for FIR input sample rates based on master reference clock rate, number of data samples, and interpolation rate.

TABLE 2. EXAMPLES OF THE DIFFERENT CASES AND DIFFERENT FIR INPUT SAMPLING FREQUENCIES

EXAMPLE	F_{CLK}	DS	IP	MAX F_{FS}
1	52MHz	16	16	52/256 = 203kHz
2	52MHz	16	8	52/128 = 406kHz
3	52MHz	16	4	52/64 = 813kHz
4	52MHz	10	4	52/40 = 1300kHz
5	52MHz	8	4	52/32 = 1625kHz

Shaping Filter Application Issues

Note that when using quadrature modulation, saturation/overflow will occur when the input values for I and Q exceed 0.707 peak. Also note that there is gain in Interpolation filter. Because of these two implementation constraints, the Shaping filter coefficients may need to be reduced from full scale to provide unity gain in the PUC and to prevent saturation in the shaping filter. After the shaping filter computation, a gain scaling control is provided. It is possible to allow the shaping filter computation to approach unity on each channel and then scale the I/Q magnitudes in the Gain Control.

The shaping filtered is designed so that the filter signal matches its output samples rate, i.e., 4x, 8x, 16x baud. If the interpolation rate (IP) is used, the filter does not have to be changed for different rates. Only the carrier NCO frequency would need to be modified.

Gain Control

Between the Shaping filter and the Interpolation filter is a gain adjustment stage that provides for identical scaling of the I and Q shaped signals. Gain adjustment is from 0 to slightly less than unity. This gain control can be used to prevent signal overflow in the Interpolation filter or saturation in the quadrature mixer. Gain control can also be used to set the level of a signal prior to summing multiple signals in the modulated output section.

The scaling multiplier value is programmed using an bits 0-7 in Control Word 17. The attenuation is set by:

$$Atten = OutGain/2^8 \quad \text{(EQ. 5)}$$

$$OutGain = [(Atten)2^8]Hex \quad \text{(EQ. 5A)}$$

$$Atten_{dB} = 20\log[OutGain/2^8] \quad \text{(EQ. 5B)}$$

$$OutGain = \left[10^{(Atten_{dB}/20)}2^8\right]Hex \quad \text{(EQ. 5C)}$$

where Atten is the desired signal attenuation, $Atten_{dB}$ is the desired signal attenuation in dB, and OutGain is the control word value.

Table 3 details a few key control words and the associated attenuations for the I and Q signals.

TABLE 3. SCALING GAIN ATTENUATION

CONTROL WORD	SCALING GAIN ((V_{OUT}/V_{IN})%)	ATTENUATION (dBFS)
1111 1111	99.6	-0.033996
1000 0000	50.0	-6.021
0100 0000	25.0	-12.041
0010 0000	12.5	-18.062
0001 0000	6.25	-24.082
0000 1000	3.125	-30.103
0000 0100	1.5625	-36.124
0000 0010	0.78125	-42.144
0000 0001	0.390625	-48.165

Re-Sampling NCO

The Sample Rate NCO provides the sample clock and sample clock phase information to both the shaping and Interpolation filters. Figure 5 details the conceptual design. The sample frequency is set with 30-bit resolution. The LSB is $REFCLK/2^{32}$. The internal accumulator resolution in 32 bits. The MSB of the accumulator is the sample clock for the filters. Four bits of coarse timing phase resolution control the Shaping filter, while twelve bits of fine timing phase resolution control the Interpolation filter.

The resampling NCO frequency control word is double buffered. The 30-bit timing NCO frequency is written to Control Addresses 2 and 3. The frequency control word is transferred from the buffer into the Re-Sampling NCO on a pulse from SYNCIN or on a write to Control Word 2. Control Word 22, bit 0, sets which action, the SYNCIN or write to CW2, will induce a frequency control word transfer in the NCO. The Re-Sampler NCO is disabled by a $\overline{RST}$ assertion, a "write to CW21" reset assertion, or until a sync control assertion is detected (independent of the initiating sync source).

The PUC input sample rate is set by the Re-Sampling NCO. The maximum error is $52MHz/(2^{32})$ = 0.012Hz. The frequency control word is computed by

$$F_{RESAMP} = SR(29:0) \times F_{CLK} \times 2^{-32} \quad \text{(EQ. 6)}$$

where SR(29:0) is the 30-bit frequency control word and is REFCLK.

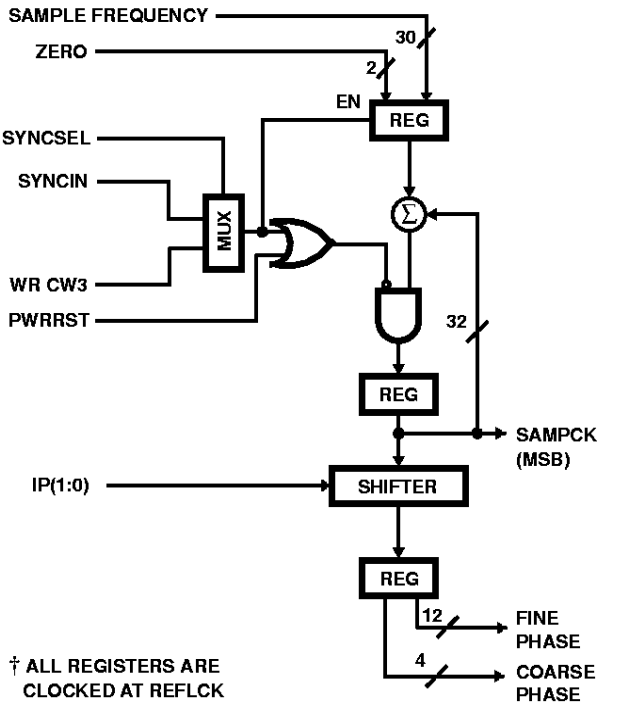


FIGURE 5. RE-SAMPLING NCO BLOCK DIAGRAM

Re-Sampling NCO Application Issues

1. Common clocking of the PUC and PDC:

NOTE that at a board level, the HSP50214 (PDC) and HSP50215 (DUC) sample rate NCO's typically utilize different clocks. The DUC circuitry is clocked at the master clock, REFCLK, rate. The PDC output circuitry runs off the decimated sample rate. If a common sample clock is used for both parts, then synchronization can be achieved by scaling and/or truncating the PDC frequency control word to match the PUC frequency control word. Powers of 2 are handled by simply truncating the PDC frequency control word to match the bit width of the DUC frequency control word. If the PDC decimation factor is not power of 2, then errors will accumulate.

2. Improving the NCO Accuracy

The Re-Sampler NCO frequency can be adjusted to maintain phase and frequency lock to a reference clock, if more accuracy is required.

Interpolation Filter

The Interpolation filter provides non-integer sampling rate conversion from input to output, as well as filter characteristics similar to a cascaded integrator-comb (CIC) filter. The impulse response of the Interpolation filter is shown in Figures 6A and 6B. The Interpolation filter has a pipeline delay of 3 coarse input samples plus 3 REFCLK cycles.

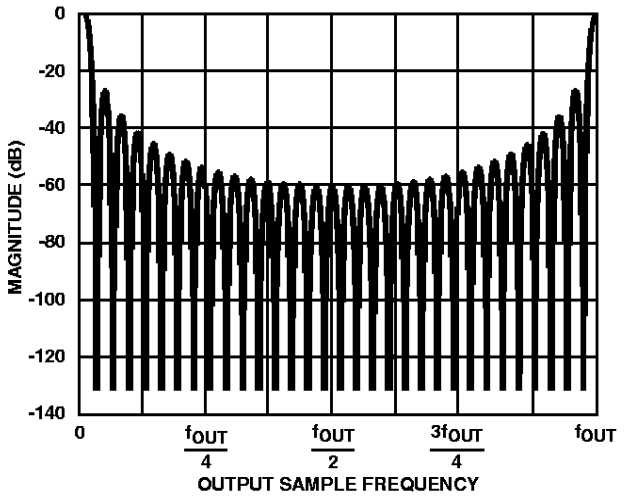


FIGURE 6A. INTERPOLATION FILTER IMPULSE RESPONSE

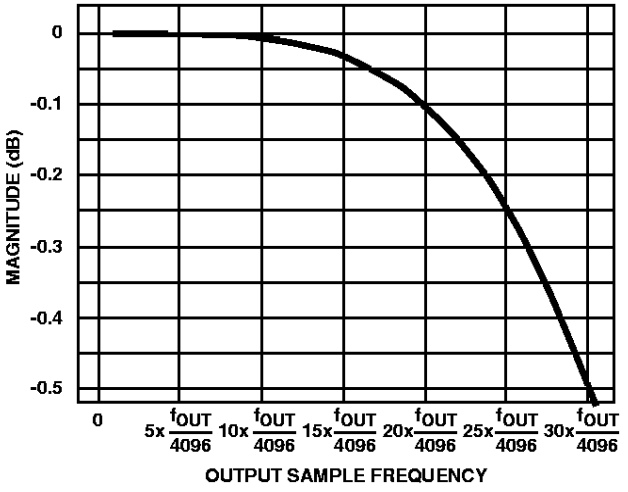


FIGURE 6B. INTERPOLATION FILTER IMPULSE RESPONSE

Carrier NCO

The Carrier NCO provides the quadrature local oscillator references for the Vector Modulator/Mixer. The Carrier NCO input carrier frequency control word has 32 bits of resolution. The block diagram is shown in Figure 7. The internal accumulator resolution in 32 bits.

The carrier frequency is a single buffered 32-bit frequency control, loaded 16 bits at a time into Control Words 4 and 5. Since the DUC requires two loads, there is a possibility of a phase glitch.

The Carrier NCO is disabled during a $\overline{RST}$ assertion or a reset caused by writing to CW21. The Carrier NCO is also disabled until a sync assertion is detected independent of the initiating sync source (SYNCIN or WR CW3). The Carrier NCO is also disabled by programming a zero in Control Word 16 bit 3. This bit freezes the NCO and also disables the output of the modulator.

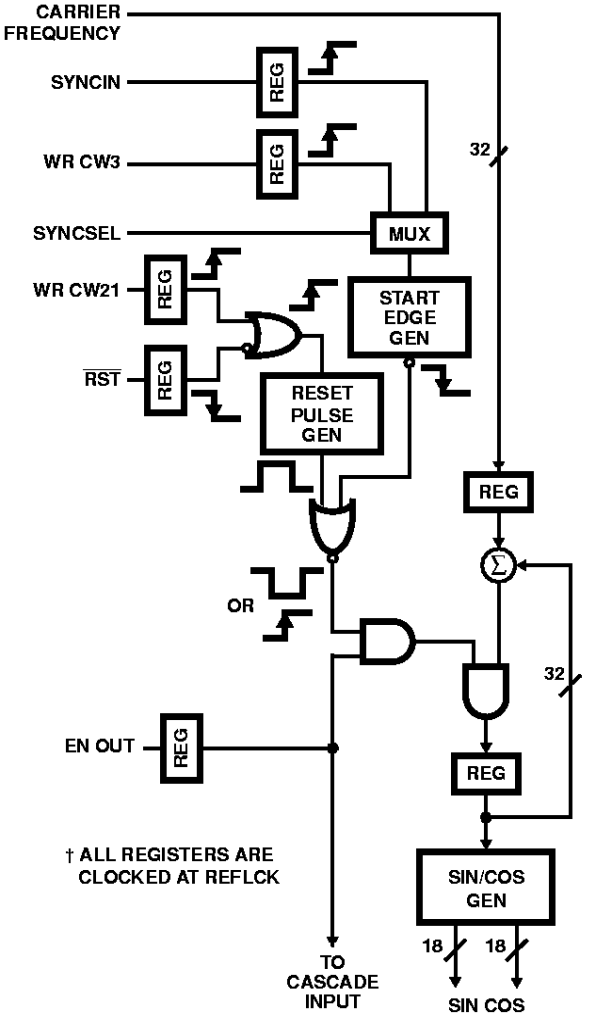


FIGURE 7. CARRIER NCO BLOCK DIAGRAM

To avoid the phase glitch, noted above, the phase accumulator can be disabled at reset, and the frequency can be preloaded prior to asserting sync.

The maximum error is 52MHz/(2^{32}) = 0.012Hz. The carrier frequency can be calculated from the value loaded into Control Address 4 and 5 by

$$F_{CARRIER} = CR(31:0) \times F_{CLK} \times 2^{-32} \quad \text{(EQ. 7)}$$

where CR(31:0) is the 32-bit frequency control word which can range from -2^{31} to $\sim 2^{31}$ for a NCO output range of $-F_{CLK}/2$ to $\sim F_{CLK}/2$. F_{CLK} is the REFCLK frequency.

This NCO frequency range allows for spectral inversion. Given a desired carrier frequency, the value for CR(31:0) loaded into the part can be calculated by

$$CR(31:0) = INT[F_C / F_{CLK} * 2^{32}] \quad \text{(EQ. 8)}$$

where INT[X] is the integer part of the real number X.

The most significant 18 bits of the 32-bit phase word from the Carrier NCO drives a Sin/Cos generator. Eighteen bit resolution are supplied on the sinusoid outputs.

Vector Modulator/Mixer

The frequency resolution of the vector modulator is 32 bits. The conceptual block diagram of the Vector Modulator/Mixer is shown in Figure 8. The modulator operates at maximum frequency of 52MHz. The mixer takes the sin/cos terms generated by the carrier NCO sin/cos generator and mixes it with the input data lines I and Q. The resulting output is given by

$$\text{Output} = I * \cos - Q * \sin \quad \text{(EQ. 9)}$$

There is no overflow protection provided at the output of the modulator summer, so care must be taken to ensure that the input signals are scaled prior to input to prevent overflow.

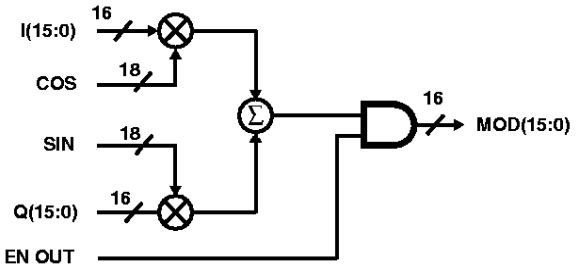
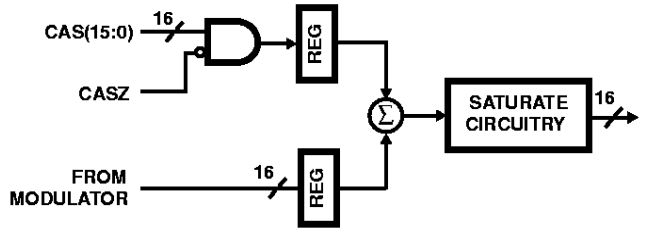


FIGURE 8. VECTOR MODULATOR/MIXER BLOCK DIAGRAM

Cascade Input

The cascade input allows multiple modulated signals to be summed together prior to routing to a DAC. Figure 9 details the block diagram of the cascade circuitry. The CAS(15:0) input is used as the point of entry for the output of other DUC's. The CASZ is used to zero the CAS(15:0) input when it is not used. Both the CAS(15:0) and the modulator data path are registered, prior to summation. The output of the summation is saturated to prevent roll-over



† ALL REGISTERS ARE CLOCKED AT REFLCK

FIGURE 9. CASCADE INPUT BLOCK DIAGRAM

Output Formatter

The output formatter provides the data output in either Two's Complement or Offset Binary format. The OFM signal is used to select the output format. OFM = 1 is Two's Complement. OFM = 0 is Offset Binary format. The $\overline{OE}$ signal is used to enable the data bus output. $\overline{OE}$ = 0 enables the output.

NOTE: The HSP43216 can be used to double the output sample rate of the DUC, in applications where a higher sample rate into the DAC is required.

Microprocessor Interface

The microprocessor interface is a memory mapped direct access interface. The control pins are $\overline{RD}$, $\overline{WR}$ and $\overline{CE}$, while the 10-bit address bus is A(9:0) [address space is 1024 words] and the 16-bit data bus is C(15:0). The $\overline{CE}$ signal gates the $\overline{RD}$ and $\overline{WR}$. Care must be taken in changing the address and data lines, as the addresses are updated asynchronous to REFCLK except in the cases noted in the Microprocessor Write Section. Most destination addresses are intended to be programmed after RESET and before the Start Sequence, and left alone after that. See the RESET and Start Sequence sections from more details on initiating operation of the part.

The Re-Sampler NCO center frequency is a 32-bit doubled buffer interface, allowing for the center frequency value to be programmed at will and transferred via control command. The control command can be either a SYNC signal or a write to Control Address 03.

The read's are asynchronous to clock. The shaping filter coefficients cannot be read. See the Configuration Control Register Bit Definitions section for programming details of the 13 Control Words and the 512 Coefficient Registers.

Microprocessor Write

The Microprocessor Write Interface is used for loading data into the DUC control registers. The Microprocessor Write Interface for the DUC consists of ten 16-bit configuration registers, one 10-bit address word and address decode logic. Only the Re-Sampler NCO Center Frequency register is double buffered, allowing for a data transfer to be aligned with an external system timing event. Write registers are accessed via the 10-bit address bus (A9:0) and the 16-bit data bus (C15:0). The address map for these registers is given in the Configuration Control Register Bit Definition section. A configuration load is implemented by setting up the address (A9:0) and data (C15:0) and generating a rising edge on $\overline{WR}$. The HSP50214 is configured by loading a series of ten 16-bit control registers and 512 coefficient registers. A control register loading sequence is shown in Figure 10. Figure 10 assumes that $\overline{CE}$ is asserted. The filter coefficients for the shaping filter are loaded in a similar manner into Control Word addresses 512 - 1023.

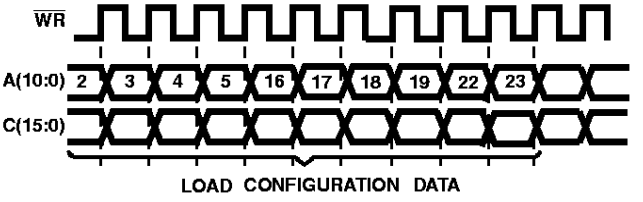


FIGURE 10. CONTROL REGISTER LOADING SEQUENCE

The Re-Sampler NCO Center Frequency data transfers from the Microprocessor Interface holding registers to the Center Frequency Register on the assertion of SYNCIN or a Write to Configuration Control Word 3. The timing waveforms for this process are shown in Figure 11.

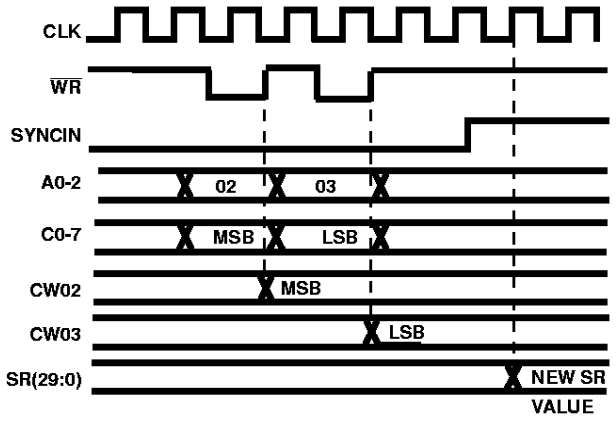


FIGURE 11. RESAMPLER CENTER FREQUENCY CONTROL REGISTER LOADING SEQUENCE

When SYNCIN is sampled "high" by the rising edge of clock, the contents of the holding registers are transferred to the Sample Center Frequency Register. Caution should be taken when using the SYNCIN since the holding register contents will be transferred to the Sample Center Frequency Register whenever SYNCIN is asserted (and selected via CW22).

Shaping filter I coefficients are loaded from the first coefficient (C0) in address 0x200h to the last address in 0x2FFh.

Because interpolation by 16 is possible, the coefficient addresses are structured in blocks of 16, one address for each phase of the interpolation. With a 256 tap filter using an interpolation of 16, there are 16 multiplies required to implement the filter. Tables 4 and 5 detail the coefficient address allocation, with the Interpolation Phase indicated by the IP number on the left, and the multiplier number indicated by the numbers 0 through 15 across the top.

TABLE 4. I SHAPING FILTER COEFFICIENT ADDRESSES

	DS_0	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	DS_9	DS_{10}	DS_{11}	DS_{12}	DS_{13}	DS_{14}	DS_{15}
IP0	512	528	544	560	576	592	608	624	640	656	672	688	704	720	736	752
IP1	513	529	545	561	577	593	609	625	641	657	673	689	705	721	737	753
IP2	514	530	546	562	578	594	610	626	642	658	674	690	706	722	738	754
IP3	515	531	547	563	579	595	611	627	643	659	675	691	707	723	739	755
IP4	516	532	548	564	580	596	612	628	644	660	676	692	708	724	740	756
IP5	517	533	549	565	581	597	613	629	645	661	677	693	709	725	741	757
IP6	518	534	550	566	582	598	614	630	646	662	678	694	710	726	742	758
IP7	519	535	551	567	583	599	615	631	647	663	679	695	711	727	743	759
IP8	520	536	552	568	584	600	616	632	648	664	680	696	712	728	744	760
IP9	521	537	553	569	585	601	617	633	649	665	681	697	713	729	745	761
IP10	522	538	554	570	586	602	618	634	650	666	682	698	714	730	746	762
IP11	523	539	555	571	587	603	619	635	651	667	683	699	715	731	747	763
IP12	524	540	556	572	588	604	620	636	652	668	684	700	716	732	748	764
IP13	525	541	557	573	589	605	621	637	653	669	685	701	717	733	749	765
IP14	526	542	558	574	590	606	622	638	654	670	686	702	718	734	750	766
IP15	527	543	559	575	591	607	623	639	655	671	687	703	719	735	751	767

TABLE 5. Q SHAPING FILTER COEFFICIENT ADDRESSES

	DS_0	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	DS_9	DS_{10}	DS_{11}	DS_{12}	DS_{13}	DS_{14}	DS_{15}
IP0	768	784	800	816	832	848	864	880	896	912	928	944	960	976	992	1008
IP1	769	785	801	817	833	849	865	881	897	913	929	945	961	977	993	1009
IP2	770	786	802	818	834	850	866	882	898	914	930	946	962	978	994	1010
IP3	771	787	803	819	835	851	867	883	899	915	931	947	963	979	995	1011
IP4	772	788	804	820	836	852	868	884	900	916	932	948	964	980	996	1012
IP5	773	789	805	821	837	853	869	885	901	917	933	949	965	981	997	1013
IP6	774	790	806	822	838	854	870	886	902	918	934	950	966	982	998	1014
IP7	775	791	807	823	839	855	871	887	903	919	935	951	967	983	999	1015
IP8	776	792	808	824	840	856	872	888	904	920	936	952	968	984	1000	1016
IP9	777	793	809	825	841	857	873	889	905	921	937	953	969	985	1001	1017
IP10	778	794	810	826	842	858	874	890	906	922	938	954	970	986	1002	1018
IP11	779	795	811	827	843	859	875	891	907	923	939	955	971	987	1003	1019
IP12	780	796	812	828	844	860	876	892	908	924	940	956	972	988	1004	1020
IP13	781	797	813	829	845	861	877	893	909	925	941	957	973	989	1005	1021
IP14	782	798	814	830	846	862	878	894	910	926	942	958	974	990	1006	1022
IP15	783	799	815	831	847	863	879	895	911	927	943	959	975	991	1007	1023

TABLE 6. I COEFFICIENT ADDRESSING FOR A 16 TAP INTERPOLATED BY 4 FILTER

	DS_0	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	DS_9	DS_{10}	DS_{11}	DS_{12}	DS_{13}	DS_{14}	DS_{15}
IP0	512 = C0	528 = C4	544 = C8	560 = C12	576	592	608	624	640	656	672	688	704	720	736	752
IP1	513 = C1	529 = C5	545 = C9	561 = C13	577	593	609	625	641	657	673	689	705	721	737	753
IP2	514 = C2	530 = C6	546 = C10	562 = C14	578	594	610	626	642	658	674	690	706	722	738	754
IP3	515 = C3	531 = C7	547 = C11	563 = C15	579	595	611	627	643	659	675	691	707	723	739	755
IP4	516	532	548	564	580	596	612	628	644	660	676	692	708	724	740	756
IP5	517	533	549	565	581	597	613	629	645	661	677	693	709	725	741	757
IP6	518	534	550	566	582	598	614	630	646	662	678	694	710	726	742	758
IP7	519	535	551	567	583	599	615	631	647	663	679	695	711	727	743	759
IP8	520	536	552	568	584	600	616	632	648	664	680	696	712	728	744	760
IP9	521	537	553	569	585	601	617	633	649	665	681	697	713	729	745	761
IP10	522	538	554	570	586	602	618	634	650	666	682	698	714	730	746	762
IP11	523	539	555	571	587	603	619	635	651	667	683	699	715	731	747	763
IP12	524	540	556	572	588	604	620	636	652	668	684	700	716	732	748	764
IP13	525	541	557	573	589	605	621	637	653	669	685	701	717	733	749	765
IP14	526	542	558	574	590	606	622	638	654	670	686	702	718	734	750	766
IP15	527	543	559	575	591	607	623	639	655	671	687	703	719	735	751	767

The convolution multiplies C0 by the most recent data sample. For a 16 tap, interpolate-by-4 filter, the calculations are:

OUTPUT0 = (C0*D[n]) + (C4*D[n-1]) + (C8*D[n-2]) + (C12*D[n-3])

OUTPUT1 = (C1*D[n]) + (C5*D[n-1]) + (C9*D[n-2]) + (C13*D[n-3])

OUTPUT2 = (C2*D[n]) + (C6*D[n-1]) + (C10*D[n-2]) + (C14*D[n-3])

OUTPUT3 = (C3*D[n]) + (C7*D[n-1]) + (C11*D[n-2]) + (C15*D[n-3])

Table 6 indicates how the I coefficients should be addressed to yield the desired filter. Notice that since 16 filter coefficients are required (all other addresses not used) and the filter interpolates by 4, the coefficients are loaded sequentially through the 4 interpolation phases.

Shaping filter Q coefficients are loaded from the first coefficient (B0) in address 0x300h to the last address in 0x3FFh. The convolution multiplies B0 by the most recent data sample. For a 16 tap, interpolate-by-4 filter, the calculations are:

OUTPUT0 = (B0*D[n]) + (B4*D[n-1]) + (B8*D[n-2]) + (B12*D[n-3])

OUTPUT1 = (B1*D[n]) + (B5*D[n-1]) + (B9*D[n-2]) + (B13*D[n-3])

OUTPUT2 = (B2*D[n]) + (B6*D[n-1]) + (B10*D[n-2]) + (B14*D[n-3])

OUTPUT3 = (B3*D[n]) + (B7*D[n-1]) + (B11*D[n-2]) + (B15*D[n-3])

Table 7 indicates how the Q coefficients should be addressed to yield the desired filter. Identical to the I filter, notice that since 16 filter coefficients are required (all other addresses not used) and the filter interpolates by 4, thee coefficients are loaded sequentially through the 4 interpolation phases.

Microprocessor Read

The DUC offers the microprocessor access to all of the control data configuration registers through a read process. The shaping filter coefficients, however, cannot be read. With $\overline{CE}$ asserted, a read process consists of dropping the $\overline{RD}$ line low to transfer data from the register addresses indicated by A(9:0). The read address mapping is provided in Table 8. The timing is shown in Figure 12.

TABLE 7. Q COEFFICIENT ADDRESSING FOR A 16 TAP INTERPOLATED BY 4 FILTER

	DS_0	DS_1	DS_2	DS_3	DS_4	DS_5	DS_6	DS_7	DS_8	DS_9	DS_{10}	DS_{11}	DS_{12}	DS_{13}	DS_{14}	DS_{15}
IP0	768 = D0	784 = D4	800 = D8	816 = D12	832	848	864	880	896	912	928	944	960	976	992	1008
IP1	769 = D1	785 = D5	801 = D9	817 = D13	833	849	865	881	897	913	929	945	961	977	993	1009
IP2	770 = D2	786 = D6	802 = D10	818 = D14	834	850	866	882	898	914	930	946	962	978	994	1010
IP3	771 = D3	787 = D7	803 = D11	819 = D15	835	851	867	883	899	915	931	947	963	979	995	1011
IP4	772	788	804	820	836	852	868	884	900	916	932	948	964	980	996	1012
IP5	773	789	805	821	837	853	869	885	901	917	933	949	965	981	997	1013
IP6	774	790	806	822	838	854	870	886	902	918	934	950	966	982	998	1014
IP7	775	791	807	823	839	855	871	887	903	919	935	951	967	983	999	1015
IP8	776	792	808	824	840	856	872	888	904	920	936	952	968	984	1000	1016
IP9	777	793	809	825	841	857	873	889	905	921	937	953	969	985	1001	1017
IP10	778	794	810	826	842	858	874	890	906	922	938	954	970	986	1002	1018
IP11	779	795	811	827	843	859	875	891	907	923	939	955	971	987	1003	1019
IP12	780	796	812	828	844	860	876	892	908	924	940	956	972	988	1004	1020
IP13	781	797	813	829	845	861	877	893	909	925	941	957	973	989	1005	1021
IP14	782	798	814	830	846	862	878	894	910	926	942	958	974	990	1006	1022
IP15	783	799	815	831	847	863	879	895	911	927	943	959	975	991	1007	1023

TABLE 8. READ ADDRESS MAP FOR MICRO PROCESSOR INTERFACE

A4	A2	A1	A0	DESCRIPTION
0	X	0	0	Re-Sampler Center Frequency: SF(29:16)
0	X	0	1	Re-Sampler Center Frequency: SF(15:0)
0	X	1	0	Carrier Center Frequency: CF(31:16)
0	X	1	1	Carrier Center Frequency: CF(15:0)
1	0	0	0	Modulation Control: En Out bit 3; Mod(2:0)
1	0	0	1	Gain Control: GN(7:0)
1	0	1	0	FIFO Control: FIFO Ready bit 5; I FIFO Empty bit 4; Q FIFO Empty bit 3; RTH(2:0)
1	0	1	1	Poly-Phase Control: DS(3:0) = b5-2; IP(1:0)
1	1	0	X	EnNCO
1	1	1	0	Sync Control: Ext Sync Polarity bit 1; Sync Sel bit 0
1	1	1	1	Test Control