

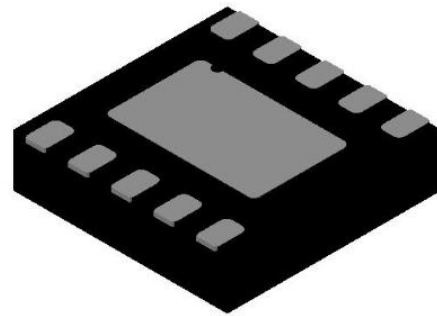
# WL2866D

## 4-Channel LDO PMIC for Camera Applications

[Http://www.willsemi.com](http://www.willsemi.com)

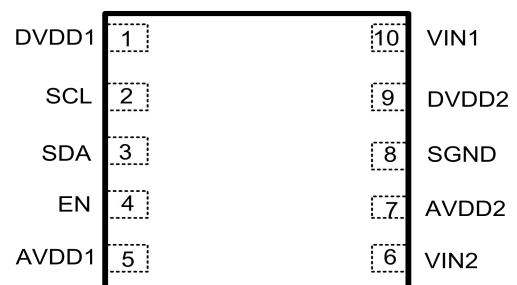
### Descriptions

The WL2866D is a 4-Ch integrated LDOs for camera sensor applications include 2-Ch DVDD, 2-Ch AVDD, With 400KHz high speed I2C interface, the function setting is flexible such as power sequence, output voltage, output discharge. The chip enable control support EN pin control and I2C control.



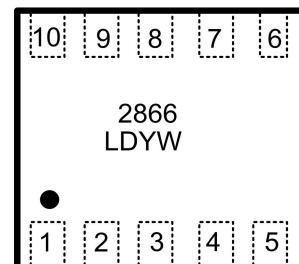
Due to high load current and lower working voltage of DVDD, WL2866D used N-MOSFET LDO architecture without charge pump for 2-Ch DVDD LDO. DVDD LDO input source is VIN1 and VIN2 is the bias voltage. Ultra low dropout voltage (Typ.80mV @ 0.5A Load) of DVDD LDOs is designed for high efficiency and lower power dissipation purpose. For the AVDD, WL2866D used P-MOSFET LDO architecture. The input source is VIN2. Due to high performance requirement of AVDD, WL2866D's AVDD used special circuit design and optimized pin assignment which is easy for system PCB layout.

### DFN2x2-10L (Bottom View)



Highly integrated, small package size .WL2866D is available in DFN2x2-10L package. Standard products are Pb-free and halogen-free.

### Pin configuration (Top view)



### Features:

- VIN1 input voltage range : 0.6V~2.0V
- DVDD1/2 output voltage range : 0.6V~1.8V
- DVDD1/2 dropout voltage : 80mV@0.5A
- DVDD1/2 output current : 700mA Min.
- VIN2 Supply Quiescent Current : 65uA
- VIN2 Supply Current, Shutdown : 0.22uA
- VIN2 input voltage range : 3.0V~5.5V
- AVDD1/2 output voltage range : 1.2V~4.3V
- VIN2 UVLO : 2V
- AVDD1/2 output current : 300mA Min.
- AVDD LDO PSRR : 90dB
- AVDD LDO output noise : 8uV

### Marking

- 2866 : Device Code
- LD : Special Code
- Y : Year Code
- W : Week Code

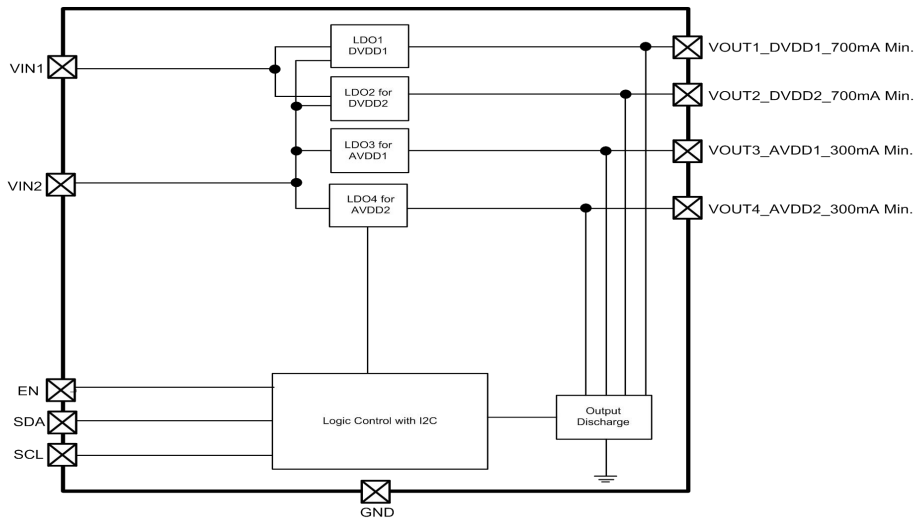
### Order Information

Device	Package	Shipping
WL2866D-10/TR	DFN2x2-10L	3000/Reel&Tape

### Applications:

- Smart Phone
- IP Camera
- Camera Module

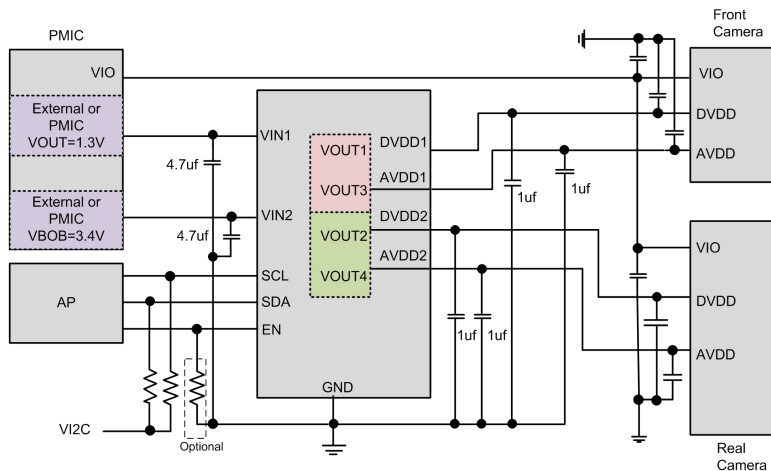
## Block Diagram



## PIN Descriptions

Pin No.	Symbol	Description
1	DVDD1	LDO1 output
2	SCL	I2C interface
3	SDA	
4	EN	Global enable control, Active high. Maintain to low if I2C control used
5	AVDD1	LDO3 output
6	VIN2	LDO3~LDO4 Supply input, LDO1, LDO2 bias
7	AVDD2	LDO4 output
8	SGND	Ground
9	DVDD2	LDO2 output
10	VIN1	LDO1, LDO2 supply input

## Typical Applications



**Absolute Maximum Ratings**

Parameter		Value	Unit
V <sub>IN</sub> Range (VIN1 ,VIN2)		-0.3~6.5	V
V <sub>EN</sub> Range		-0.3 to V <sub>IN</sub> + 0.3	V
V <sub>OUT</sub> Range		-0.3 to V <sub>IN</sub> + 0.3	V
I <sub>OUT</sub>		Check EC table	mA
Lead Temperature Range		260	°C
Storage Temperature Range		-55 ~ 150	°C
Operating Junction Temperature Range		150	°C
MSL		Level-3	
ESD Ratings	HBM	7000	V
	MM	300	V

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**Recommend Operating Ratings**

Parameter		Value	Unit
VIN1 Operating Supply Voltage Range		0.6~2.0	V
VIN2 Operating Supply Voltage Range		3~5.5	V
Operating Temperature Range		-40~85	°C
Thermal Resistance, R <sub>θJA</sub> (note )		58	°C/W

Note:

Single component mounted on 2 oz, FR 4 PCB with 645 mm<sup>2</sup> Cu area

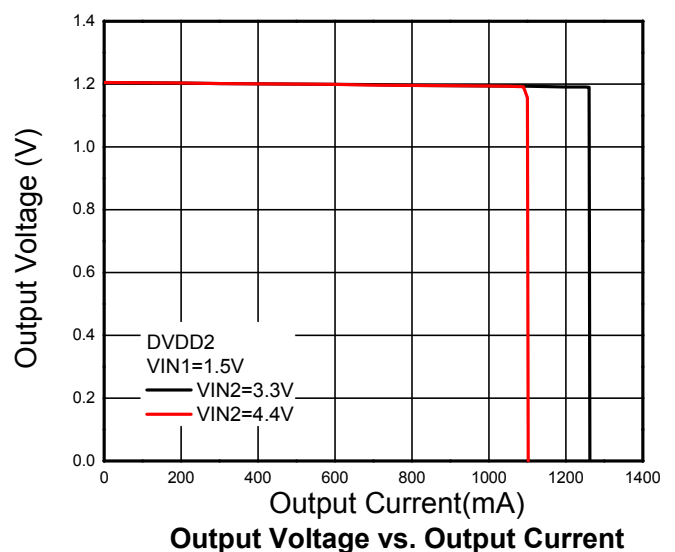
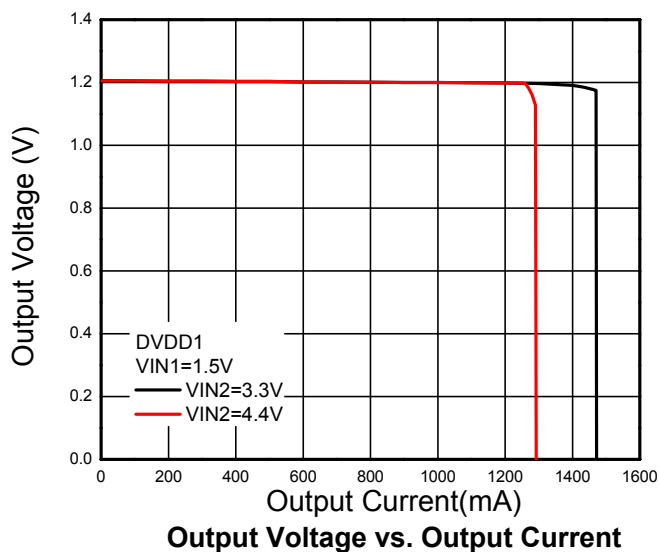
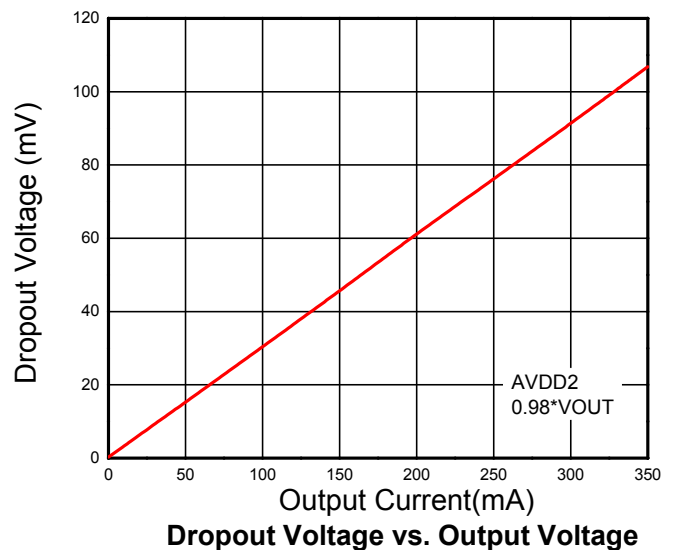
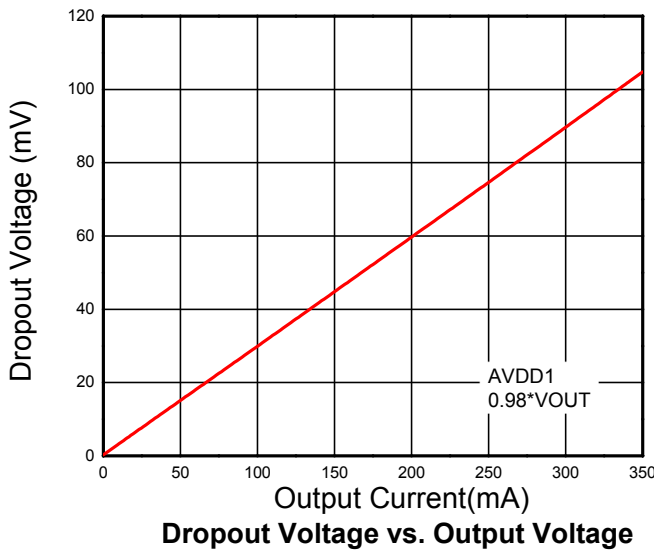
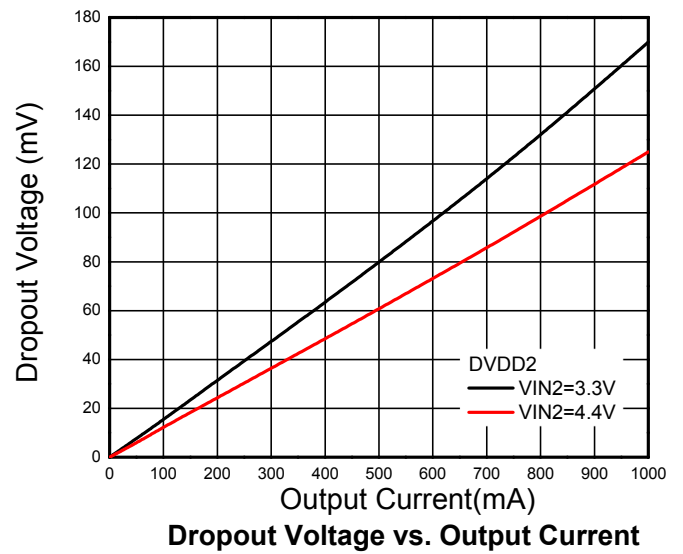
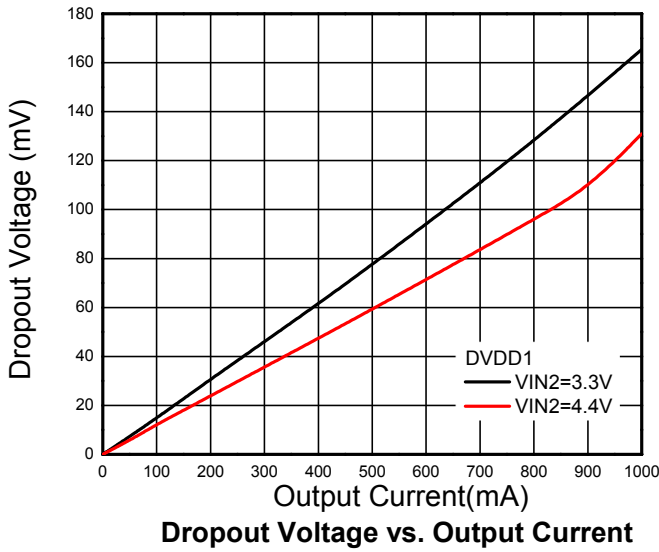
**Electronics Characteristics ( $V_{IN1}=1.35V$ ,  $V_{IN2}=3.3V$ ,  $C_{IN}=4.7\mu F$ ,  $C_{OUT}=1\mu F$ ,  $T_a = +25^\circ C$ , unless otherwise noted)**

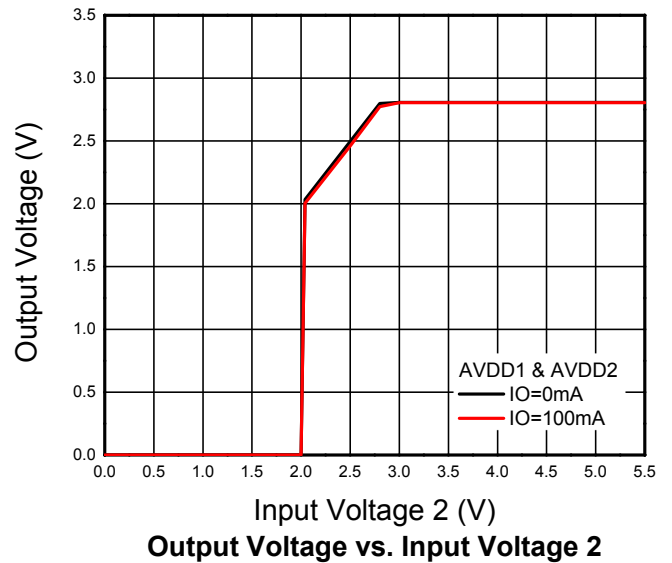
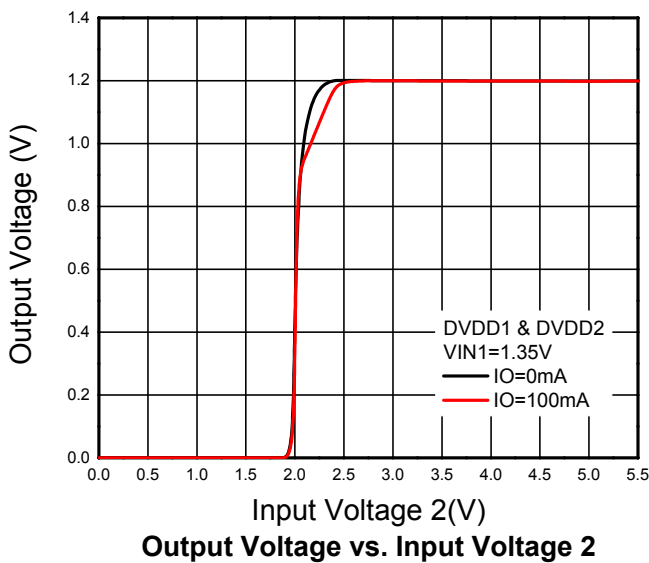
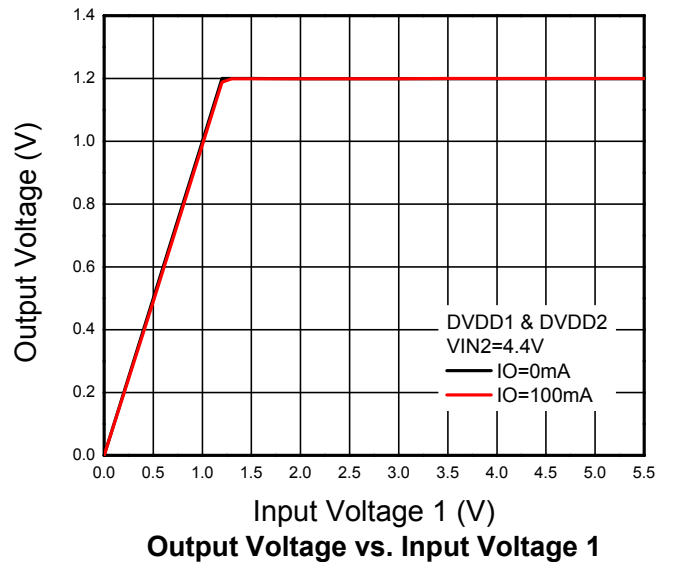
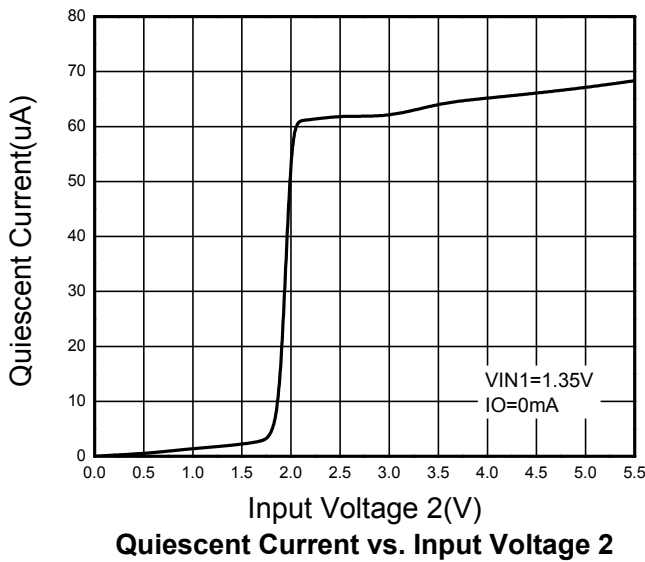
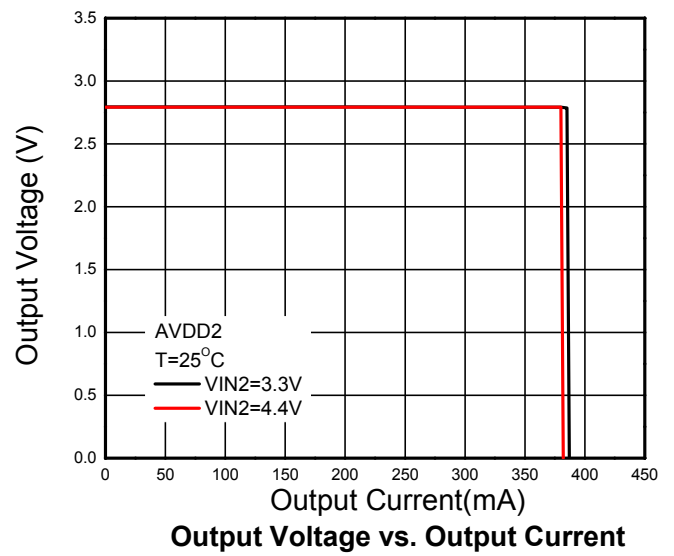
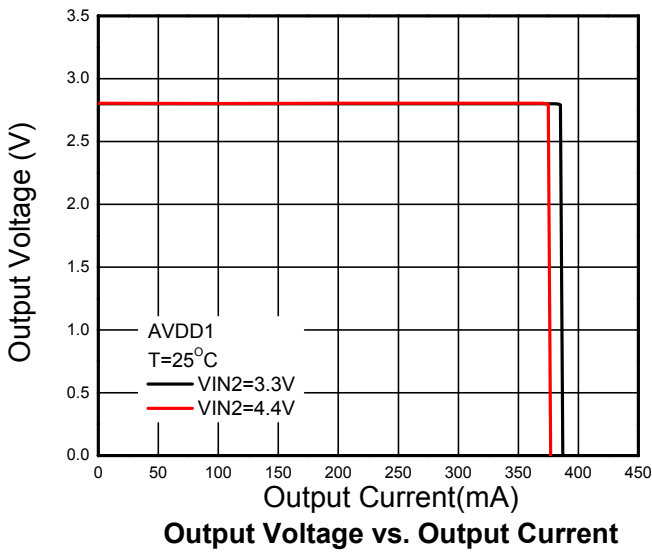
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>Whole Device</b>						
Quiescent current at all LDO active	$I_Q$	EN=H or Enable chip by I2C, No load		65	105	$\mu A$
Shutdown current	$I_{SHDN}$	EN=L or Shutdown by I2C		0.23	1.0	$\mu A$
EN logic high voltage	$V_{ENH}$		1.2			V
EN logic low voltage	$V_{ENL}$				0.4	V
EN pin leakage current	$I_{EN}$	$V_{EN}=0$ to 5.5V			8	$\mu A$
Turn-On Time	$T_{ON}$	EN=L to H, $V_{OUT}=1.2V$ DVDD1/2 $V_{OUT}=V_{OUT} * 90\%$		0.5		mS
		EN=L to H, $V_{OUT}=2.8V$ , AVDD1/2 $V_{OUT}=V_{OUT} * 90\%$		0.8		mS
Thermal shutdown threshold	$T_{SDH}$	$I_{OUT}=1mA$		140		$^\circ C$
Thermal shutdown hysteresis	$T_{SDH-HYS}$	$I_{OUT}=1mA$		30		$^\circ C$
Output discharge resistor ON resistance	$R_{DCHG}$	EN=L or Shutdown by I2C		400		$\Omega$
Under voltage lock-out	UVLO_VIN1	VIN1 Falling		N.A		V
	UVLO_VIN2	VIN2 Falling		2.0		V
ULVO hysteresis	UVLO_HYS	VIN Rising		0.1		V

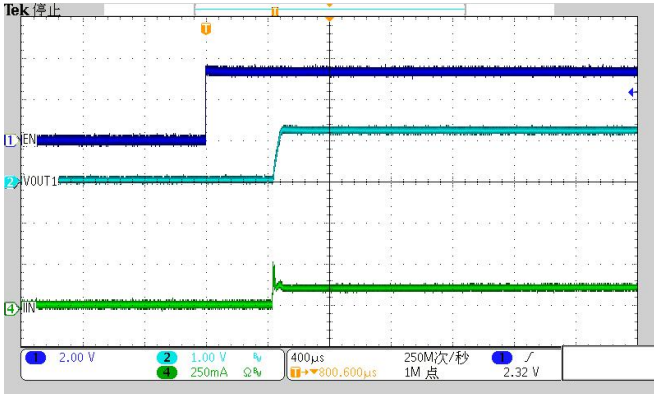
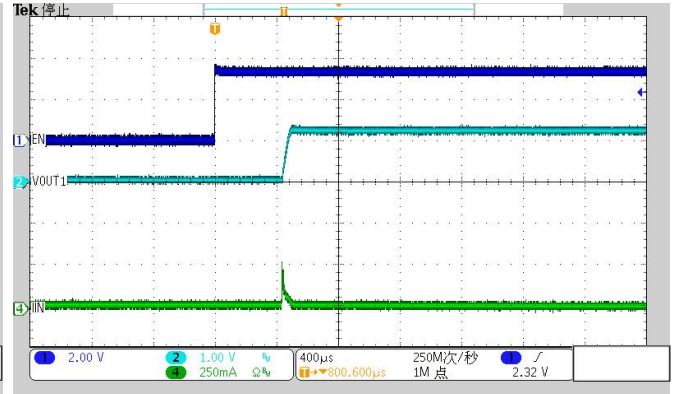
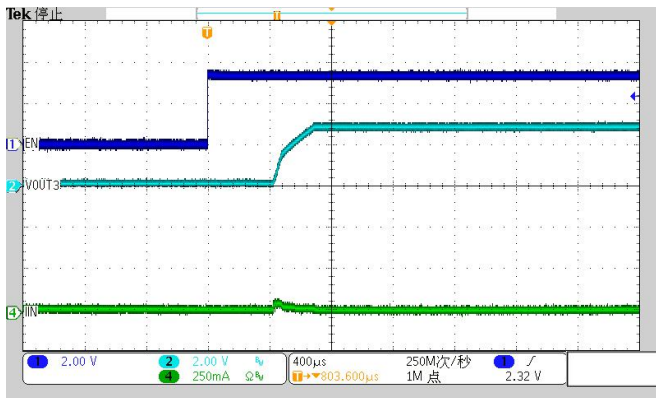
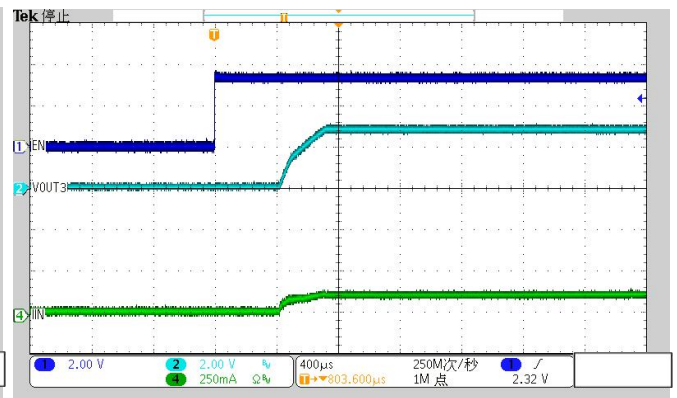
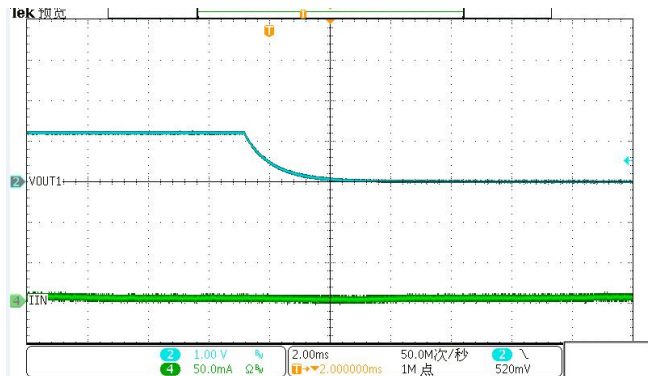
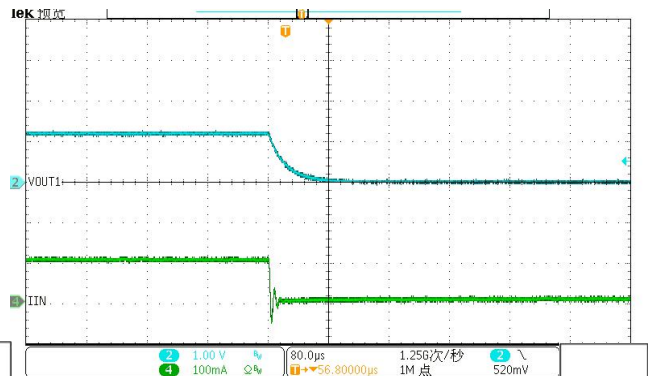
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>LDO1, LDO2 (DVDDx)</b>						
Input voltage range	V <sub>IN1</sub>		0.6		2.0	V
Output voltage range	DVDDx		0.6		1.8	V
Default output voltage	DVDDx	EN=H		1.2		V
Output voltage accuracy	V <sub>OUT_ACC</sub>		-2		+2	%
Output current limit	I <sub>LIM</sub>	R <sub>L</sub> =1Ω	700			mA
Short current	I <sub>SHORT</sub>	V <sub>OUT</sub> =GND		940		mA
Dropout voltage	V <sub>DROP</sub>	V <sub>IN2</sub> =3.3V, V <sub>OUT</sub> =1.05V, I <sub>OUT</sub> =500mA		72		mV
		V <sub>IN2</sub> =3.3V, V <sub>OUT</sub> =1.2V, I <sub>OUT</sub> =500mA		80		mV
	V <sub>DROP</sub>	V <sub>IN2</sub> =4.4V, V <sub>OUT</sub> =1.05V, I <sub>OUT</sub> =500mA		58		mV
		V <sub>IN2</sub> =4.4V, V <sub>OUT</sub> =1.2V, I <sub>OUT</sub> =500mA		60		mV
Load regulation	ΔV <sub>Load</sub>	V <sub>IN2</sub> =3.3V, V <sub>IN1</sub> =1.35V, V <sub>OUT</sub> =1.2V, I <sub>OUT</sub> =1~200mA		2		mV
Line regulation	ΔV <sub>LINE</sub>	V <sub>IN2</sub> =3.3V, V <sub>IN1</sub> =1.25~2.0V V <sub>OUT</sub> =1.2V, I <sub>OUT</sub> =10mA		0.1		mV
		V <sub>IN2</sub> =3.0~4.0V, V <sub>IN1</sub> =1.3V V <sub>OUT</sub> =1.2V, I <sub>OUT</sub> =10mA		0.1		mV
Output voltage noise	e <sub>NO</sub>	V <sub>IN2</sub> =3.3V, V <sub>IN1</sub> =1.3V V <sub>OUT</sub> =1.2V, 10Hz to 100KHz I <sub>OUT</sub> =0		150		uV
Power Supply Rejection Rate	PSRR <sub>VIN1</sub>	V <sub>IN1</sub> =1.35V+0.2V <sub>P-P</sub> V <sub>IN2</sub> =4.4V, V <sub>OUT</sub> =1.2V I <sub>OUT</sub> =10mA, F=1KHz, C <sub>OUT</sub> =1uF		72		dB
	PSRR <sub>VIN2</sub>	V <sub>IN2</sub> =4.4V+0.2V <sub>P-P</sub> V <sub>IN1</sub> =1.35V, V <sub>OUT</sub> =1.2V I <sub>OUT</sub> =10mA, F=1KHz, C <sub>OUT</sub> =1uF		45		dB

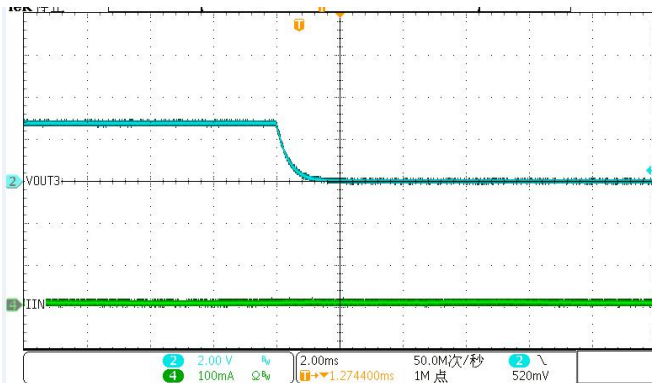
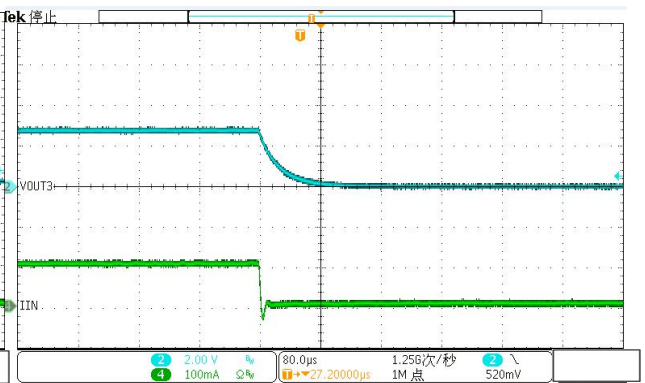
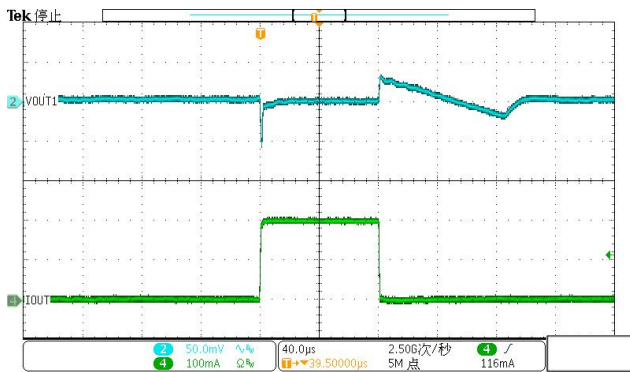
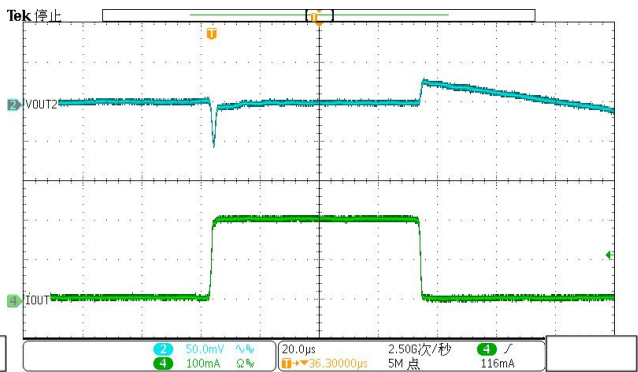
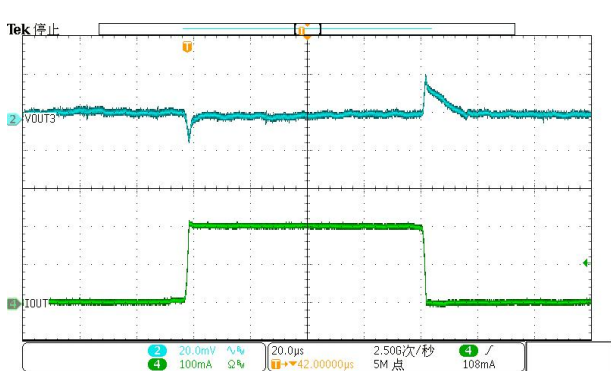
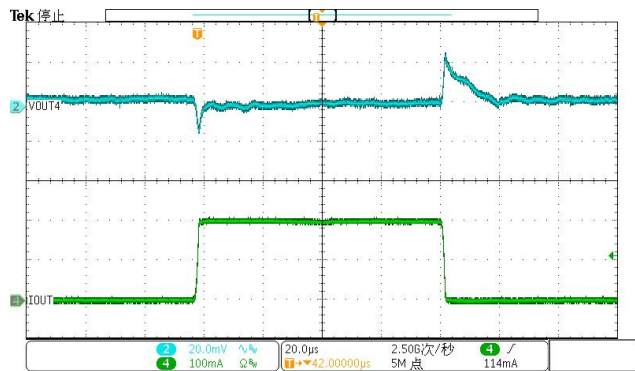
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>LDO3, LDO4 (AVDDx)</b>						
Input voltage range	V <sub>IN2</sub>		3		5.5	V
Output voltage range	AVDDx		1.2		4.3	V
Default output voltage	AVDDx	EN=H		2.8		V
Output voltage accuracy	V <sub>OUT_ACC</sub>		-2		+2	%
Output current limit	I <sub>LIM</sub>	R <sub>L</sub> =1Ω	300			mA
Short current	I <sub>SHORT</sub>	V <sub>OUT</sub> =GND		430		mA
Dropout voltage	V <sub>DROP</sub>	V <sub>OUT</sub> =2.8V, I <sub>OUT</sub> =300mA		90		mV
Load regulation	ΔV <sub>Load</sub>	V <sub>IN2</sub> =3.3V, V <sub>OUT</sub> =2.8V, V <sub>IN1</sub> =1.35V, I <sub>OUT</sub> =1~200mA		3		mV
Line regulation	ΔV <sub>LINE</sub>	V <sub>IN2</sub> =3.0V~4.0V, V <sub>OUT</sub> =2.8V, V <sub>IN1</sub> =1.35V, I <sub>OUT</sub> =10mA,		0.1		mV
Output voltage noise	e <sub>NO</sub>	V <sub>IN2</sub> =3.3V, V <sub>OUT</sub> =2.8V, V <sub>IN1</sub> =1.35V, 10Hz to 100KHz I <sub>OUT</sub> =0		8		uV
Power Supply Rejection Rate	PSRR	V <sub>IN2</sub> =4.4V+0.2V <sub>P-P</sub> , V <sub>IN1</sub> =1.35V, V <sub>OUT</sub> =2.8V, I <sub>OUT</sub> =10mA, F=1KHz, C <sub>OUT</sub> =1uF		92		dB
		V <sub>IN2</sub> =4.4V+0.2V <sub>P-P</sub> , V <sub>IN1</sub> =1.35V, V <sub>OUT</sub> =2.8V, I <sub>OUT</sub> =10mA, F=1KHz, C <sub>OUT</sub> =4.7uF		92		dB
		V <sub>IN2</sub> =4.4V+0.2V <sub>P-P</sub> , V <sub>IN1</sub> =1.35V, V <sub>OUT</sub> =2.8V, I <sub>OUT</sub> =10mA, F=1MHz, C <sub>OUT</sub> =1uF		35		dB
		V <sub>IN2</sub> =4.4V+0.2V <sub>P-P</sub> , V <sub>IN1</sub> =1.35V, V <sub>OUT</sub> =2.8V, I <sub>OUT</sub> =10mA, F=1MHz, C <sub>OUT</sub> =4.7uF		48		dB

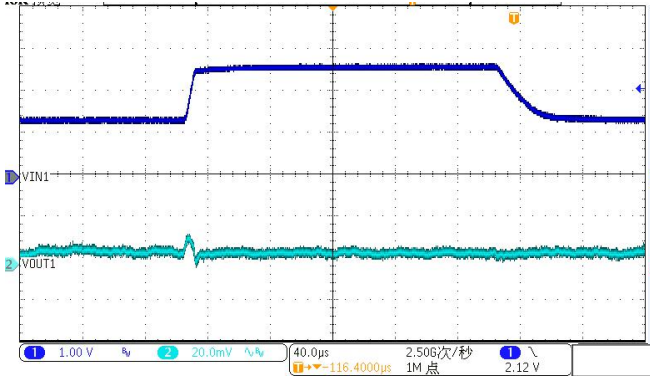
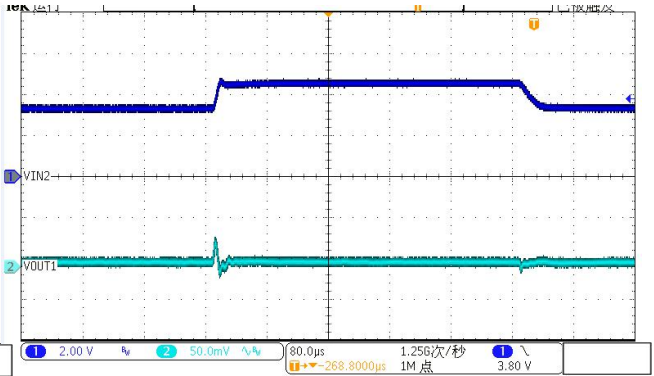
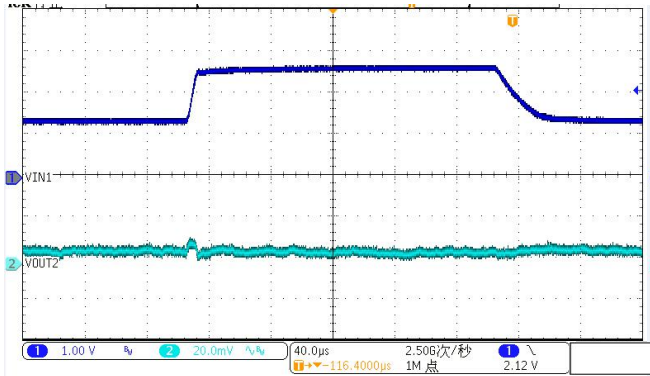
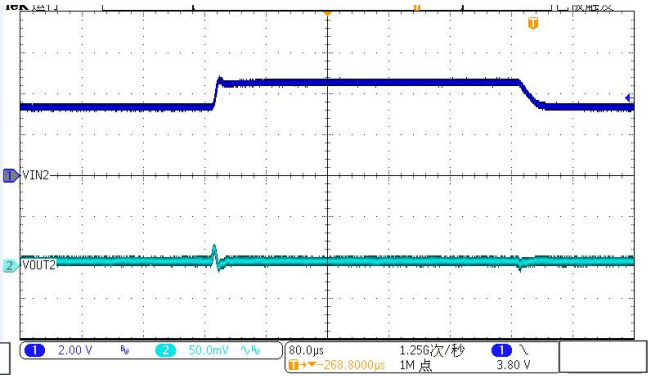
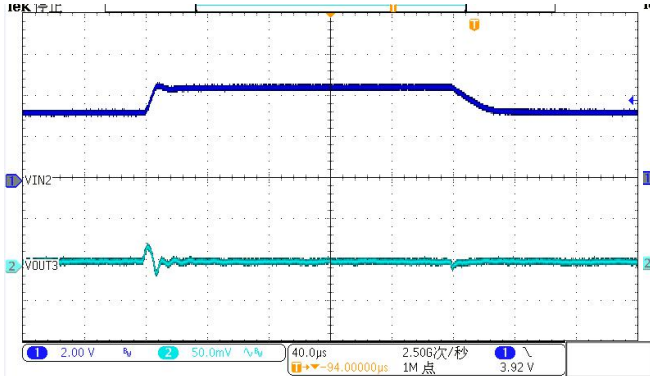
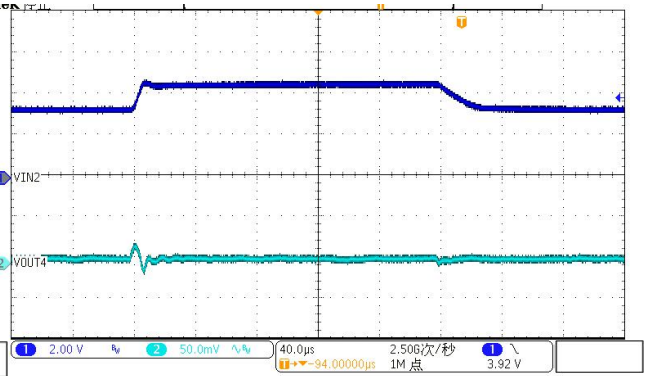
Typical Characteristics ( $T_A=25^{\circ}\text{C}$ ,  $C_{IN}=4.7\mu\text{F}$ ,  $C_{OUT}=1\mu\text{F}$ , unless otherwise noted)

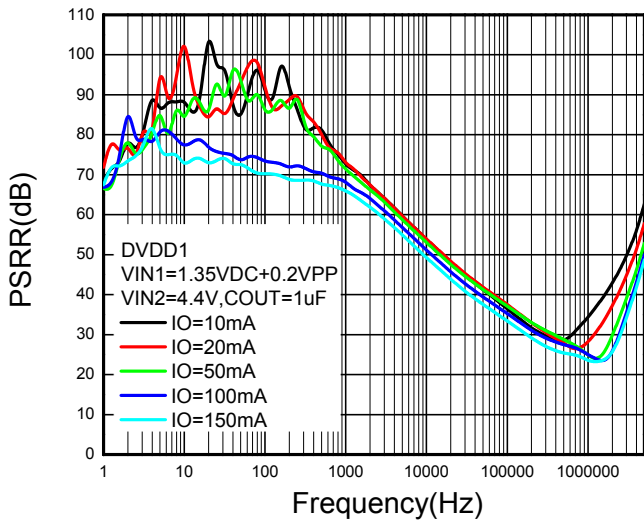
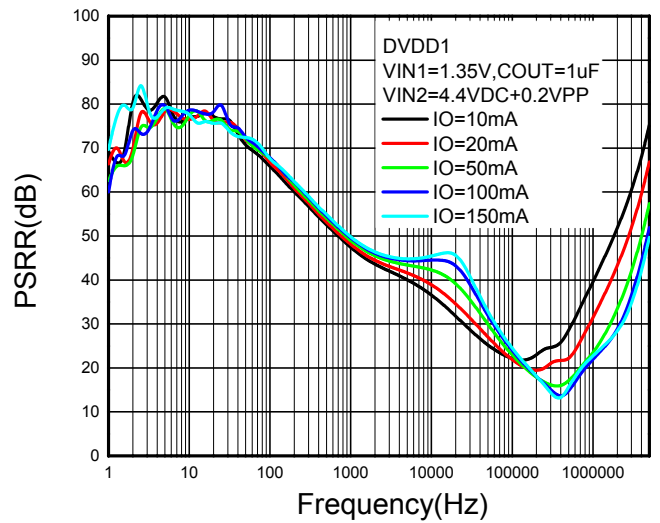
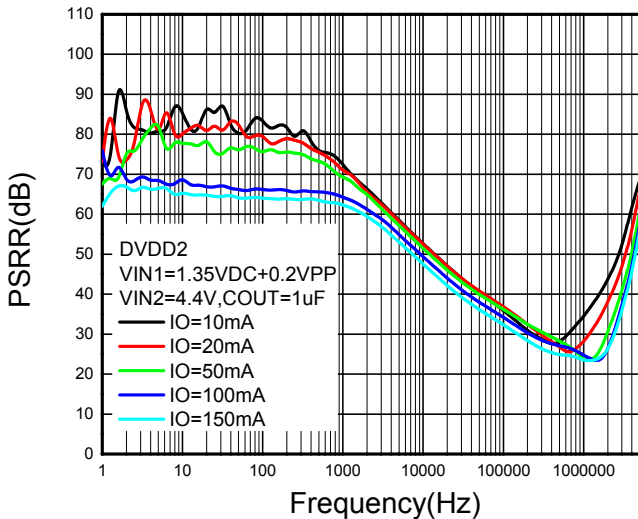
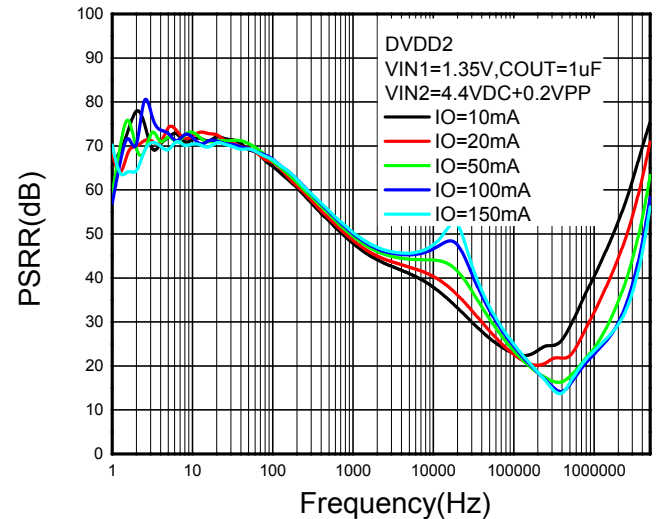
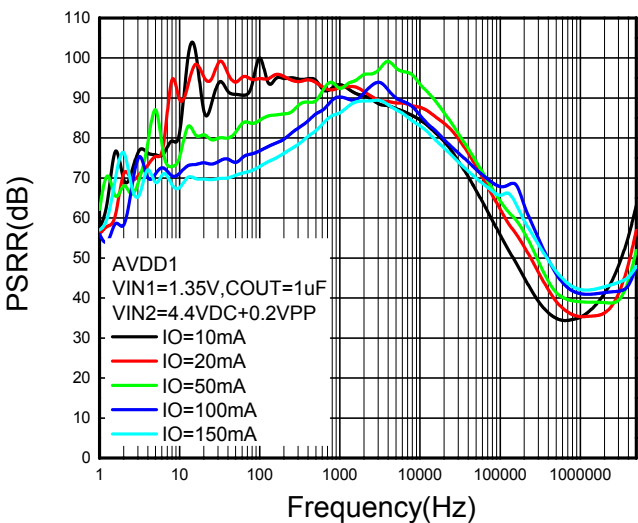
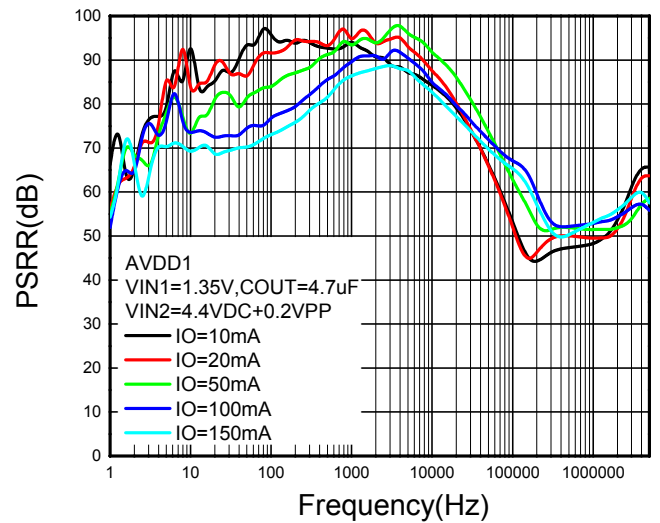


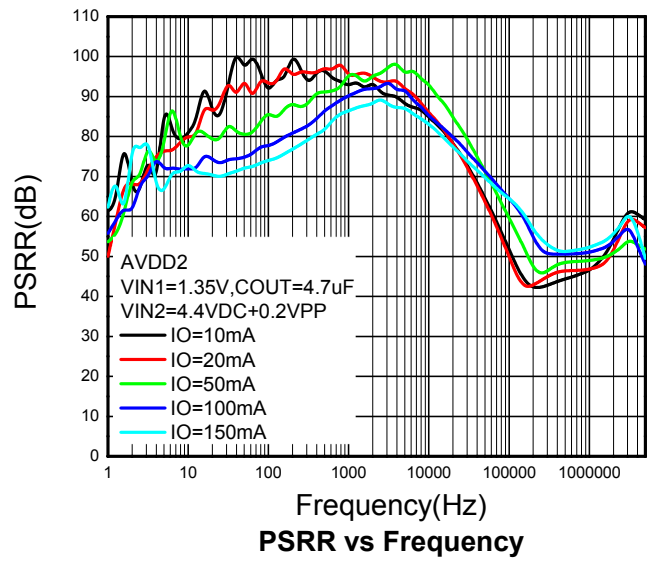
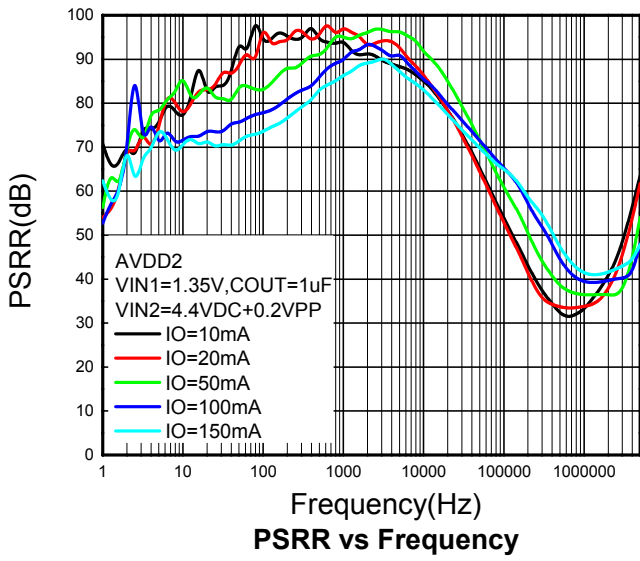


**Start Up**
**DVDD1/2**
 $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=0mA$ 

 $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=100mA$ 

**AVDD1/2**
 $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=0mA$ 

 $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=100mA$ 

**Shut Down**
**DVDD1/2**
 $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=0mA$ 

 $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=100mA$ 


**AVDD1/2**
 $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=0mA$ 

 $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=100mA$ 

**Load Transient**
**DVDD1,  $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=1\sim 200mA$** 

**DVDD2,  $V_{IN1}=1.35V, V_{IN2}=3.3V, I_{OUT}=1\sim 200mA$** 

**AVDD1,  $V_{IN2}=3.3V, I_{OUT}=1\sim 200mA$** 

**AVDD2,  $V_{IN2}=3.3V, I_{OUT}=1\sim 200mA$** 


**Line Transient**
**DVDD1,  $V_{IN1}=1.3\sim 2.6V$ ,  $V_{IN2}=3.3V$ ,  $I_{OUT}=1mA$** 

**DVDD1,  $V_{IN1}=1.35V$ ,  $V_{IN2}=3.3\sim 4.5V$ ,  $I_{OUT}=1mA$** 

**DVDD2,  $V_{IN1}=1.3\sim 2.6V$ ,  $V_{IN2}=3.3V$ ,  $I_{OUT}=1mA$** 

**DVDD2,  $V_{IN1}=1.35V$ ,  $V_{IN2}=3.3\sim 4.5V$ ,  $I_{OUT}=1mA$** 

**AVDD1,  $V_{IN2}=3.3\sim 4.5V$ ,  $I_{OUT}=1mA$** 

**AVDD2,  $V_{IN2}=3.3\sim 4.5V$ ,  $I_{OUT}=1mA$** 


**Power Supply Ripple Rejection (PSRR)**

**PSRR vs Frequency**

**PSRR vs Frequency**

**PSRR vs Frequency**

**PSRR vs Frequency**

**PSRR vs Frequency**

**PSRR vs Frequency**



## Function Description

WL2866D has 4 LDO regulators. Power up/down of each regulator can be controlled by the following three ways. It can be set at the registers DVDD<sub>x</sub>\_SEQ[3:0] & AVDD<sub>x</sub>\_SEQ[3:0] (x=1 to 4) respectively.

- A. External EN pin toggles from low to high, it will force DVDD<sub>x</sub> & AVDD<sub>x</sub> regulators powered up.
- B. Individual on/off control.
- C. Automatic power up/down sequence control.

### A. Chip enable control

External EN pin toggles from low to high, it will force DVDD<sub>x</sub> & AVDD<sub>x</sub> regulators powered up, output voltage of each LDO is default voltage, check EC Table.

When external EN pin is low, LDO output can be controlled by an I2C register.

### B. Individual on/off control.

Power-up and shut down of each regulator can be controlled by an I2C register. DVDD<sub>x</sub>\_EN & AVDD<sub>x</sub>\_EN are internal signals to enable one of regulators, If DVDD<sub>x</sub>\_SEQ[3:0] & AVDD<sub>x</sub>\_SEQ[3:0] set to '0000', that DVDD<sub>x</sub> & AVDD<sub>x</sub> channels can be controlled directly by a bit specified in register DVDD<sub>x</sub>\_EN & AVDD<sub>x</sub>\_EN. DVDD<sub>x</sub>\_VOUT[7:0] & AVDD<sub>x</sub>\_VOUT[7:0] can set output voltage of each channel.

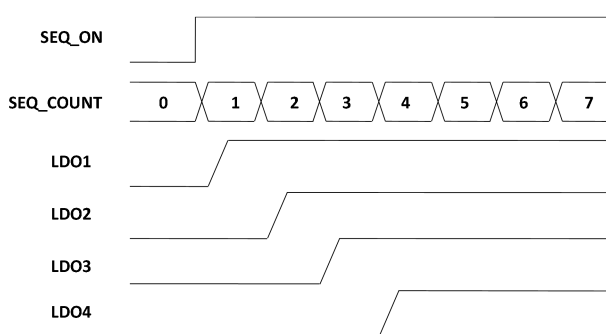
### C. Automatic power up/down sequence control.

WL2866D has seven SLOTS to which each regulator can be assigned.

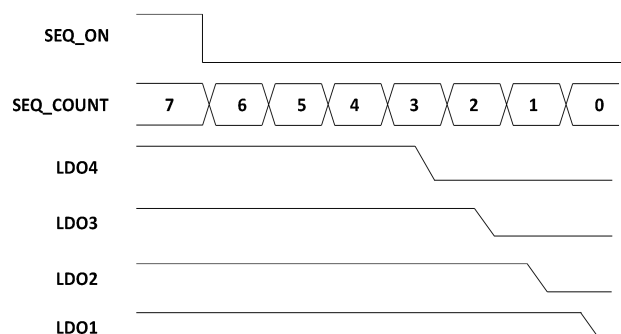
SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7
-------	-------	-------	-------	-------	-------	-------

They are started by SEQ\_ON signal. when SEQ\_ON is high. Internal counter SEQ\_COUNT[2:0] starts increments from 0 ( "000" ) to 7 ( "111" ). When SEQ\_ON is low, SEQ\_COUNT[2:0] decrements from 7 ( "111" ) to 0 ( "000" ). Regulators assigned to one of SLOTS starts power-up or power-down when SEQ\_COUNT[2:0] matches the SLOT number.

Internal logic signal SEQ\_ON is asserted by I2C, write '00' to SEQ\_CTRL[1:0] will set SEQ\_ON to '0', while write '01' to SEQ\_CTRL[1:0] will set SEQ\_ON to '1'.



Example of Power-up in the case of L DVDD<sub>x</sub> & AVDD<sub>x</sub> are assigned to SLOT1 - SLOT4 respectively



Example of Shutdown in the case of DVDD<sub>x</sub> & AVDD<sub>x</sub> are assigned to SLOT1 - SLOT4 respectively.

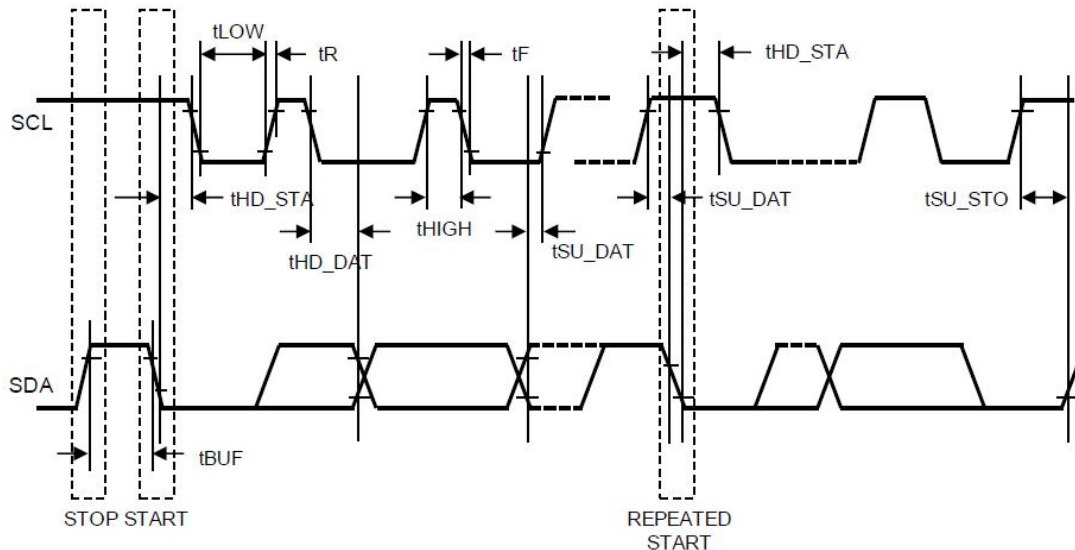
## Output discharge setting

Set related bits to select output discharge function for Discharge Resistor(0x02H Register), "0": Disable. "1". Enable

## I2C Interface

WL2866 utilizes I2C interface to write / read internal registers. It supports 100Kbps standard mode 400Kbps fast mode. The I2C address is 0x50H.

### I2C Serial Data Bus



**Figure 2. I<sup>2</sup>C Mode Timing Diagram**

The WL2866 supports the I2C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The WL2866 operates as a slave on the I2C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The WL2866 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The following bus protocol has been defined (Figure 2 and Figure 3). Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

#### **Bus Not Busy**

Both data and clock lines remain HIGH.

#### **Start Data Transfer**

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

#### **Stop Data Transfer**

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

#### **Data Valid**

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period

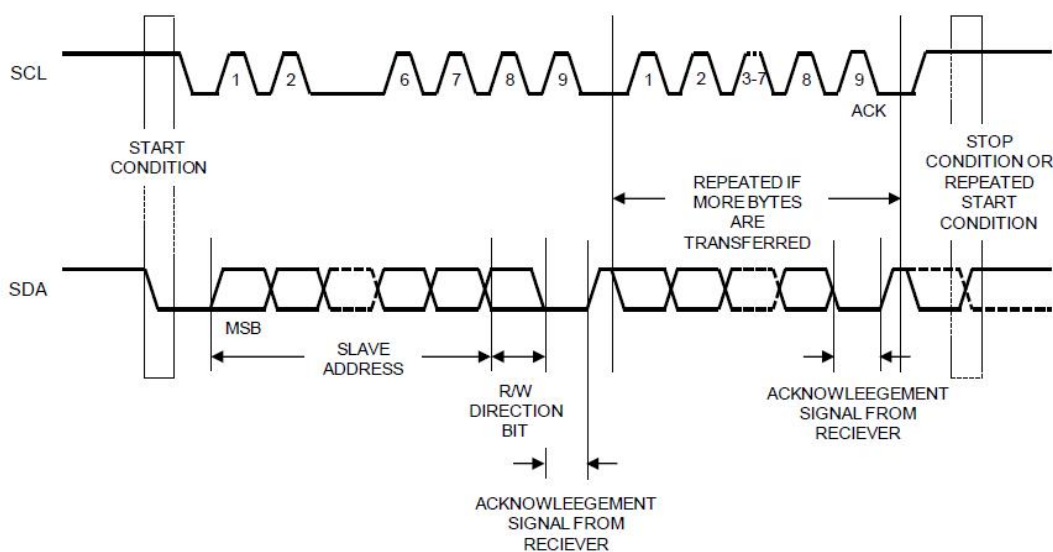
of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

### **Acknowledge**

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.



**Figure 3. Data Transfer on I<sup>2</sup>C Serial Bus**

Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
  
2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The WL2866 can operate in the following two modes:

**1. Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 4 for Interface). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 4-bit WL2866 address followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the WL2866 acknowledges the slave address + write bit, the master transmits a register address to the WL2866. This sets the register pointer on the WL2866. The master may then transmit zero or more bytes of data, with the WL2866 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

**2. Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the WL2866 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 4-bit WL2866 address followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The WL2866 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The WL2866 must receive a “not acknowledge” to end a read.

The 7-bit slave device address is 01010000 binary (or 50H).

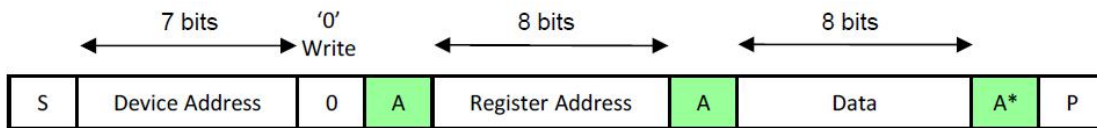


Figure 4. I<sup>2</sup>C Write – Slave Receiver Mode

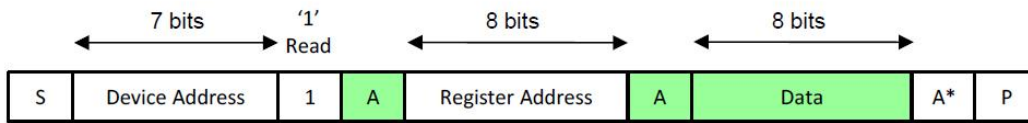
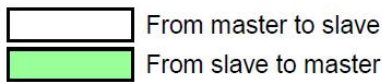


Figure 5. I<sup>2</sup>C Read – Slave Transmitter Mode

Where

- S = START condition
- P = STOP condition
- Device Address = 01010000 (7 bits, MSB first)
- Register Address = Reg0 – Reg15 address (8 bits)
- Data = data to read or write (8 bits)
- 1 = Read command bit
- 0 = Write command bit
- A = acknowledge (SDA low)
- A\* = not acknowledge (SDA high)

**Register Description**

0x00	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Chip_REV[7:0]							
Mode	R							
Init	0000 0000							
0x01	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.							
Mode	RW							
Init	0000 0000							
0x02	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Discharge Resistor Enable/Disable							
Mode	RW	RW	RW	RW	RW			
Init	0	0	0	0	0000			
0x03	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DVDD1_VOUT[7:0]							
Mode	RW							
Init	0110 0100							
0x04	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DVDD2_VOUT[7:0]							
Mode	RW							
Init	0110 0100							
0x05	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AVDD1_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x06	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AVDD2_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x07	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.							
Mode	RW							
Init	0000 0000							
0x08	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.							
Mode	RW							
Init	0000 0000							
0x09	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.							
Mode	RW							
Init	0000 0000							

0x0A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DVDD2_SEQ[3:0]				DVDD1_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AVDD2_SEQ[3:0]				AVDD1_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.				N.A.			
Mode	RW				RW			
Init	0000				0000			
0x0D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.				N.A.			
Mode	RW				RW			
Init	0000				0000			
0x0E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.				AVDD2_EN	AVDD1_EN	DVDD2_EN	DVDD1_EN
Mode	RW				RW	RW	RW	RW
Init	0000				0	0	0	0
0x0F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SEQ_SPEED[1:0]		SEQ_CTRL[1:0]		SEQ_ON	SEQ_COUNT[2:0]		
Mode	RW		RW		R	R		
Init	00		00		0	000		

**Register Description**

0x00	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Chip_REV[7:0]							
Mode	R							
Init	0000 0000							

**Chip\_REV[7:0]**

Indicates the device ID with revision. Read only.

0x02	Bit7*	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Discharge Resistor Enable/Disable							
Mode	RW	RW	RW	RW	RW			
Init	0	0	0	0	0000			

**Discharge Resistor Selection**

Each LDO regulators output discharge resistor enable control.

Bit0 for DVDD1, Bit1 for DVDD2 ,

Bit2 for AVDD1, Bit3 for AVDD2 .

0= Disable , 1= Enable

\*Note : When use the Discharge Function , should set Bit7 =1 .

0x03	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DVDD1_VOUT[7:0]							
Mode	RW							
Init	0110 0100							
0x04	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DVDD2_VOUT[7:0]							
Mode	RW							
Init	0110 0100							

**DVDD1\_VOUT[7:0] & DVDD2\_VOUT[7:0]**

Define the Output Voltage Level of DVDD1 & DVDD2

$$VOUT_x = 0.6V + DVDD_x\_VOUT[7:0] * 0.006V$$

The following table shows the code of each voltage setting for reference

Dec.	Binary	Hex.	Voltage (V)	Dec.	Binary	Hex.	Voltage (V)
0	0000 0000	00H	0.6000	85	0101 0101	55H	1.11
	*****			86	0101 0110	56H	1.116
60	0011 1100	3CH	0.96	87	0101 0111	57H	1.122
61	0011 1101	3DH	0.966	88	0101 1000	58H	1.128
62	0011 1110	3EH	0.972	89	0101 1001	59H	1.134
63	0011 1111	3FH	0.978	90	0101 1010	5AH	1.14
64	0100 0000	40H	0.984	91	0101 1011	5BH	1.146
65	0100 0001	41H	0.99	92	0101 1100	5CH	1.152
66	0100 0010	42H	0.996	93	0101 1101	5DH	1.158
67	0100 0011	43H	1.002	94	0101 1110	5EH	1.164
68	0100 0100	44H	1.008	95	0101 1111	5FH	1.17
69	0100 0101	45H	1.014	96	0110 0000	60H	1.176
70	0100 0110	46H	1.02	97	0110 0001	61H	1.182
71	0100 0111	47H	1.026	98	0110 0010	62H	1.188
72	0100 1000	48H	1.032	99	0110 0011	63H	1.194
73	0100 1001	49H	1.038	100	<b>0110 0100</b>	<b>64H</b>	<b>1.20</b>
74	0100 1010	4AH	1.044	101	0110 0101	65H	1.206
75	0100 1011	4BH	1.05	102	0110 0110	66H	1.212
76	0100 1100	4CH	1.056	103	0110 0111	67H	1.218
77	0100 1101	4DH	1.062	104	0110 1000	68H	1.224
78	0100 1110	4EH	1.068	105	0110 1001	69H	1.23
79	0100 1111	4FH	1.074	106	0110 1010	6AH	1.236
80	0101 0000	50H	1.08	107	0110 1011	6BH	1.242
81	0101 0001	51H	1.086	108	0110 1100	6CH	1.248
82	0101 0010	52H	1.092	109	0110 1101	6DH	1.254
83	0101 0011	53H	1.098	110	0110 1110	6EH	1.26
84	0101 0100	54H	1.104	~255	*****		

0x05	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AVDD1_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x06	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AVDD2_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x07	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.							
Mode	RW							
Init	0000 0000							
0x08	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.							
Mode	RW							
Init	0000 0000							
0x09	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.							
Mode	RW							
Init	0000 0000							

**AVDD1\_VOUT[7:0] & AVDD2\_VOUT[7:0]**

Define the Output Voltage Level of AVDD1& AVDD2

$$VOUT_x = 1.2V + AVDD_x\_VOUT[7:0] * 0.0125V.$$

The following table shows the code of each voltage setting for reference

Dec.	Binary	Hex.	Voltage (V)	Dec.	Binary	Hex.	Voltage (V)
0	0000 0000	00H	1.2000	128	1000 0000	80H	2.8000
1	0000 0001	01H	1.2125	129	1000 0001	81H	2.8125
2	0000 0010	02H	1.2250	130	1000 0010	82H	2.8250
3	0000 0011	03H	1.2375	131	1000 0011	83H	2.8375
4	0000 0100	04H	1.2500	132	1000 0100	84H	2.8500
5	0000 0101	05H	1.2625	133	1000 0101	85H	2.8625
6	0000 0110	06H	1.2750	134	1000 0110	86H	2.8750
7	0000 0111	07H	1.2875	135	1000 0111	87H	2.8875
8	0000 1000	08H	1.3000	136	1000 1000	88H	2.9000
9	0000 1001	09H	1.3125	137	1000 1001	89H	2.9125
10	0000 1010	0AH	1.3250	138	1000 1010	8AH	2.9250
11	0000 1011	0BH	1.3375	139	1000 1011	8BH	2.9375
12~127	*****			~255	*****		

0x0A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DVDD2_SEQ[3:0]				DVDD1_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	AVDD2_SEQ[3:0]				AVDD1_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.				N.A.			
Mode	RW				RW			
Init	0000				0000			
0x0D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.				N.A.			
Mode	RW				RW			
Init	0000				0000			

#### DVDD<sub>x</sub>\_SEQ[3:0] & AVDD<sub>x</sub>\_SEQ[3:0]

Power sequence setting register. there are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shut down start from slot7 to slot1. Power-up and shut down of each LDO regulator can be set at any one of the slots.

Register Value	VOUT <sub>x</sub>
0000	Controlled by I2C register LDO <sub>x</sub> _EN[6:0]
x001	slot1
x010	slot2
x011	slot3
x100	slot4
x101	slot5
x110	slot6
x111	slot7

In the case of that register value of DVDD<sub>x</sub>\_SEQ[3:0] & AVDD<sub>x</sub>\_SEQ[3:0] ,are set to be default “0000”, that DVDD<sub>x</sub> and AVDD<sub>x</sub> regulators will be controlled by register DVDD<sub>x</sub>\_EN & AVDD<sub>x</sub>\_EN, which will be controlled by register SEQ\_CTRL[1:0], in this stage, the power-up and shutdown sequence of each LDO regulators will be followed by register DVDD<sub>x</sub>\_SEQ[3:0] & AVDD<sub>x</sub>\_SEQ[3:0] setting witch shown as above table.

0x0E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	N.A.				AVDD2_EN	AVDD1_EN	DVDD2_EN	DVDD1_EN
Mode	RW				RW	RW	RW	RW
Init	0000				0	0	0	0

### DVDD<sub>x</sub>\_EN & AVDD<sub>x</sub>\_EN

Chip enable control register by I2C while the register value of DVDD<sub>x</sub>\_SEQ[3:0] & AVDD<sub>x</sub>\_SEQ[3:0] are set to be default "0000". This register can be written to enable or disable the corresponding LDO regulator.

Bit0 for DVDD1\_EN, Bit1 for DVDD2\_EN, Bit2 for AVDD1\_EN, Bit3 for AVDD2\_EN .

0x0F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SEQ_SPEED[1:0]		SEQ_CTRL[1:0]		SEQ_ON	SEQ_COUNT[2:0]		
Mode	RW		RW		R	R		
Init	00		00		0	000		

**SEQ\_SPEED[1:0]** define the slot period as following:

Register Value	slot period (ms)
00	2.00
01	1.00
10	0.50
11	0.25

**SEQ\_CTRL[1:0]** enables power-up or shut down of SEQ

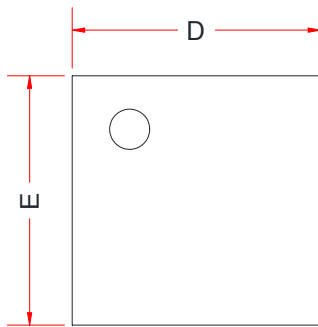
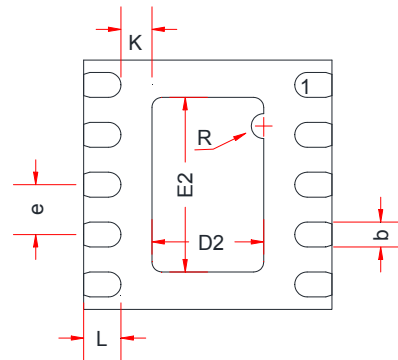
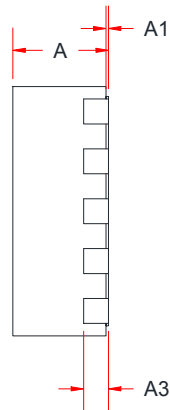
Register Value	SEQ Status
x0	Shutdown
x1	Power-up

**SEQ\_ON[1:0]** indicates the activation signal of SEQ, read only.

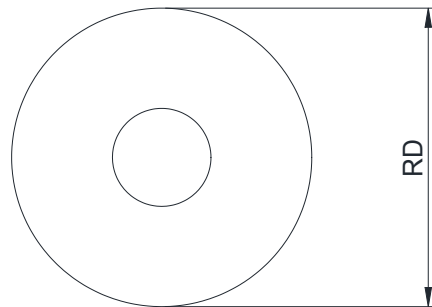
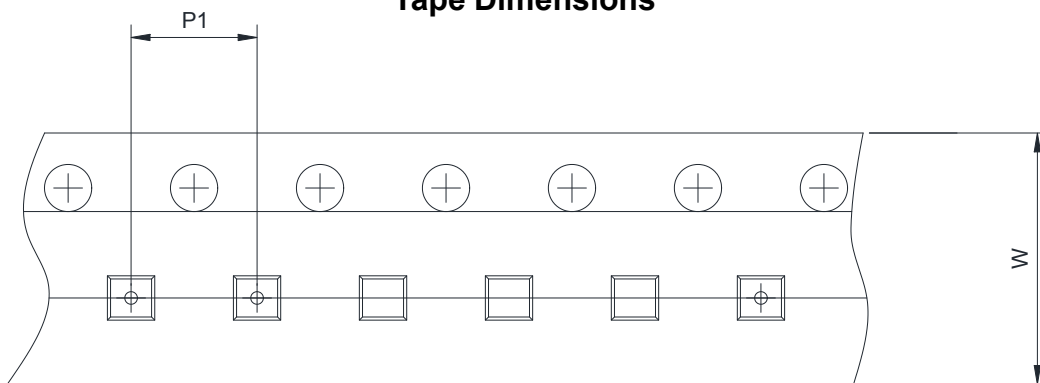
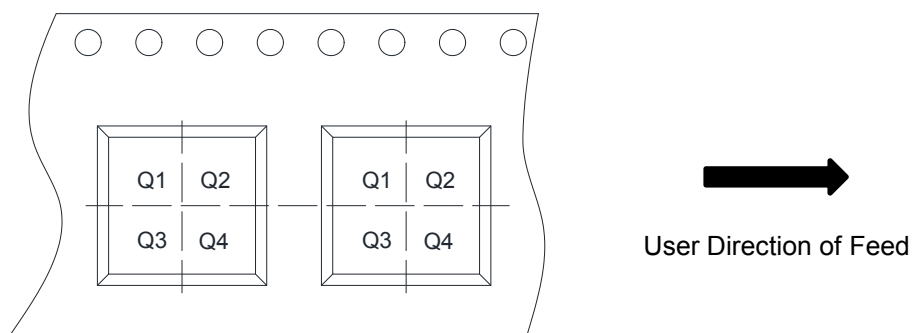
Register Value	SEQ Status
0	Shutdown
1	Power-up

**SEQ\_COUNT[1:0]** indicates the slot number of SEQ at the moment. Read only.

Register Value	SEQ Counter
000	No LDO starts.
001	slot1 starts
010	slot2 starts
011	slot3 starts
100	slot4 starts
101	slot5 starts
110	slot6 starts
111	slot7 starts and stop counting.

**PACKAGE OUTLINE DIMENSIONS**
**DFN2x2-10L**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 Ref.		
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.80	0.90	1.00
E2	1.30	1.40	1.50
e	0.30	0.40	0.50
K	0.15	0.25	0.35
L	0.25	0.30	0.35
R	0.10 Ref.		

**TAPE AND REEL INFORMATION**
**Reel Dimensions**

**Tape Dimensions**

**Quadrant Assignments For PIN1 Orientation In Tape**


RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch	<input type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm	<input type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input checked="" type="checkbox"/> 4mm <input type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4