PM8385

QuadPHY® RT

4-Port GE/FC Retimer

Data Sheet

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Revision History

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1	December 2003	Initial Release

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Preface

This Product Overview describes the features and applications of PMC-Sierra's PM8385 QuadPHY® RT. The Product Overview is essential reading for system architects who are evaluating the QuadPHY RT and for designers who will use the QuadPHY RT.

In order to understand the information in this document, the reader should have a strong working understanding of digital design, serializer/deserializers (SERDES), high-speed serial design, Gigabit Ethernet and Fibre Channel.

1 Features

- The PM8385 QuadPHY RT is a 4-channel uni-directional or dual bi-directional repeater /retimer for backplane and line card links operating from 1.0625Gbit/s to 2.125Gbit/s
- Supports repeater or retimer applications for IEEE 802.3 Gigabit Ethernet links at 1.25 Gbit/s and Fibre Channel Physical Interface (FC-PI) links at 1.0625 or 2.125 Gbit/s.
- Provides non-blocking cross-bar for protection switching, broadcasting and multi-cast
- High-speed Inputs and Outputs have independent, selectable terminations on a per-channel basis that provide ability to connect between mediums with different impedances (i.e. 50-ohm PCB trace to 75-ohm cable).
- Each port supports FC 1G or 2G-rate detection/auto-selection.
- Contains a per-link, 16 word receive FIFO for clock rate difference compensation up to ± 100 ppm from the nominal rate, by inserting and deleting idle characters or ordered sets.
- Supports single-ended or differential 125 MHz reference clock REFCLK for Gigabit Ethernet or 106.25MHz reference clock for Fibre Channel applications.

High Speed Interface Features

- Requires no external components to interface the high-speed signals to optics, twinax (1000BASE-CX), or serial back planes with use of the internal coupling capacitors. This results in minimum board footprint and greatly improved signal integrity.
- High-speed outputs with selectable output amplitude and programmable pre-emphasis per port to counteract dielectric losses and allow maximum reach on printed circuit boards.
- Selectable receive input equalization on per-channel basis for improved signal integrity
- Selectable receive input termination or source output impedance (100/150 Ω differential) on per-channel basis.

Test and Control Features

- Standalone repeater or retimer operation via pin-strap configuration
- Supports optional 2-pin serial management interface using selectable Two-Wire Interface (TWI) or MDC/MDIO protocol for configuration and diagnostic access.
- Digital Loss of Link (DLOLB) detected outputs can be programmed to indicate multiple error parameters or conditions for monitoring individual or multiple links. An Interrupt output is provided to flag changes in DLOLB error conditions.
- Supports internal serial loop back modes for each port for testing and debugging.
- Standard 5 signal IEEE 1149.1 JTAG test port for digital pin (only) boundary scan.

Packaging

- 0.18 µ CMOS, 1.8 V and 3.3 V Supply.

- Extended temperature range of –40 °C to +85 °C for challenging system environments.
- Small 15 mm x 15 mm footprint, 196-pin Chip Array BGA with 1.0 mm ball pitch.
- Ultra-low operating power of 1.3 W typical with all 4 channels active at 2.125 G.

2 References

1. Fibre Channel – Framing and Signaling, FC-FS, Rev 1.70, February 8, 2002.

2. Fibre Channel – Physical Interfaces, FC-PI, Rev 13, Dec 09, 2001.

3. Fibre Channel – Physical Interfaces, FC-PI-2, Rev 3.0, Sept 13, 2002.

4. Fibre Channel – Arbitrated Loop, FC-AL-2 , Version 1.0, Dec 08, 1999.

5. Fibre Channel-Methodology for Jitter and Signal quality specification, FC-MJSQ, Version 7.0, Oct 06,2002

6. *IEEE* 1149.1-1990 Standard Test Access Port and Boundary-Scan Architecture.

7. *IEEE* 802.3ae Clause 45 Management Interface Specification (MDC/MDIO).

8. *IEEE* 802.3z Clause 36 (1000Base-X PCS/PMA)

9. PMC-2010750, Signal Integrity for PMC-Sierra 3.125/2.488/1.25 Gbit/s Links Application Note.

10. Electronic Industries Association. *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)*: EIA/JESD51. December 1995.

11. Electronic Industries Alliance 1999. *Integrated Circuit Thermal Test Method Environmental Conditions –Junction-to-Board: JESD51-8*. October 1999.

12. Telcordia Technologies. *Network Equipment-Building System (NEBS) Requirements: Physical Protection: Telcordia Technologies Generic Requirements GR-63-CORE*. Issue 1. October 1995.

13. SEMI (Semiconductor Equipment and Materials International). *SEMI G30-88 Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages*. 1988.

3 Applications

The QuadPHY RT device addresses repeater, retiming and signal conditioning for gigabit serial link extension and ensuring standards compliance and robust system operation in a variety of challenging line card and backplane system environments. Specifically, the QuadPHY RT meets and exceeds IEEE 802.3 Gigabit Ethernet and ANSI T11.2 for 1 Gigabit and 2 Gigabit Fibre channel standards. Typically the QuadPHY RT is used as a backplane driver for link extension or as a companion for higher-layer devices such as ASICs, FPGAs and switch standard products that incorporate serial I/O.

In addition to providing extensive signal integrity features to improve high-speed serial performance, the QuadPHY RT has the ability to perform error monitoring on each link. The device can be used in the following applications:

- High-speed backplane driver operating from 1.0625Gbit/s to 2.125Gbit/s
- Distributed switch fabrics or protection switches via data bi-cast, multi-cast or broadcast to fabric elements
- Allows fully redundant systems, protection switching and simplifies distributed switch fabric applications via a non-blocking cross-bar for broadcasting and multi-casting
- Enterprise Ethernet or Fibre Channel Switches.
- Fibre Channel Retimer
- Gigabit Ethernet Retimer including 1000BASE-CX
- Industrial Control and Processing Systems
- Inter-medium Connections

Retimers Provide Optimal Solution for the Hostile Backplane Environment

The backplane is a hostile environment for multi-gigabit signals that presents many design challenges to system designers. At the same time, backplane design is a critical component in determining system reliability and robust operation. Backplane design issues include a host of challenges that must be considered including system link distance, link speed, bit error rate (BER) and jitter, line card hot plug capability, connectors, vias, and ESD protection. Subtle issues such as latch-up, common mode balance, cross talk, and return loss can impact reliability and system data integrity over a wide variety of operating temperatures and environments.

The QuadPHY RT provides a small footprint, and low power solution to mitigate these issues, ensure standards compliance and minimize back end system qualification. More importantly, the inclusion of retimer backplane drivers can reduce the chances of in-field system failures due to system signal integrity issues that can lead to expensive and lengthy system debug, re-design and qualification.

The QuadPHY RT can operate as a 4 port uni-directional retimer, or a 2 port bi-directional retimer depending on system requirements. Figure 1shows the QuadPHY RT can as a bi-directional 2 port Gigabit Ethernet retimer. Other Gigabit Ethernet applications include stacking port applications (ie 1000BASE-CX) where the QuadPHY RT drives cables between boxes. Figure 2 shows how the QuadPHY RT is used in Fibre Channel applications to convert the 150 Ω differential impedance from the next rack's cable to match the 100 Ω differential impedance connections to the Host Bus Adapter (HBA) and PBC 18x2G.

Figure 1 QuadPHY RT as Dual Bi-directional Gigabit Ethernet Retimer

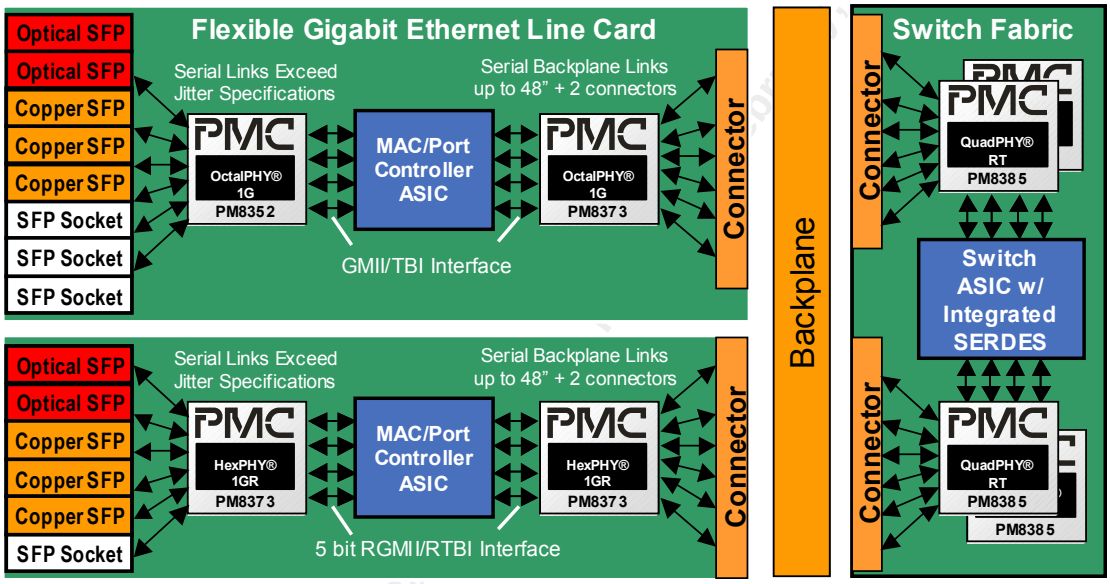
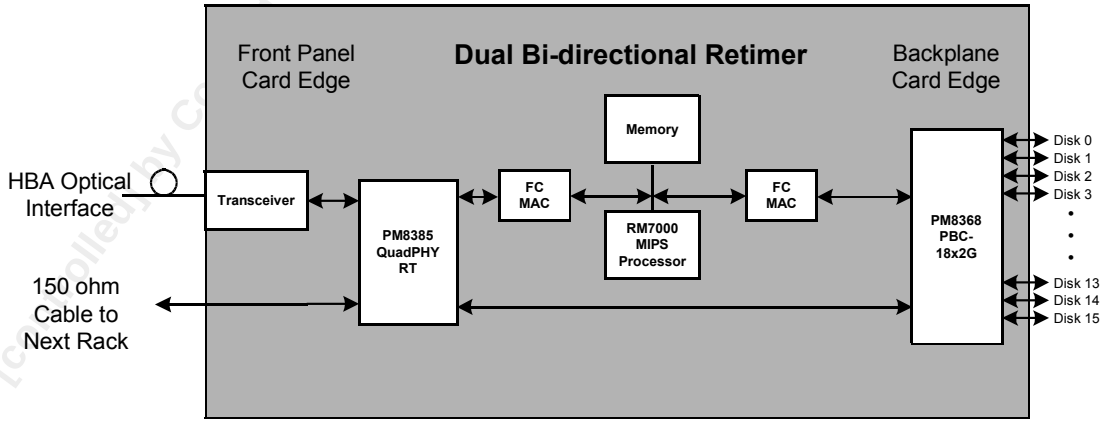


Figure 2 QuadPHY RT as Dual Bi-directional Fiber Channel Retimer



Redundant System Architectures Supported By the QuadPHY RT

The QuadPHY RT supports redundant system architectures by allowing a single input to be broadcast to multiple outputs. The ingress data stream is broadcast to both the working and protection ports while the egress uses the management interface to select whether to source data from the working or protection port. Figure 3 shows a redundant line card application that incorporates working and protection switch fabrics. Figure 4 shows a distributed switch fabric architecture where the QuadPHY RT is used to simplify the interconnect via data broadcast or multicast cross-connect capability.

Figure 3 Redundant Gigabit Ethernet or Fibre Channel Architectures

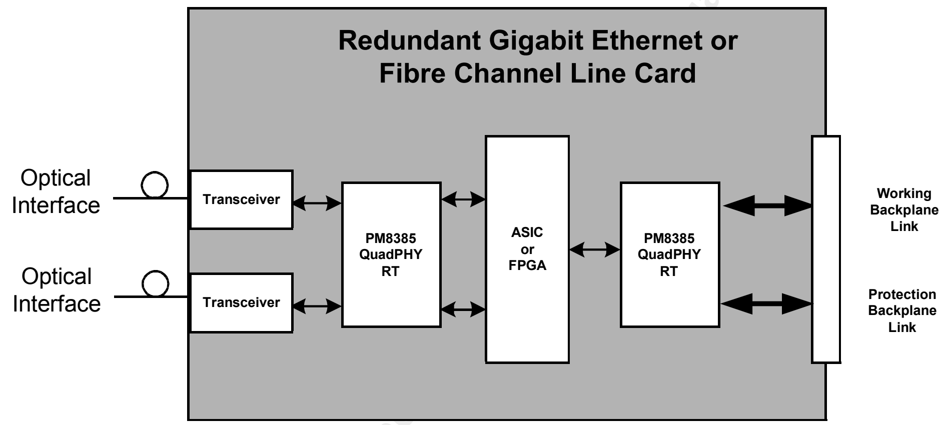
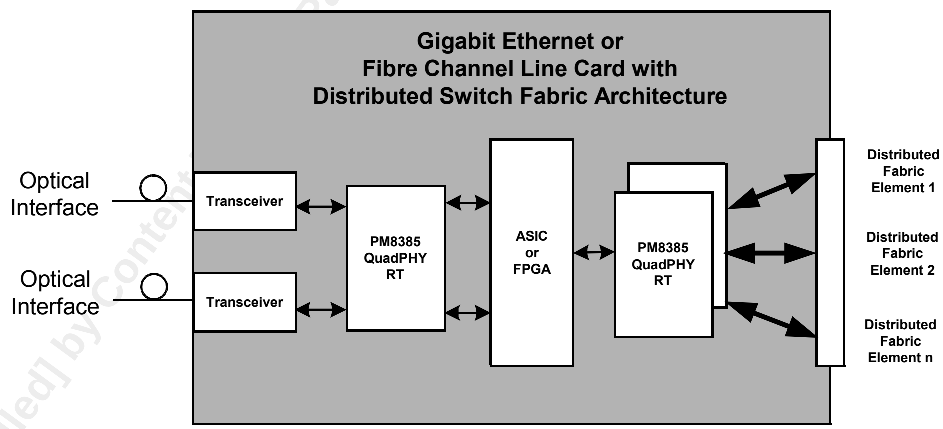


Figure 4 Broadcast or Multicast for Distributed Switch Fabric Architectures



4 Operational Description

The QuadPHY RT is a low power, four-channel uni-directional retimer or 2 channel bi-directional repeater or retimer suitable for applications such as high-speed serial backplanes for Gigabit Ethernet and Fibre Channel. The QuadPHY RT significantly improves system jitter to ensure system standards compliance or to extend link distances. Extensive signal integrity features, low latency, a small footprint and low power enable best practice backplane and system design for robust and standards compliant operation in a wide variety of system environments. The internal non-blocking cross-bar provides flexibility for loopbacks or data replication for the bi-cast, multi-cast or broadcast of data to working and protection fabrics, or distributed fabric elements.

The QuadPHY RT provides bi-directional clock and data recovery on all ports at 1.25Gbit/s for Gigabit Etherent per IEEE 802.3-2002 or 1.0625Gbit/s or 2.125Gbit/s Fibre Channel Physical Interface (FC-PI) data streams. The PM8385 supports rate detection and auto-selection for 1G and 2G Fibre Channel applications. As a repeater, the QuadPHY RT uses the recovered clock as the timing reference for the egress link. As a retimer, the QuadPHY RT uses the local clock for retiming as well as an elastic FIFO for rate adaptation.

The PM8385 includes extensive features to support a wide variety of applications that require high quality and standards compliant signal integrity. The PM8385 integrates coupling capacitors and terminating resistors to minimize board footprint and improve singal integrity. Receive input and source output termination are selectable for 100Ω or 150Ω differential.

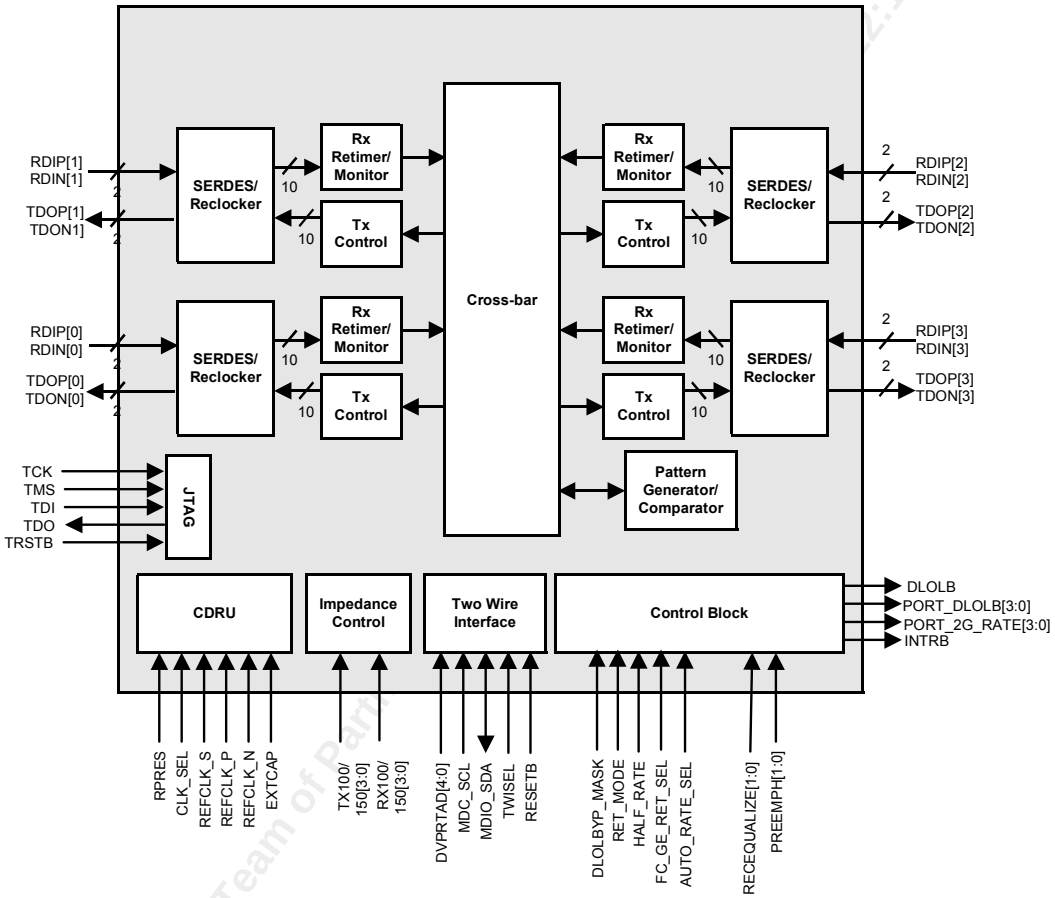
In the receive direction the PM8385 receives serial differential data, recovers the data and performs either a repeating or retiming function. The high-speed differential receiver on each link has internal capacitor coupling and parallel termination to eliminate the need for external passive devices and their impact on signal integrity. Programmable receive equalization provides robust data recovery of highly degraded input signals. After recovery, the data can be repeated using a recovered clock (repeater) or retimed to the local reference clock (retimer). An elastic FIFO provides rate adaptation and can accommodate clock differences of 200ppm. Optionally, the receive data may be multi-cast or broadcast to any output ports for redundant or distributed fabric system architectures when performing a retiming function.

In the transmit direction, the PM8385 transmitter can interface directly to optics, 1000BASE-CX (twinax) or serial backplanes. Selectable pre-emphasis per port is supported to counteract dielectric losses and allow maximum reach on printed circuit boards and twinax cable. Each output has selectable output swing and includes the source termination so that external resistors are not required. External capacitors can optionally be used on transmit and receive interfaces. In redundant system applications, the data source can be selected via the managemnet interface from either working or protection port.

The QuadPHY RT can be operated either standalone (via control pins) or through an optional serial management interface. The serial management interface supports both the standard Two-Wire Interface (TWI) and MDIO/MDC protocols. A fully maskable interrupt output pin is provided to signal the host device on events such as link error events. The QuadPHY RT provides optional extensive link monitoring to support backplane testing and in-system diagnostics.

5 Block Diagram

Figure 5 Block Diagram



6 Pin Diagram

The QuadPHY RT is packaged in a 196-pin CABGA package having a body size of 15 mm x 15 mm and a ball pitch of 1.0 mm.

Figure 6 Pin Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	VDD_33	VSS	VSS	VSS	RESETB	VSS	VSS	PREEMPH[0]	DLOLBYP_MASK	VSS	DVPRTAD[2]	VDD_33	VSS	A
B	VDD_33	VDD_33	HALF_RATE	CLK_SEL	MDIO_SDA	MDC_SCL	DLOLB	VDD_33	PREEMPH[1]	VDD_33	TWISEL	DVPRTAD[3]	VDD_33	VDD_33	B
C	RECEQUALIZE[1]	VSS	TDI	TCK	VDD_33	VDD_33	INTRB	VDD_33	EXTCAP	VDD_33	DVPRTAD[0]	DVPRTAD[4]	VSS	VSS	C
D	RECEQUALIZE[0]	TRSTB	TDO	VSS	TMS	VDD_33	VSS	NC	VSS	VSS	DVPRTAD[1]	VSS	VSS	VDD_33	D
E	PORT_DLOLB[2]	VDD_33	PORT_DLOLB[1]	PORT_DLOLB[0]	VSS	VSS	VSS	VSS	VSS	VSS	PORT_2G_RATE[0]	VSS	VDD_33	VDD_33	E
F	RX100/150[2]	RX100/150[3]	VDD_33	VDD_33	PORT_DLOLB[3]	VSS	VSS	VSS	VSS	VDD_18	PORT_2G_RATE[1]	PORT_2G_RATE[2]	AUTO_RATE_SEL	PORT_2G_RATE[3]	F
G	VSS	VDD_33	RX100/150[0]	RX100/150[1]	VSS	VSS	VSS	VSS	VSS	VSS	VDD_18	VSS	VSS	VDD_18	G
H	TX100/150[0]	TX100/150[1]	VSS	VSS	TX100/150[2]	VSS	VSS	VSS	VSS	VDD_18	VSS	RDIN[0]	RDIP[0]	VSS	H
J	RET_MODE	VDD_33	TX100/150[3]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	VDD_18	TDON[0]	TDOP[0]	J
K	FC_GE_RET_SEL	VDD_33	VDD_18	VDD_18	VSS	VDD_18	VSS	VDD_18	VSS	VDD_18	NC	RDIN[1]	RDIP[1]	VSS	K
L	VDD_18	VDD_18	VSS	VSS	VSS	NC	NC	VSS	NC	NC	VSS	VDD_18	TDON[1]	TDOP[1]	L
M	VSS	VSS	RPRES	VDD_18	VSS	VDD_18	NC	VDD_18	RDIN[3]	VDD_18	RDIN[2]	VDD_18	VDD_18	VSS	M
N	VDD_18	VDD_18	VSSA[1]	VDDA[1]	REFCLK_S	REFCLK_N	NC	TDON[3]	RDIP[3]	TDON[2]	RDIP[2]	VSS	VDD_18	VDD_18	N
P	VSS	VDD_18	VSSA[0]	VDDA[0]	VSS	REFCLK_P	VSS	TDOP[3]	VSS	TDOP[2]	VSS	VSS	VDD_18	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

7 Pin Description

Table 1 Gigabit Ethernet and Fibre Channel Port Pin Descriptions

Pin Name	Type	Pin No.	Function
RDIP[3] RDIN[3] RDIP[2] RDIN[2] RDIP[1] RDIN[1] RDIP[0] RDIN[0]	Input	N9, M9 N11, M11 K13, K12 H13, H12	**Receive Differential Input Positive/Negative (RDIP[3:0], RDIN[3:0])** RDIP and RDIN are the high-speed differential inputs used for 1.25Gbit/s Gigabit Ethernet or 1.0625 Gbit/s / 2.125 Gbit/s Fibre Channel inputs. Each input pair is internally AC coupled and terminated with a selectable 100 or 150 Ω termination. These inputs are ignored during Serial Loopback. Do not use pull-up/pull-down resistors on the high-speed differential inputs. These inputs can be left unconnected when this channel is disabled.
TDOP[3] TDON[3] TDOP[2] TDON[2] TDOP[1] TDON[1] TDOP[0] TDON[0]	Output	P8, N8 P10, N10 L14, L13 J14, J13	**Transmit Differential Output Positive/Negative (TDOP[3:0], TDON[3:0])** TDOP and TDON are the high-speed outputs used for the 1.25Gbit/s Gigabit Ethernet or 1.0625 Gbit/s / 2.125 Gbit/s Fibre Channel outputs and are internally terminated with a selectable 100 or 150 Ω differential termination. These outputs are pulled high through a terminating resistor when disabled via management register control.

Table 2 Port Control and Status Pins – 3.3 V I/O

Pin Name	Type	Pin No.	Function
DLOLBYP_MASK	Input	A10	**Performance Monitor Enable** When DLOLBYP_MASK is set to logic 0, Performance Monitoring is enabled. Each receive input can be fully monitored for loss of link, link errors, and link level violations. When DLOLBYP_MASK is set to logic 1 performance monitoring is disabled. Performance monitoring is only supported in Retimer Modes (not supported in Repeater Modes). This input has an internal 50 KΩ pull-up resistor.
EXTCAP	Input	C9	**External Capacitor Select** This pin selects the use of external capacitors for all high-speed input ports on power-up when set to logic 1. When set to logic 0, this pin selects the use of the internal coupling capacitors for all high-speed input ports on power-up. After power-up, the use of external capacitors can be programmed in the registers on a per port basis. High-speed input ports are not DC coupled internally. This input has an internal 50 KΩ pull-down resistor.

<table>
<tr><th>Pin Name</th><th>Type</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>PREEMPH[1]
PREEMPH[0]</td><td>Input</td><td>B9,
A9</td><td>Pre-emphasis Select
The PREEMPH pins select the level of pre-emphasis used on the serial transmit outputs of all ports on power-up. After power-up, the level of pre-emphasis can be programmed in the registers on a per port basis. The amount of pre-emphasis is dictated by the following equation:
$a-bz^{-1}$, where the coefficients a and b are set :
<table>
<tr><th>PREEMPH[1:0]</th><th>A</th><th>B</th><th>Pre-emphasis</th></tr>
<tr><td>00</td><td>1</td><td>0</td><td>0dB (off)</td></tr>
<tr><td>01</td><td>0.875</td><td>0.125</td><td>2.5 dB</td></tr>
<tr><td>10</td><td>0.75</td><td>0.25</td><td>6.0dB</td></tr>
<tr><td>11</td><td>0.667</td><td>0.333</td><td>9.5dB</td></tr>
</table>
PREEMPH[1:0] inputs have internal 50 KΩ pulldowns.
NOTE: Pre-emphasis is not supported in half-rate mode.</td></tr>
<tr><td>RECEQUALIZE[1]
RECEQUALIZE[0]</td><td>Input</td><td>C1
D1</td><td>Receive Equalization Select
The RECEQUALIZE pins select the level of equalization used on the serial receive inputs of all ports on power-up. After power-up, the level of equalization can be programmed in the registers on a per port basis.
<table>
<tr><th>RECEQUALIZE [1:0]</th><th>Equalization</th><th>Description</th></tr>
<tr><td>00</td><td>Max Equalization</td><td>Both stages enabled</td></tr>
<tr><td>01</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>10</td><td>Moderate Equalization</td><td></td></tr>
<tr><td>11</td><td>No Equalization</td><td>1st & 2nd Stage Eq-off (default for 2.125Gbit/s)</td></tr>
</table>
RECEQUALIZE[1] has an internal 50 KΩ pullup.
RECEQUALIZE[0] has an internal 50 KΩ pulldown.</td></tr>
</table>

Pin Name	Type	Pin No.	Function
RX100/150[3] RX100/150[2] RX100/150[1] RX100/150[0]	Input	F2 F1 G4 G3	**Receive 100 or 150 Ω Termination Select** The RX100/150[X] input selects the impedance of the termination between the RDIP[X] and RDIN[X] inputs. When set to logic 0, the RX100/150[X] forces the RDIP[X] and the RDIN[X] inputs to match a 100 Ω differential termination. When set to logic 1, the RX100/150[X] forces the RDIP[X] and the RDIN[X] inputs to match a 150 Ω differential termination. These inputs each have an internal 50 KΩ pull-down resistor.
TX100/150[3] TX100/150[2] TX100/150[1] TX100/150[0]	Input	J3 H5 H2 H1	**Transmit 100 or 150 Ω Termination Select** The TX100/150[X] input selects the impedance of the termination on the TDOP[X] and TDON[X] outputs. When set to logic 0, the TX100/150[X] forces the TDOP[X] and the TDON[X] outputs to match a 100 Ω termination. When set to logic 1, the TX100/150[X] forces the TDOP[X] and the TDON[X] outputs to match a 150 Ω termination. These inputs each have an internal 50 KΩ pull-down resistor.
RET_MODE	Input	J1	**Retimer Mode Select** The RET_MODE pin selects the retimer data path when set to logic 1 or as the repeater data path when set to logic 0. This input has an internal 50 KΩ pulldown resistor.
FC_GE_RET_SEL	Input	K1	**GE FC Retimer Select** The FC_GE_RET_SEL pin selects the device to operate as a Fibre Channel Retiming device when set to logic 1 or as a Gigabit Ethernet Retiming Device when set to logic 0. This input has an internal 50 KΩ pullup resistor.
INTRB	Output	C7	**Interrupt Output** This output signal goes to logic 0 to indicate when an interrupt condition has occurred. Interrupt condition is defined as change of status of any port due to Port_DLOLB. The interrupt output can be masked and cleared through mask interrupt registers. This output is an Open Drain and requires an external pull-up.
DLOLB	Output	B7	**Digital Loss of Link** This pin indicates the combined state of the Digital Loss of Link logic for all active receivers. Logic 0 indicates that one or more active channels has lost link. Logic 1 indicates that all active channels are receiving valid data.
PORT_DLOLB[3] PORT_DLOLB[2] PORT_DLOLB[1] PORT_DLOLB[0]	Output	F5 E1 E3 E4	**Port Digital Loss of Link** These pins indicate the state of each port's Digital Loss of Link logic for all active receivers. Logic 0 indicates that the respective channel has lost link. Logic 1 indicates that the respective channel is receiving valid data.

Pin Name	Type	Pin No.	Function
PORT_2G_RATE[3] PORT_2G_RATE[2] PORT_2G_RATE[1] PORT_2G_RATE[0]	Output	F14 F12 F11 E11	**Port Rate Detected** These pins indicate the Fibre Channel rate detected of each port's receive logic for all active receivers. Logic 0 indicates that the respective channel has detected the rate to be 1.0625 Gbit/s. Logic 1 indicates that the respective channel has detected the rate to be 2.125 Gbit/s.

Table 3 Management Interface Pin Descriptions – 3.3 V I/O

Pin Name	Type	Pin No.	Function
RESETB	Input	A6	**Device Reset** This input resets the device to a known state when set to a logic 0. All registers go to default values, all state machines are reset, and all data path flip-flops are reset. RESETB should be held low for at least 100 uS. If RESETB has been asserted, the CSU requires RESETB be negated for at least 200 uS to regain lock. Note that this pin should not be asserted for very long periods of time (many minutes or more) .
DVPRTAD[4] DVPRTAD[3] DVPRTAD[2] DVPRTAD[1] DVPRTAD[0]	Input	C12 B12 A12 D11 C11	**Device Port Address (DVPRTAD[4:0])** These address terminals are used to assign a unique address to each QuadPHY RT. Note that the address is assigned to the entire chip, not to individual ports within the chip. When TWISEL is set to logic 0, DVPRTAD[4:0] pins are used as the port address according to the IEEE 802.3ae Clause 45 Management Data Interface specification. When TWISEL is set logic 1, DVPRTAD[4:0] pins are used as the lower 5 bits of the slave address according to the TWI protocol; the most significant bit of the slave address is not provided and assumed to be 0.
TWISEL	Input	B11	**Two-Wire Interface Select** When set to logic 1, the Management Interface operates using the standard Two-Wire Interface (TWI) protocol. When set to logic 0, the Management interface operates according to the IEEE 802.3ae Clause 45 Management Data Interface specification. This input has an internal 50 KΩ pull-up resistor.
MDC_SCL	Input with schmit trigger	B6	**Management Data Clock – Serial Clock** This signal is part of the device 2-wire serial control interface. This signal is used to clock data transfer to and from the serial management interface registers. When TWISEL is logic 1, this pin operates as the serial clock for TWI transfers. When TWISEL is logic 0, this pin operates as the Management Interface Clock.

Pin Name	Type	Pin No.	Function
MDIO_SDA	I/O	B5	**Management Data Input/Output – Serial Data** This signal is part of the device 2-wire serial control interface. When TWISEL is logic 1, this pin operates as the bi-directional serial data port for TWI transfers. When TWISEL is logic 0, this pin operates as the Management Interface bi-directional serial data port. In TWI mode, the bi-directional MDIO_SDA pin operates as an open-drain when outputting, and requires an external pullup resistor (1 KΩ to 10 KΩ).

Table 4 JTAG Test Pin Descriptions – 3.3V I/O

Pin Name	Type	Pin No.	Function
TMS	Input	D5	**JTAG (IEEE 1149.1) Test Mode Select Input** This input controls the test operations that can be carried out using the IEEE 1149.1 test access port. This input has an internal 50 KΩ pullup resistor.
TCK	Schmit input trigger	C4	**JTAG (IEEE 1149.1) Test Clock Input.** This signal provides timing for test operations that can be carried out using the IEEE 1149.1 test access port.
TDI	Input	C3	**JTAG (IEEE 1149.1) Test Data Input** When the QuadPHY RT is configured for JTAG operation, this input carries test data into the device via the IEEE 1149.1 test access port. This input has an internal 50 KΩ pullup resistor.
TDO	Output	D3	**JTAG (IEEE 1149.1) Test Data Output** This signal carries test data out of the QuadPHY RT via the IEEE 1149.1 test access port.
TRSTB	Schmit input trigger	D2	**JTAG (IEEE 1149.1) Test Reset Input** Provides an asynchronous reset to the 1149.1 test access port. This input has an internal 50 KΩ pullup resistor.

Table 5 Clock, Control and Status Pin Descriptions – 3.3 V I/O excluding REFCLK

Pin Name	Type	Pin No.	Function
REFCLK_P REFCLK_N	Input	P6 N6	**Reference Clock - Differential** This input requires a low jitter differential reference clock operating at 106.25 MHz ±100 ppm for Fibre Channel operation or 125 MHz ±100 ppm for Gigabit Ethernet Retimer operation. The Clock Synthesis PLL uses this clock to generate a phase locked internal 20x clock for serialization and deserialization. These pins are internally terminated with a 100 Ω and require 0.01uF external AC coupling capacitor.

Pin Name	Type	Pin No.	Function
REFCLK_S	Input	N5	**Reference Clock – Single-Ended** This input requires a low jitter reference clock operating at 106.25 MHz ±100 ppm for Fibre Channel operation or 125 MHz ±100 ppm for Gigabit Ethernet Retimer operation. The Clock Synthesis PLL uses this clock to generate a phase locked internal 20x clock for serialization and deserialization. REFCLK_S input is tolerant of 3.3 V.
CLK_SEL	Input	B4	**Reference Clock Select** When set to logic 1, selects a single-ended reference clock, REFCLK_S, as input to the PLL. When set to logic 0, selects a differential reference clock, REFCLKP, REFCLKN, as input to the PLL. This input has an internal 50 KΩ pulldown resistor.
AUTO_RATE_SEL	Input	F13	**Automatic Rate Selection** When set to logic 1, all ports will automatically detect the data rate of 1.0625 Gbit/s or 2.215 Gbit/s and operate at that rate. When set to logic 0, the HALF_RATE pin will select the operating rate of all ports. If the FC_GE_RET_SEL pin is set to logic 0, the AUTO_RATE_SEL pin must be set to logic 0. This input has an internal 50 KΩ pulldown resistor.
HALF_RATE	Input	B3	**1 Gbit/s Operation Select** When set to logic 1 selects 1.0625 / 1.25 Gbit/s operation on all ports. When set to logic 0 selects 2.125 Gbit/s operation on all ports. If the FC_GE_RET_SEL pin is set to logic 0, the HALF_RATE pin must be set to logic 1. This input has an internal 50 KΩ pulldown resistor.

Table 6 Supply and Reference Pin Descriptions

Pin Name	Type	Pin No.	Function
RPRES	Input	M3	**Terminal for a Precision Resistor** A precision 10 KΩ 1/8 W, 1% reference resistor is connected between this terminal and ground. This resistor sets the internal reference current sources.
VDD_18[24:0]	Power	F10 G11 G14 H10 J12 K3 K4 K6 K8 K10 L1 L2 L12 M4 M6 M8 M10 M12 M13 N1 N2 N13 N14 P2 P13	**Digital Core Power Supply** 1.8 V ± 5%

Pin Name	Type	Pin No.	Function
VDD_33[21:0]	Power	A2 A13 B1 B2 B8 B10 B13 B14 C5 C6 C8 C10 D6 D14 E2 E13 E14 F3 F4 G2 J2 K2	**Digital quiet I/O Power Supply** 3.3 V ± 5%
VDDA[1] VDDA[0]	Power	N4 P4	**Analog Power Supply** 1.8 V ± 5% analog supply for PLL only.
VSSA[1] VSSA[0]	Ground	N3 P3	**Analog ground for PLL** These pins should be tied to the same ground plane as the VSS pins.
VSS[72:0]	Ground	A1 A3 A4 A5 A7 A8 A11 A14 C2 C13 C14 D4 D7 D9 D10 D12 D13 E5 E6 E7 E8 E9 E10 E12 F6 F7 F8 F9 G1 G5 G6 G7 G8 G9 G10 G12 G13 H3 H4 H6 H7 H8 H9 H11 H14 J4 J5 J6 J7 J8 J9 J10 K5 K7 K9 K14 L3 L4 L5 L8 L11 M1 M2 M5 M14 N12 P1 P5 P7 P9 P11 P12 P14	Ground
NC[8:0]	No Connect	D8 J11 K11 L10 L9 L7 L6 M7 N7	No Connect.

8 Functional Description

The following sections detail the major modes of operation and the functional description of the QuadPHY RT. The QuadPHY RT supports two main modes of operation for Gigabit Ethernet and 1/2G Fibre Channel as listed in Table 7; and is composed of five main system blocks, SERDES Reclocker, Receive Retimer/Monitor, Transmit Control, Cross Connect and the Packet Generator /Comparator. In addition to repeating or retiming, the non-blocking cross-connect provides significant flexibility to configure the device for redundancy, multi-cast or broadcast.

Table 7 QuadPHY RT Modes of Operation

QuadPHY RT Mode	Description
Repeater Mode	Recovered serial data is retimed to recovered clock as shown in Figure 7
Retimer Mode	Recovered serial data is retimed to local reference clock as shown Figure 8

Figure 7 QuadPHY RT in Repeater Mode

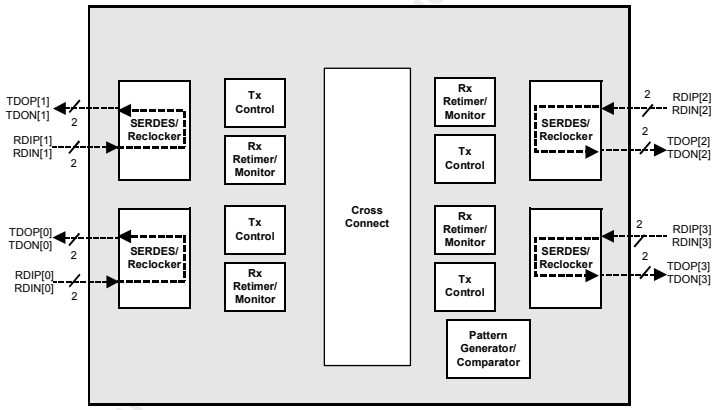
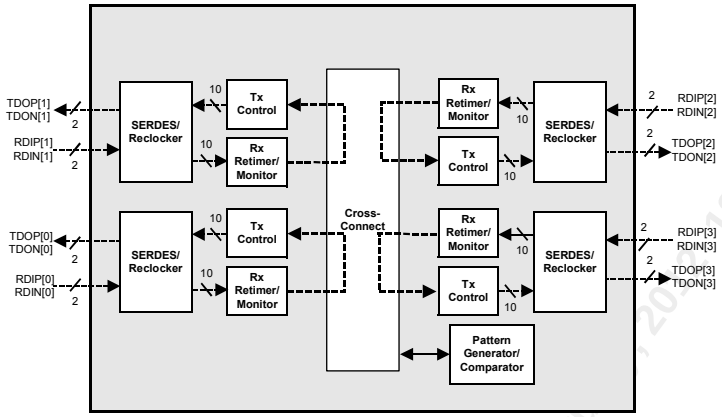


Figure 8 QuadPHY RT in Retimer Mode



8.1 Mode Configuration

The major functional modes of the QuadPHY RT can be configured through simple pin configuration using the Port Control pins. Table 8 summarizes the configuration requirements for the various operating modes.

Table 8 Mode Configuration through Control Pins

Operating Mode	DLOLBYP_MASK	RET_MODE	AUTO_RATE_SEL	HALF_RATE	FC_GE_RET_SEL
GigE/1G FC Repeater	1	0	0	1	X
2G FC Repeater	1	0	0	0	X
GigE Retimer	0	1	0	1	0
1G FC Retimer	0	1	1/0[1]	1[2]	1
2G FC Retimer	0	1	1/0[1]	0[2]	1

1. AutoRate Detection for Fibre Channel Retimer Modes is optional. Set AUTO_RATE_SEL to '1' to enable AutoRate Detection.

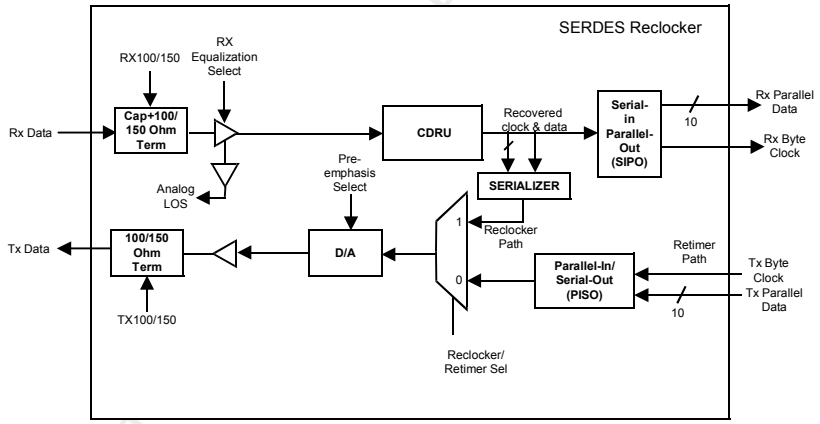
2. When AutoRate Detection is enabled the HALF_RATE pin is ignored.

8.2 SERDES Reclocker Block

The SERDES Reclocker block provides clock and data recovery and optional serial to parallel data conversion for an incoming Gigabit Ethernet or 1/2 Gigabit Fibre Channel data stream. Two modes of operation are provided for Repeater and Retimer applications. In repeater mode, the SERDES Reclocker block is used to recover the clock and data for transmission on the associated transmit data path. In Retimer mode after the data is recovered it is converted from a serial to a parallel data stream to be sent to the upstream Retimer block. The SERDES Reclocker receive channel contains the subsystems to recover clock and data (Clock Data Recovery Unit - CDRU), perform optional receive equalization, and convert the data from serial to 10-bit parallel format (Serial In Parallel Out – SIPO).

The SERDES Reclocker block also provides the parallel to serial conversion of 10B data received from the Receive Retimer and Monitor via the Cross Connect block. The serial data is then transmitted on to the high-speed channel via selectable termination and optional programmable pre-emphasis and programmable output swing.

Figure 9 SERDES Reclocker Block Diagram



8.2.1 Repeater Receive Data Flow

There are two paths for receive data to take through the block depending on whether the Repeater or Retimer mode is enabled. In Repeater mode, the receive data goes through the clock and data recovery process. The data is then re-transmitted out through the Serializer to the output buffers. The data is transmitted at the same rate as the input data is received using the recovered clock. Programmable receive equalization (Table 9) provides robust data recovery of highly degraded input signals. The Repeater path attenuates the jitter with minimum latency.

8.2.2 Retimer Receive Data Flow

For the QuadPHY RT Retimer mode, the data goes through the clock and data recovery process, including optional programmable receive equalization (Table 9). The data is then converted from serial to 10-bit parallel via the SIPO block. This data is the presented to the adjacent Retiming block. The data then passes through the retiming logic back to the PISO. In this mode the data is transmitted out at the local clock rate. The difference in the clock rate is handled through the elastic buffer in the digital domain. This mode produces a high-speed output, which is fully compliant with Gigabit Ethernet or 1/2G Fibre Channel transmit jitter specifications.

Table 9 Programmable Receive Equalization Settings

Input Equalization Port [1:0]	Equalization	Comments
00	Max Equalization	Both stages enabled
01	Moderate-equalization	Do Not Use.
10	Moderate Equalization	Default
11	No Equalization	1st & 2nd Stage Eq-off

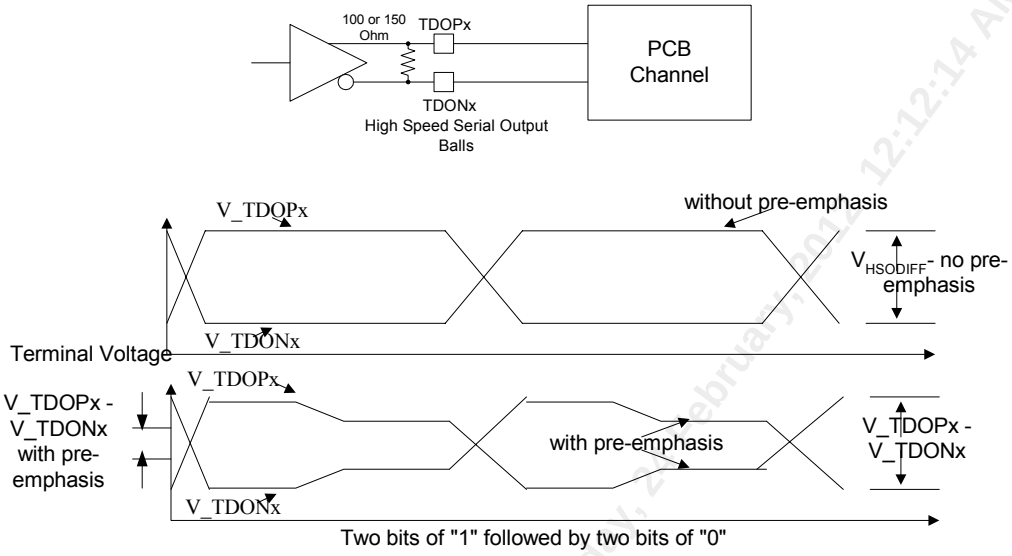
8.2.3 High-Speed Output Driver

High-speed output data is driven differentially and may directly drive optics, coaxial cable or PC-board interconnect. The QuadPHY RT supports pin selectable source output impedance of 100 Ω or 150 Ω differential. The TX100/150 pins control the selection on a per port basis of the source output impedance.

For back planes implemented with FR4 or similar materials, significant dielectric losses occur at high frequencies. These losses are frequency-dependent and severely limit the achievable separation between transmitter and receiver.

To mitigate this problem, the QuadPHY RT supports programmable pre-emphasis on the high-speed transmit outputs. The pre-emphasis circuit accentuates high-frequency components. Pre-emphasis compensates for loss of high-frequency components in the back plane material, so that the signal received at the far end is much cleaner and has a wider eye than data transmitted with simple bi-level output buffers. Figure 10 shows how pre-emphasis is performed.

Figure 10 Output Pre-Emphasis



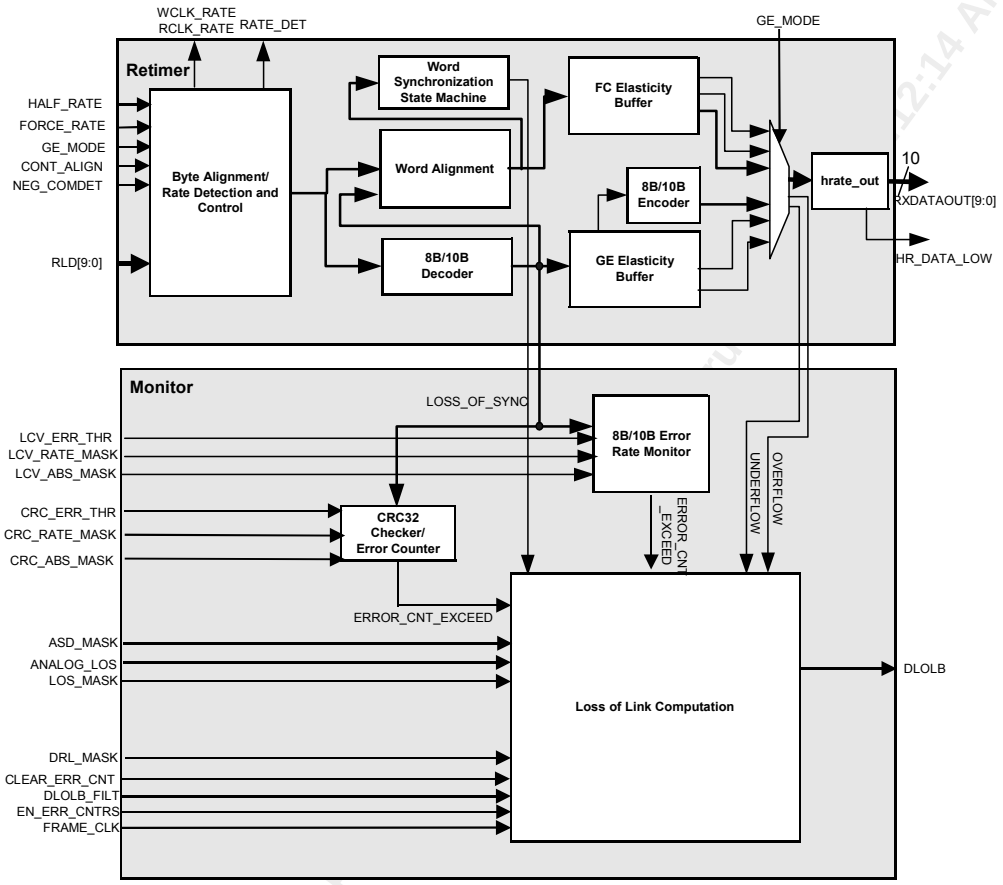
8.2.4 High-Speed Input Receiver

The high-speed input receiver contains a pin selectable parallel 100 Ω or 150 Ω terminating resistor and AC coupling. The RX100/150 pins control the selection on a per port basis of the terminating resistor value. The internal AC coupling provided is limited to the common-mode range of 0 to VDD_18 volts on a 1 V peak differential signal level. For a common-mode range greater than this, external AC capacitors are required and the EXTCAP pin or registers must be set to logic 1. This receiver accepts the high-speed differential signal and amplifies it with programmable equalization to the proper signal levels inside the chip. The input signal is also monitored for analog loss of signal.

8.3 Receive Retimer and Monitor

The receiver logic contains a Retimer function and data monitoring capabilities. The Retimer feature transfers the recovered data to the local clock to be retransmitted without the accumulated jitter from the serial inputs. The data path through the Retimer and all monitoring functions are enabled through registers. Figure 11 shows the Rx Retimer and Monitor functional blocks.

Figure 11 Rx Retimer and Monitor Block Diagram



8.3.1 Receive Retimer Function

The Retimer Logic is comprised of a Byte Alignment/Rate Detection block, Word Alignment block and State Machine, 8B/10B Encoder and Decoder, and an Elastic Buffer. The Byte Alignment logic searches for the 10B encoded incoming serial stream for a sequence defined in IEEE 802.3 and FC-FS as a comma. It has a unique position within a 10-bit word of a valid 10B coded data stream to simplify the detection of the proper alignment of incoming characters. The GE byte sync or the FC word sync blocks can also control the byte alignment logic to explicitly search for a comma.

For Gigabit Ethernet, byte alignment is performed by feeding the 8B10B decode output into the GE Byte synchronization block to determine when to align to a comma character in the data stream. Data alignment is done either explicitly in the loss_of_sync state, or in a continuous mode where alignment will take place on any comma character.

Fibre Channel data alignment occurs at both the byte and subsequent word levels. Word alignment partitions incoming 10B codes into groups of four characters that are aligned to the receive ordered set as defined in the FC-FC document. Similar to the Gigabit Ethernet mode, data alignment is done either explicitly in the loss_of_sync state, or in a continuous mode where alignment will take place on any comma character.

8.3.2 Fibre Channel 1 / 2 Gigabit Rate Detection (should not be used in GE mode)

The QuadPHY RT optionally performs rate detection between 1 Gigabit and 2 Gigabit Fibre Channel. The Fibre Channel rate detection block uses the word synchronization state from the alignment logic. The process starts in full rate mode, and searches for word synchronization. If word sync is not gained before a counter threshold, half rate mode is selected and word alignment is monitored. After successful word synchronization is monitored to ensure proper rate acquisition at which point RATE_DET output is set to high to indicate that a valid rate has been detected. Subsequent loss of word synchronization for more than TFAIL bytes will restart the rate detection process.

8.3.3 Elastic Buffers for Rate Compensation

Gigabit Ethernet Rate Compensation

The Gigabit Ethernet Elastic Buffer achieves clock tolerance compensation by inserting or deleting 2 octet wide IDLE sequences or 4 octet wide configuration patterns as needed. The GE Elastic Buffer will only delete an IDLE sequence when more than one IDLE sequence has been recognized. When the GE Elastic Buffer inserts an IDLE sequence after and IDLE sequence has been recognized. The IDLE sequence inserted is the same as the previous IDLE sequence received. The QuadPHY RT has a sixteen (16) character deep FIFO on each receive channel. This enables the QuadPHY RT to tolerate up to +/-100ppm clock differences on 16k byte packets with a 4 byte IPG. Larger packet sizes can be accommodated with larger IPG.

Fibre Channel Rate Compensation

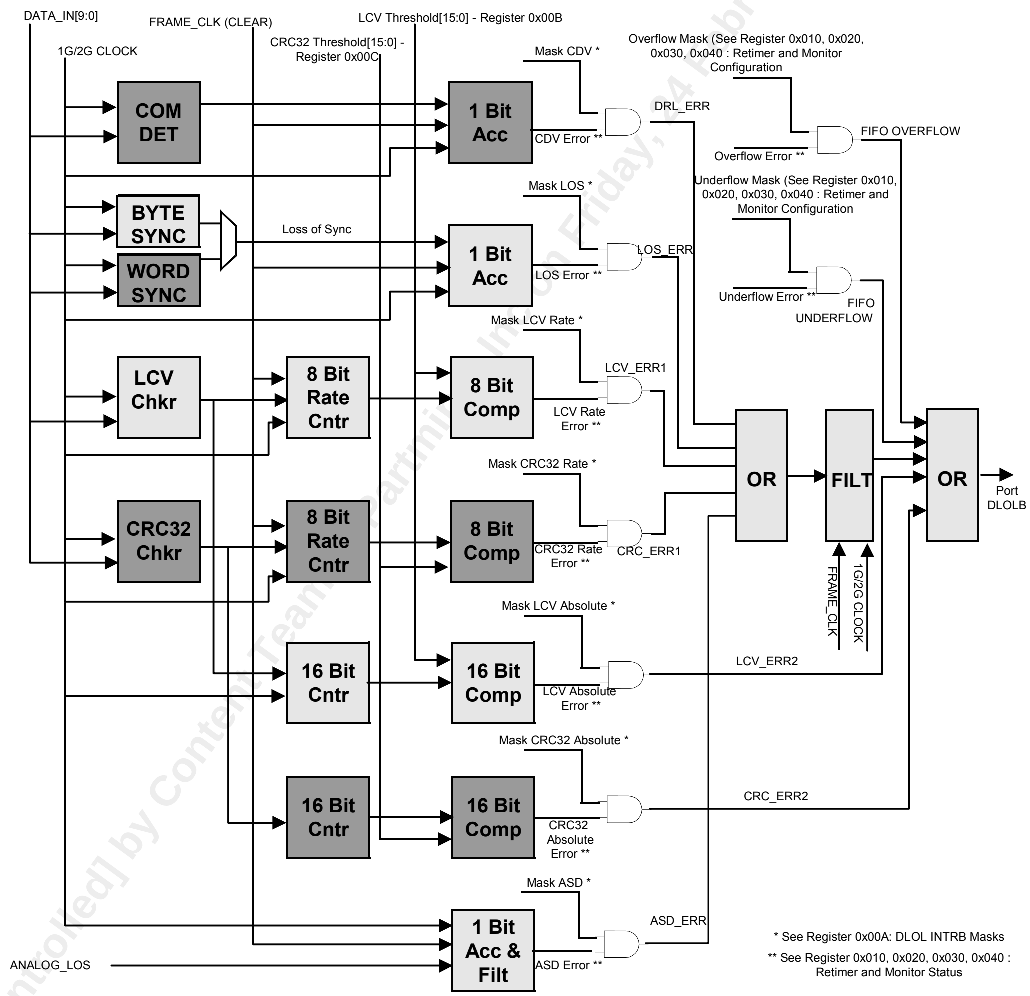
The Fibre Channel Elastic Buffer provides clock tolerance by inserting or deleting fill words comprised of specific IDLE or ARB ordered sets based on rules assigned to multiple buffer fill levels in the FC-AL-2 specification. In addition to supporting the 4 standard fill level states, an additional 5th non-standard fill level has been introduced in order to maintain data integrity under extreme conditions. There are two different scenarios when insertion or deletion will take place: between packets and during the transmission of primitive sequences for port initialization. ARB ordered sets (ARB(x), ARB(F0), and ARB(FF)) are inserted when a Fibre Channel loop is trying to arbitrate for the use of shared loop media, where IDLEs are inserted when packets are not being sent. Note that in addition to ARB or IDLE deletion, it is possible to remove primitive sequences such as LIPs, LPBs and LPEs from the data stream for clock skew management

Clock deviations are specified to +/-100 ppm within the FC_PH-x and FC-PI standards. The QuadPHY RT accommodates a worst-case clock rate difference is 200 ppm via a 16-byte deep FIFO. This depth is determined in part by the standard, which requires only 1 character for the insertion pending state, 1 word for the quiescent state, 1 word for the low priority deletion state and 1 word for the high priority deletion state [see FC-AL-2, Annex A].

8.4 Receive Monitor Function

The second function of the receive logic is to provide error detection and monitoring of data integrity. There are five classes of error detection and data monitoring within QuadPHY RT: 1) 8B/10B code violation and disparity errors, 2) a loss of synchronization indication from either the FC Word Synchronization State Machine or the GE compatible Byte Synchronization State Machine, 3) a low K28.5- received character density, 4) CRC32 errors, and 5) a filtered analog signal detect. A programmable combination of these five classes of errors generates the Digital Loss of Link signal Port DLOLB. See Figure 12.

Figure 12 PORT_DLOLB Generation



8.4.1 CRC Checker

The CRC checker (Fibre Channel mode only) implements a 32-bit polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1$$

The CRC is calculated on the frame header and payload. SOF and EOF delimiters are not included for calculation. This calculated CRC is compared with the word immediately following the payload and directly preceding the EOF. If it does not match, then the CRC error counter is incremented. There are two CRC error counters:

- 8-bit Rate Counter: This counter counts CRC32 errors in fixed time intervals that are dependent on the Frame Clk period. If the counter exceeds an 8-bit threshold at the end of the Frame Clk period, then a CRC32 rate error is generated. The counter is then cleared and this procedure is repeated over the next period. The threshold is the lower 8 bits of the input CRC threshold, CRC32 Threshold [7:0] (see “Register 0x00C: CRC32 Threshold”). Setting theMask CRC32 Rate bit in “Register 0x00A: DLOL INTRB Masks” high disables generation of PORT DLOLB from a CRC32 rate error.
- 16-bit (Absolute) Sticky Counter: This 16-bit counter only gets cleared through a reset or setting the Clear Error Counters bit in “Register 0x00D: Clear Error Counters”, or the Clear counters bit in “Register 0x010, 0x020, 0x030, 0x040 : Retimer and Monitor Configuration”. It is sticky at its maximum value of 0xFFFF. An absolute CRC32 error is generated whenever this counter exceeds the threshold (CRC32 Threshold [15:0]). Setting the Mask CRC32 Absolute bit high in “Register 0x00A: DLOL INTRB Masks” disables generation of PORT DLOLB from an absolute CRC32 error. This is not a rate counter. When the Clear Error Counters bit in “Register 0x00D: Clear Error Counters”, or the Clear counters bit in “Register 0x010, 0x020, 0x030, 0x040 : Retimer and Monitor Configuration” is asserted, the contents of this code error rate counter is loaded into “Register 0x013, 0x023, 0x033, 0x043 : Retimer and Monitor CRC Error Count” and then each counter is set to logic 0.

There are 11 different SOF delimiters and 8 different EOF delimiters defined by the standard. All of them are identified to demarcate the boundaries of the frame.

The absolute and rate counters are disabled when DLOLBYP_MASK pin is set to logic 1.

Table 10 List of SOF/EOF Delimiters

Abbr	Delimiter Function	Beginning RD	Ordered Set
SOFc1	SOF Connect Class 1	Negative	K28.5 – D21.5 – D23.0 – D23.0
SOFi1	SOF Initiate Class 1	Negative	K28.5 – D21.5 – D23.2 – D23.2
SOFn1	SOF Normal Class 1	Negative	K28.5 – D21.5 – D23.1 – D23.1
SOFi2	SOF Initiate Class 2	Negative	K28.5 – D21.5 – D21.2 – D21.2
SOFn2	SOF Normal Class 2	Negative	K28.5 – D21.5 – D21.1 – D21.1
SOFi3	SOF Initiate Class 3	Negative	K28.5 – D21.5 – D22.2 – D22.2
SOFn3	SOF Normal Class 3	Negative	K28.5 – D21.5 – D22.1 – D22.1
SOFc4	SOF Activate Class 4	Negative	K28.5 – D21.5 – D25.0 – D25.0

Abbr	Delimiter Function	Beginning RD	Ordered Set
SOFi4	SOF Initiate Class 4	Negative	K28.5 – D21.5 – D25.2 – D25.2
SOFn4	SOF Normal Class 4	Negative	K28.5 – D21.5 – D25.1 – D25.1
SOFf	SOF Fabric	Negative	K28.5 – D21.5 – D24.2 – D24.2
EOFt	EOF Terminate	Negative	K28.5 – D21.4 – D21.3 – D21.3
		Positive	K28.5 – D21.5 – D21.3 – D21.3
EOFdt	EOF Disconnect Terminate – Class 1 or Class 4	Negative	K28.5 – D21.4 – D21.4 – D21.4
		Positive	K28.5 – D21.5 – D21.4 – D21.4
EOFa	EOF Abort	Negative	K28.5 – D21.4 – D21.7 – D21.7
		Positive	K28.5 – D21.5 – D21.7 – D21.7
EOFn	EOF Normal	Negative	K28.5 – D21.4 – D21.6 – D21.6
		Positive	K28.5 – D21.5 – D21.6 – D21.6
EOFni	EOF Normal Invalid	Negative	K28.5 – D10.4 – D21.6 – D21.6
		Positive	K28.5 – D10.5 – D21.6 – D21.6
EOFdti	EOF Disconnect Terminate-Invalid Class 1 or Class4	Negative	K28.5 – D10.4 – D21.4 – D21.4
		Positive	K28.5 – D10.5 – D21.4 – D21.4
EOFrt	EOF Remove-Terminate Class 4	Negative	K28.5 – D21.4 – D25.4 – D25.4
		Positive	K28.5 – D21.5 – D25.4 – D25.4
EOFrti	EOF Remove-Terminate Invalid Class 4	Negative	K28.5 – D10.4 – D25.4 – D25.4
		Positive	K28.5 – D10.5 – D25.4 – D25.4

8.4.2 CDV Checker

The CDV checker monitors comma density in Fibre Channel mode. The CDV Error status bit in "Register 0x011, 0x021, 0x031, 0x041 : Retimer and Monitor Status") is set if a /K28.5/ is not received within a Frame Clk period. Setting the Mask CDV bit in "Register 0x00A: DLOL INTRB Masks" high disables CDV Errors from generating PORT DLOLB.

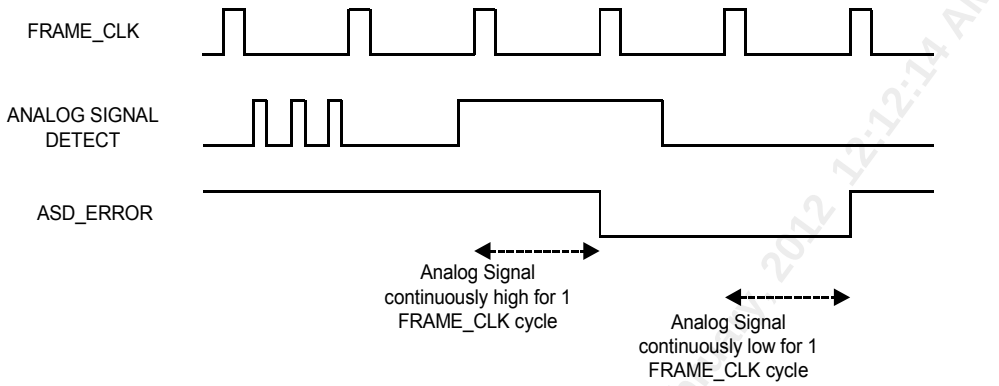
In Gigabit Ethernet mode the Mask CDV should be held high to prevent spurious PORT DLOLB generation.

8.4.3 ASD Checker

The ASD checker monitors the analog loss of signal for any change of status. The analog loss of signal is filtered to produce an error status (the ASD Error bit in "Register 0x011, 0x021, 0x031, 0x041 : Retimer and Monitor Status"). The ASD Error signal changes state only if the analog signal detect input remains at a constant value for one Frame Clk period as shown below. This hysteresis ensures that narrow transitions on the analog loss of signal are filtered out. Setting the Mask ASD bit in "Register 0x00A: DLOL INTRB Masks" high disables ASD Errors from generating PORT DLOLB.

The ASD checker is disabled when DLOLBYP_MASK pin is set to logic 1.

Figure 13 Analog Signal Detect Filtering



8.4.4 LCV Monitor

Line code violations and disparity errors are recorded in two types of LCV counters:

- 8-bit Rate Counter: This counter counts Line code violations and disparity errors in every Frame Clk period. If the counter exceeds an 8-bit threshold at the end of the Frame Clk period, then an LCV rate error is generated. The counter is then cleared and this procedure is repeated over the next period. The threshold is the lower 8 bits of the LCV_Threshold[7:0] bits in "Register 0x00B: LCV Threshold". Setting the Mask LCV Rate bit in "Register 0x00A: DLOL INTRB Masks" high disables generation PORT DLOLB from an LCV rate error.
- 16-bit (Absolute) Sticky Counter: This 16-bit counter only gets cleared through a reset or setting the Clear Error Counters bit in "Register 0x00D: Clear Error Counters", or the Clear counters register bit in "Register 0x010, 0x020, 0x030, 0x040 : Retimer and Monitor Configuration". It is sticky at its maximum value of 0xFFFF. Absolute LCV Error is generated whenever the counter exceeds the threshold (LCV Threshold [15:0]). Setting the Mask LCV Absolute bit high in "Register 0x00A: DLOL INTRB Masks" disables generation of PORT DLOLB from an Absolute LCV Error. This is not a rate counter. When the Clear Error Counters bit in "Register 0x00D: Clear Error Counters", or the Clear counters bit in "Register 0x010, 0x020, 0x030, 0x040 : Retimer and Monitor Configuration" is asserted, the contents of this code error rate counter is loaded into "Register 0x012, 0x022, 0x032, 0x042: Retimer and Monitor LCV Error Count" and then each counter is set to logic 0.

The absolute and rate counters are disabled when DLOLBYP_MASK pin is set to logic 1.

8.4.5 Loss of Synchronization Monitor

When the word synchronization block (in Fibre Channel mode) or the GE compatible byte synchronization block (in Gigabit Ethernet mode) indicates a loss of synchronization, this logic samples the loss of signal. An error signal, Loss of Sync, is generated when a loss of synchronization is detected at least once in a single Frame Clk period. Due to the built-in hysteresis in the word synchronization block, a loss of synchronization indicates a stream of invalid characters and is hence a catastrophic state. Setting Mask LOS in "Register 0x00A: DLOL INTRB Masks" high disables generation of PORT DLOLB on a Loss of Sync. The Loss of Sync Status bit is in "Register 0x011, 0x021, 0x031, 0x041 : Retimer and Monitor Status".

The loss of synchronization monitor is disabled when DLOLBYP_MASK pin is set to logic 1.

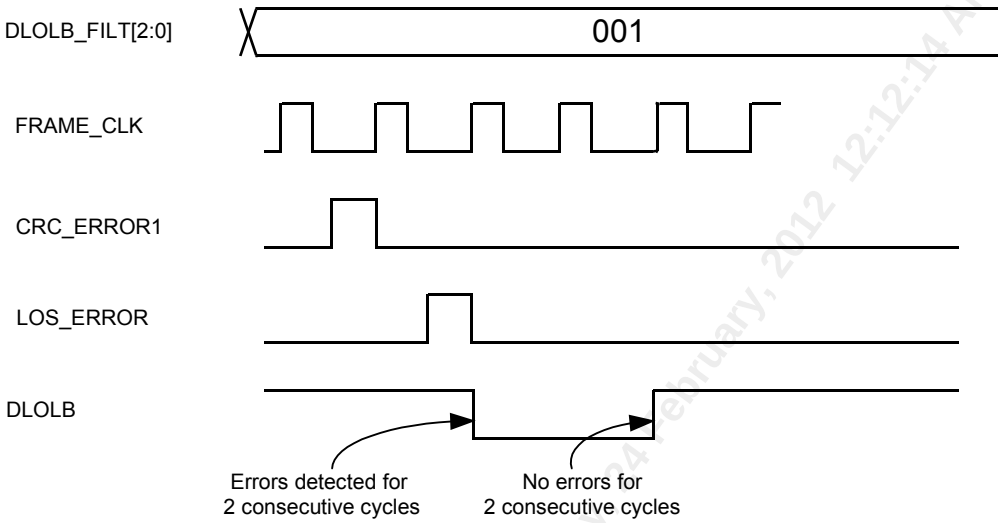
8.4.6 Overflow/Underflow Detection

Both FIFOs keep track of the read and write pointer differences; only one FIFO is active at a time so the respective outputs are muxed depending on the mode. When the pointers creep up too close to each other because of clock frequency differences, and the buffer is not able to insert/delete Fill Words or primitive sequences (Fibre Channel) or insert/delete IDLE or configuration patterns (Gigabit Ethernet) fast enough to keep the pointers separated, then there is a chance of data corruption. The buffer indicates this by raising its overflow or underflow flag. Overflow/underflow detection is not filtered. It is reflected immediately through the PORT DLOLB pin. The Overflow Mask and Underflow Masks bits are set in "Register 0x010, 0x020, 0x030, 0x040 : Retimer and Monitor Configuration", and are masked by default.

8.4.7 PORT DLOLB Generation

CRC rate errors, LCV rate errors, CDV errors, ASD errors and LOS errors are digitally filtered across a number of Frame Clk cycles. The filtered signal is ORed with CRC Error, LCV Error, FIFO Overflow and FIFO Underflow to generate the PORT DLOLB signal. The DLOLB filter[2:0] bits in "Register 0x002: Global Control" allow the user to set the number of consecutive frame clock cycles over which the ORed signal is filtered (size of the hysteresis window). Refer to section 6 for the various settings of DLOLB filter[2:0]. Refer to Figure 12 for a diagram of PORT_DLOLB generation. The figure below shows how a DLOLB is generated.

Figure 14 PORT_DLOLB Filtering



8.5 5 x 5 Cross connect

The 5 x 5 Cross connect provides non-blocking connections from the retimer of each receive port and the Pattern Generator block to all the transmit output ports and the Pattern Comparator. The Pattern Generator/Comparator connects to any link through the 5th port of the cross connect. The 5 x 5 Cross connect can be used to implement multicasting, broadcasting, protection switching and loopback switching.

The crossbar can be utilized when operating in GigE, 1G FC or 2G FC Retiming modes. The crossbar cannot be utilized when operating in a Reclocking mode. The routing of each input port through the crossbar is configurable through a single register access.

As the crossbar is a completely non-blocking, fully broadcast and multicast capable, it is possible to create flexible and optimized configurations that suit specific needs. A potential configuration for redundancy is a single input with recovered serial data retimed to local reference clock and multi-cast to working and protection ports as shown in Figure 7. Figure 16 shows a 1:3 mux configuration that could be used for simplifying connection of distributed switch fabric elements.

Figure 15 QuadPHY RT Redundancy Configuration Example

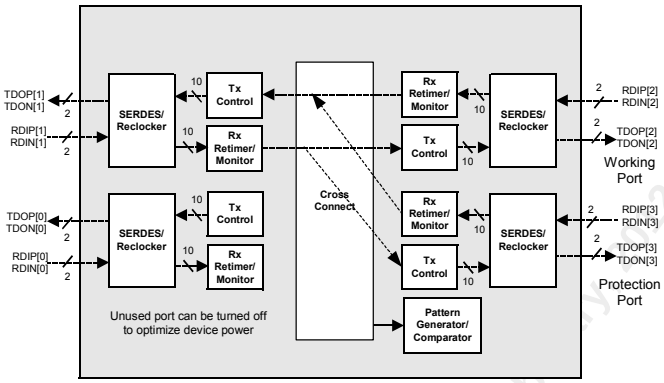
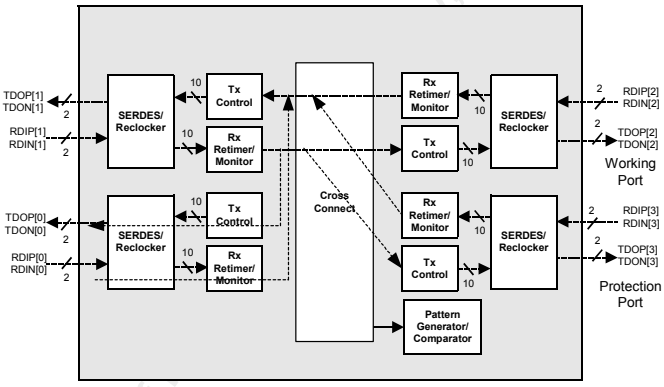


Figure 16 QuadPHY RT with Cross-Connect as 1:3 Mux



8.6 TX Control

The TX Control block transfers data from the ingress Receive Retimer/Monitor to the SERDES via the Cross Connect block. The Transmit FIFO allows the phase of Transmit clock to be arbitrary relative to the PLL reference clock (SYSCLK), which drives the Serializer and high-speed transmit logic. Note that the frequency of the SYSCLK and Transmit clock is the same.

8.7 Clock Synthesizer

The Clock Synthesizer uses a PLL to synthesize a clock from the REFCLK inputs. The frequency of the PLL clock is 20 times the frequency of REFCLK inputs. The synthesized clock is used by the SERDES/Reclocker blocks to generate recovered clocks and to provide an accurate and stable high speed transmit clock. The Clock Synthesizer also generates the internal core logic clock which is 212.5 MHz for FC and 250 MHz for GE.

Table 11 REFCLK and PLL Clock Combinations

REFCLK Frequency	Pin Setting	PLL Clock Frequency	Transmit/Receive Data Rate
125.00 MHz	FC_GE_RET_SEL = 0 HALF_RATE = 1	2.50 GHz	1.250 Gbit/s
106.25 MHz	FC_GE_RET_SEL = 1 HALF_RATE = 1	2.125 GHz	1.0625 Gbit/s
106.25 MHz	FC_GE_RET_SEL = 1 HALF_RATE = 0	2.125 GHz	2.125 Gbit/s

8.8 Management Interface

The QuadPHY RT can operate either in a standalone mode or through a 2-wire serial control interface. Device will power up with default settings.

8.8.1 2-Wire Serial Control (TWI Operation)

The TWI mode is selected by setting the TWISEL pin to logic 1. The TWI serial interface consists of two pins. One is a serial clock pin called MDC_SCL and the other is a data pin called MDIO_SDA. Data states on the MDIO_SDA line can only change while MDC_SCL is LOW. MDIO_SDA state changes while MDC_SCL is high are reserved for indicating START and STOP conditions. A HIGH to LOW transition of MDIO_SDA while MDC_SCL is HIGH is called a START condition and a LOW to HIGH transition is called a STOP condition.

The MDC_SCL and MDIO_SDA lines are connected to open drain buffers. Devices on the bus can pull them down (drive zero) but should not pull them up (cannot drive one). The pull up resistor on the bus pulls the line up when no one is driving a zero.

All transactions on the bus are 8-bit transactions. After every 8-bits transmitted the receiver will respond with a ninth bit called ACK (active LOW) except under special conditions when it may not send an ACK.

Internal Addressing Scheme

The last two bits of the slave address byte are used to implement the internal addressing scheme. The first 6 bits of the slave address byte are used for the slave address, which is pin programmable. If the last two bits are 00 it implies that this is an address write operation. If it is 10 it implies that it is a data write operation. A 01 implies a data read operation and 11 implies a data read increment operation in which the address is incremented after the operation is finished.

Write Operation

The master device generates a START condition and then sends an 8-bit slave address with the last two bits as “00”. The slave sends back an ACK if the address matches. The master then sends the high address bits (bits 15 through 8) with bit 15 transmitted first. The slave sends an ACK. The master then sends the low address bits (bits 7 through 0) of the internal address with bit 7 transmitted first. The slave sends an ACK. The slave stores these 16 address bits in an address register.

The master then generates a STOP condition and another START condition or it can generate a START condition without issuing a STOP condition first. This is called a repeated START condition. The master sends an 8-bit slave address with the last two bits as 10. The slave sends back an ACK if the address matches. The master then sends the high data bits (bits 15 through 8) with bit 15 transmitted first. The slave sends an ACK. The master then sends the low data bits (bits 7 through 0) of the data with bit 7 transmitted first. The slave sends an ACK. The Master then generates a STOP or repeated START condition.

Read Operation

The master device generates a START condition and then sends an 8-bit slave address with the last two bits as 00. The slave sends back an ACK if the address matches. The master then sends the high address bits (bits 15 through 8) with bit 15 transmitted first. The slave sends an ACK. The master then sends the low address bits (bits 7 through 0) of the internal address with bit 7 transmitted first. The slave sends an ACK. The slave stores these 16 address bits in an address register.

The master then generates a STOP condition and another START condition or it can generate a START condition without issuing a STOP condition first. This is called a repeated START condition. The master sends an 8-bit slave address with the last two bits as 01. The slave sends back an ACK if the address matches. The slave then sends the high data bits (bits 15 through 8) with bit 15 transmitted first. The master sends an ACK. The slave then sends the low data bits (bits 7 through 0) of the data with bit 7 transmitted first. The master does not generate an ACK and the slave leaves the data line HIGH for the master to generate a STOP or repeated START condition.

Read Increment Operation

The master device generates a START condition and then sends an 8-bit slave address with the last two bits as “00”. The slave sends back an ACK if the address matches. The master then sends the high address bits (bits 15 through 8) with bit 15 transmitted first. The slave sends an ACK. The master then sends the low address bits (bits 7 through 0) of the internal address with bit 7 transmitted first. The slave sends an ACK. The slave stores these 16 address bits in an address register.

The master then generates a STOP condition and another START condition or it can generate a START condition without issuing a STOP condition first. This is called a repeated START condition. The master sends an 8-bit slave address with the last two bits as “11”. The slave sends back an ACK if the address matches. The slave then sends the high data bits (bits 15 through 8) with bit 15 transmitted first. The master sends an ACK. The slave then sends the low data bits (bits 7 through 0) of the data with bit 7 transmitted first. The master does not generate an ACK and the slave leaves the data line HIGH for the master to generate a STOP or repeated START condition. The Slave also increments the internal address register. If the master needs to read the next address it can send a read or read increment frame without having to send the address frame.

Table 12 is an example of the TWI frame.

Table 12 Example of TWI frame

Frame Name	Start Cond.	Slave addr byte [7:0]	Ack	High Byte [15:8]	Ack	Low Byte [7:0]	Ack	Stop or Restart
Address	St	PPPPPP00	Ack	AAAAAAAA	Ack	AAAAAAAA	Ack	Sp/St
Write	St	PPPPPP10	Ack	DDDDDDDD	Ack	DDDDDDDD	Ack	Sp/St
Read	St	PPPPPP01	Ack	DDDDDDDD	Ack	DDDDDDDD		Sp/St
Read Inc	St	PPPPPP11	Ack	DDDDDDDD	Ack	DDDDDDDD	…	…

The PPPPPP stands for the top 6 bits of the slave's address on the system bus. These are pin programmable for the TSB. The last two bits of the slave address byte select the transaction (address, write, read or read inc.).

On a read transaction after the last bit of read data is transmitted by the slave the Master does not generate an ACK but instead generates a STOP or repeated START condition in the next cycle.

On a read increment transaction the Master sends an ACK as long as it wants the slave to keep sending data. When the Master decides to end the transaction it will not generate an ACK but instead generate a STOP or repeated START condition in the next cycle.

All address and data is 16 bits wide. So both the Master and Slave would need to send two 8-bit bytes to complete any transaction.

8.8.2 2-Wire Serial Control (MDIO/MDC Operation)

The QuadPHY RT also implements a Management Interface as defined in IEEE 802.3ae except that 3.3 V levels are supported instead of 1.2 V. This 2-wire interface consists of MDC_SCL (Management Data Clock) and MDIO_SDA (Management Data I/O) terminals. The Management Interface provides serial read/write access to internal control and status registers supporting up to 31 addressable devices. The MDIO mode is selected by setting the TWISEL pin to logic 0.

The QuadPHY RT supports indirect addressing, as proposed in *IEEE* draft P802.3ae. Table 13 illustrates the addressing of both the global and per-port registers. The order of bit transmission is from left to right.

Table 13 Management Interface Frame Format

FRAME	PRE	ST	OP	PRTAD	DEVAD	TA	ADDRESS/DATA	IDLE
Address	1…1	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAAAAA	Z
Write	1…1	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDDDD	Z
Read	1…1	00	11	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z
Read inc.	1…1	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDDD	Z

There is a sixteen-bit address register that stores the address of the register to be accessed by data transaction frames. Address frames overwrite the address register.

Write, Read and Read-increment frames access the register whose address is stored in the address register.

Upon receiving a Read-increment frame and having completed the read operation, the address register is incremented by one except when the address register contains decimal 65535 or Hex FFFF value.

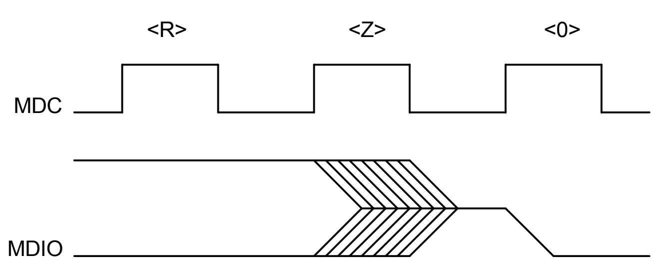
The IDLE condition on MDIO_SDA is a high impedance state. All three-state drivers shall be disabled and the pull-up resistor will pull the MDIO_SDA line to a one.

At the beginning of each transaction, the management interface controller must send a sequence of 32 contiguous logic 1 bits (PRE) on MDIO_SDA with 32 corresponding cycles on MDC_SCL to provide the QuadPHY RT with a pattern that it can use to establish synchronization. The QuadPHY RT observes a sequence of 32 contiguous 1 bits on MDIO_SDA with 32 corresponding cycles on MDC_SCL before it responds to any transaction. This preamble is followed by a start of frame (ST) which is the “00” bit sequence. Start of frame is followed by the operation code (OP), which is defined in the table above.

Following the operation code is the 5-bit port address (PRTAD). MSB is transmitted/received first. The port address is followed by a 5-bit device address (DEVAD). Each port can have 32 unique device addresses. Device address zero is reserved and should not be used. MSB is transmitted/received first. The QuadPHY RT will only respond to management interface accesses where the PRTAD matches DVPRTAD[4:0] pins and the DEVAD must match the device address 0x04.

A 2-bit time spacing called turnaround (TA) to avoid contention during a read transaction follows the device address. For a read transaction, both the management interface controller and the QuadPHY RT remain in a high-impedance state for the first bit time of the turnaround. The QuadPHY RT drives a 0 bit during the second bit time of the turnaround of a read transaction. During a write transaction, the management interface controller drives a 1 bit for the first bit time of the turnaround and a 0 bit for the second bit time of the turnaround.

Figure 17 Behavior of MDIO_SDA During TA Field of a Read Transaction



An address/data field that is 16 bits follows the turnaround bits. First bit transmitted/received is bit 15 (MSB).

8.9 Pattern Generator/Comparator

The Pattern Generator/Comparator is connected to the 5th receive and transmit port on the Crossbar. This enables any port to be isolated from its loop, connected to the Pattern Generator/Checker and extensively self-tested prior to insertion in the loop. An isolated port can also be enabled to communicate with an external device. The link to the device can be extensively tested prior to insertion of the device into the loop.

8.9.1 Pattern Generator

The Pattern Generator can be used to send one of seven fixed test patterns for jitter testing and proving link functionality in conjunction with the Pattern comparator. Setting the Pattern Generator Enable bit in the PATTERN_GEN register to logic 1 will activate the Pattern generator. The transmitted test pattern is selected by setting the Pattern Type [2:0] bits in the PATTERN_GEN register. A description of these test patterns is included in **Error! Reference source not found.**.

Table 14 Pattern Generator Test Patterns

Pattern Type [2:0]	Description
000	Compliant RPAT[2]
001	Low Transition Density Pattern[2]
010	Compliant Jitter Tolerance Pattern[1,2]
011	Half Rate and Quarter Rate Pattern[2]
100	Low Frequency Pattern[2]
101	Supply Noise Pattern[2]
110	CUSTOM Pattern[1]

Note:

1. These patterns can be used in conjunction with the pattern comparator to test connectivity between links.

2. These test patterns are described in the Jitter Working Group Technical Report Revision 10, June 9, 1999.

Compliant RPAT Pattern

The Compliant RPAT pattern is defined by the Jitter Group Technical Report Revision 10, June 9, 1999. It is described in Table 15. The pattern is constantly transmitted.

Table 15 Compliant RPAT

Starting Disparity	10B Code	Number of Cycles Character is Transmitted
-	K28.5, D21.4, D21.5, D21.5	Idle Primitive transmitted 6 times
	K28.5, D21.5, D22.1, D22.1	SOFn3 transmitted 1 time

Starting Disparity	10B Code	Number of Cycles Character is Transmitted
	D30.5, D23.6, D3.1, D7.2 D11.3, D15.4, D19.5, D20.0 D30.2, D27.7, D21.1, D25.2	RPAT Pattern transmitted 16 times
	D14.7, D3.1, D21.2, D22.0	CRC transmitted 1 time
	K28.5, D21.5, D21.6, D21.6	EOFn transmitted 1 time

Low Transition Density Pattern

The Jitter Group Technical Report Revision 10, June 9, 1999, defines this pattern. It is described in Table 16. This pattern is constantly transmitted.

Table 16 Low Transition Density Pattern

Starting Disparity	10B Code	Number of Cycles Character is Transmitted
+	D14.7	1
	D30.7	1
	D7.6	1
	D17.7	1
	D30.7	1
	D7.1	1
	D30.3	6
	D28.7	1
	D3.7	1
	D28.7	1
	D3.7	1

Compliant Receive Jitter Tolerance Pattern (CJTPAT)

The Jitter Group Technical Report Revision 10, June 9, 1999, defines this pattern. It is described by Table 17. This pattern is constantly transmitted.

Table 17 Compliant Receive Jitter Tolerance Pattern (CJTPAT)

Starting Disparity	10B Code	Number of Cycles Character is Transmitted
-	K28.5, D21.4, D21.5, D21.5	Idle Primitive transmitted 6 times
	K28.5, D21.5, D22.1, D22.1	SOFn3 transmitted 1 time
	D30.3, D30.3, D30.3, D30.3	Low Density Transition Pattern transmitted 41 times
	D30.3, D30.3, D30.3, D20.3	1
	D30.3, D11.5, D21.5, D21.5	1

Starting Disparity	10B Code	Number of Cycles Character is Transmitted
	D21.5, D21.5, D21.5, D21.5	High Density Transition Pattern transmitted 12 times
	D21.5, D30.2, D10.2, D30.3	1
	D30.3, D30.3, D30.3, D30.7	1
	D21.7, D14.1, D22.7, D29.6	CRC transmitted 1 time
	K28.5, D21.5, D21.6, D21.6	EOFn transmitted 1 time

Half Rate and Quarter Rate Pattern

The Jitter Group Technical Report Revision 10, June 9, 1999, defines this pattern. It is described by Table 18. This pattern is constantly transmitted.

Table 18 Half Rate and Quarter Rate Pattern

10B Characters	Number of Consecutive Characters
D21.5	8
D24.3	8
D10.2	8
D25.6, D6.1	8
D6.1, D25.6	8

Low Frequency Pattern

The Jitter Group Technical Report Revision 10, June 9, 1999, defines this pattern. It is described by Table 19. This pattern is constantly transmitted.

Table 19 Low Frequency Pattern

Starting Disparity	10B Code	Number of Cycles Character is Transmitted
+	D11.5	12
	D11.7	1
	D20.2	12
	D20.7	1
	D11.5	2

Supply Noise Pattern

The Jitter Group Technical Report Revision 10, June 9, 1999, defines this pattern. A D31.3 pattern is sent constantly.

8.9.2 Custom Pattern

The CUSTOM Pattern sent by the Pattern Generator is specified using Registers 0x110 through 0x128. When this CUSTOM Pattern is selected for generation, the Pattern Generator sends out the pattern whose data is taken from these Registers, and is formatted as shown in Figure 18. The order in which the bits are transmitted is shown in Figure 19.

The first four words sent out are the IDLE pattern, specified by the CUSTOM Pattern Idle Registers 1 through 4. These four words are then repeated for a total of N times where N is specified in binary by bits [6:0] of the CUSTOM Pattern Control Register. Once the IDLE Pattern has been sent, the Pattern Generator sends out the contents of CUSTOM Pattern SOF Registers 1 through 4. This is followed by sending out the contents of the CUSTOM Pattern DATA1 and DATA2 registers 1 through 4 consecutively. This entire sequence of eight words (four from DATA1 and four from DATA2) is repeated for a total of M times where M is specified in binary by bits [15:7] of the CUSTOM Pattern Control Register.

Once the data words have been sent, the Pattern Generator sends out the contents of the CUSTOM Pattern CRC Registers 1 through 4, followed by the contents of the CUSTOM Pattern EOF Registers 1 through 4.

This entire sequence (starting from the sending of IDLE pattern and ending with the sending of the EOF pattern) is repeated indefinitely, as long as the CUSTOM Pattern mode is selected.

Figure 18 Custom Frame Format

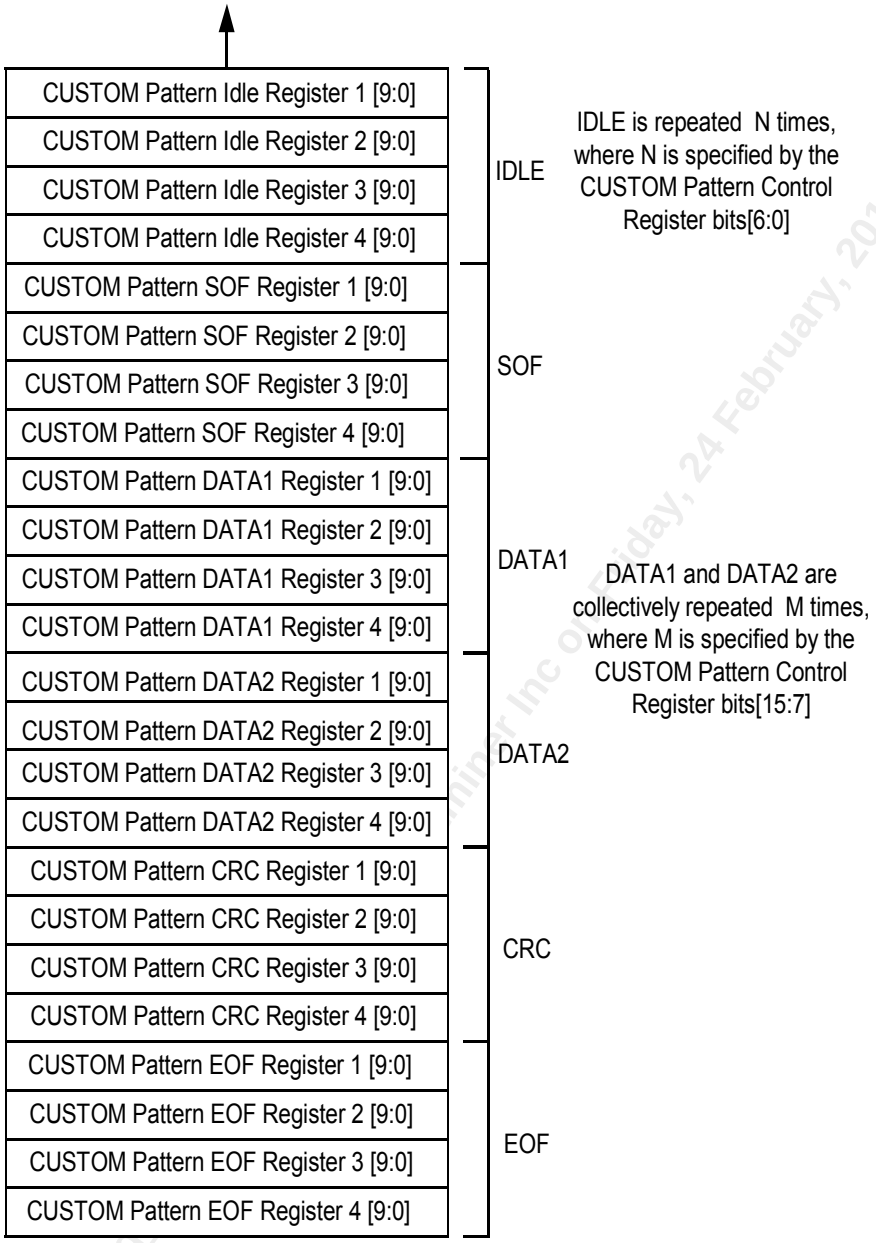
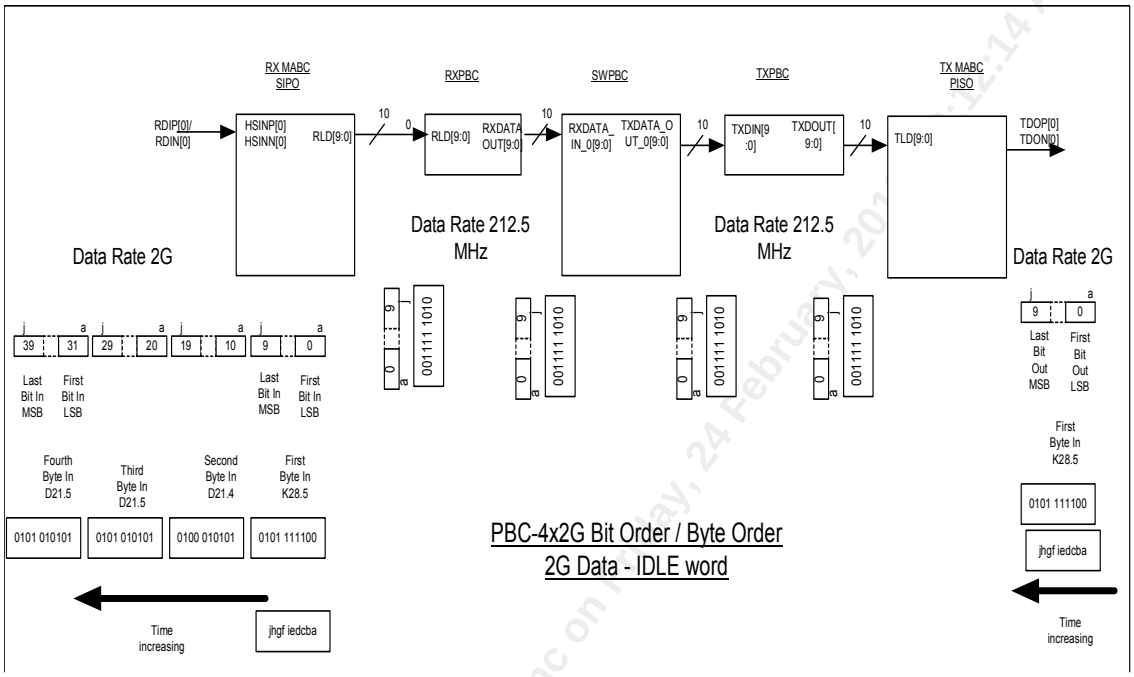


Figure 19 BIT Order/Byte Order 2G Data



8.9.3 Pattern Comparator

The Pattern Comparator is used to compare two of the seven patterns sent out by the Pattern Generator.

The Pattern Comparator is capable of comparing either the Compliant Receive Jitter Tolerance Pattern (CJTPAT), or the CUSTOM Pattern. This is selected by the same bits that select the patterns for the Pattern Generator (bits [2:0] of the Pattern Generator/Comparator Control Register).

When the Pattern Comparator is selected for comparison of the CJTPAT pattern, it only compares the contents of the CJTPAT from the SOF to the EOF of a pattern when the Check_Idles bit in the Pattern Generator/Comparator Control Register to logic 0. Any errors that are observed between the SOF and EOF are recorded by incrementing the Pattern Comparator Error Count Register. The number of SOFs and EOFs received are also counted using the Pattern Comparator SOF Count Register and the Pattern Comparator EOF Count Register respectively. When the Pattern Comparator is selected for comparison of the CJTPAT Pattern, it is capable of checking for the IDLE pattern as well by setting the Check_Idles bit in the Pattern Generator/Comparator Control Register to logic 1.

When the Pattern Comparator is selected for comparison of the CUSTOM Pattern, it is capable of checking for the IDLE pattern as well. The IDLE patterns may be checked by setting the Check_Idles bit in the Pattern Generator/Comparator Control Register to logic 1. If this bit is not set, then the Pattern Comparator only compares the CUSTOM Pattern from the SOF to the EOF. Any errors that are observed between the SOF and EOF are recorded by incrementing the Pattern Comparator Error Count Register. The number of SOFs and EOFs received are also counted using the Pattern Comparator SOF Count Register and the Pattern Comparator EOF Count Register respectively.

8.9.4 BIST Mode

The BIST Mode of operation of the Pattern Generator and the Pattern Comparator is selected when the BIST_EN bit in the Pattern Generator/Comparator Control Register is set to logic 1. For correct operation of this mode, the Type bits should either be set to 010 or 110, as the comparator is only capable of comparing these two patterns. All the Transmit ports are connected to the Pattern Generator's output data. The Comparator port is initially connected to the receive path of port 0.

The Pattern Generator sends out continuous patterns up to a maximum of 10 max size Frames. The Pattern comparator synchronizes to the incoming data by looking for an SOF character in the data stream of port 0. Once it has achieved synchronization, it looks for errors within the given Pattern. If the Pattern had an error, the BIST PORT STATUS Register for Port 0 is set to logic 1, indicating that a failure had been observed on port 0. It then continues to check for SOFs and for errors in the Patterns that follow.

The counter in the Pattern generator eventually reaches the maximum count and gives a timeout signal to the Pattern comparator. When this happens, Pattern comparator now switches its input data to the receive data of port 1. The counter resets itself and starts counting again. The Pattern comparator synchronizes to the incoming data by looking for an SOF character in the data stream of port 1. If an error was found within the Pattern, the BIST PORT STATUS Register for Port 1 is set to logic 1.

This process is repeated until all 4 ports have been tested and the BIST DONE Interrupt bit is set to logic 1. The user can now read the BIST status of all the ports using the BIST PORT STATUS Registers. The Pattern Generator and Comparator are disabled when BIST_EN is set to logic 0. To rerun, the user must set BIST_EN to logic 0 and again to logic 1. When the BIST_EN bit is set back to logic 1, the BIST PORT STATUS Register are all set to a logic 0.

8.10 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The QuadPHY RT identification code is 0x083720CD.

8.10.1 JTAG Support

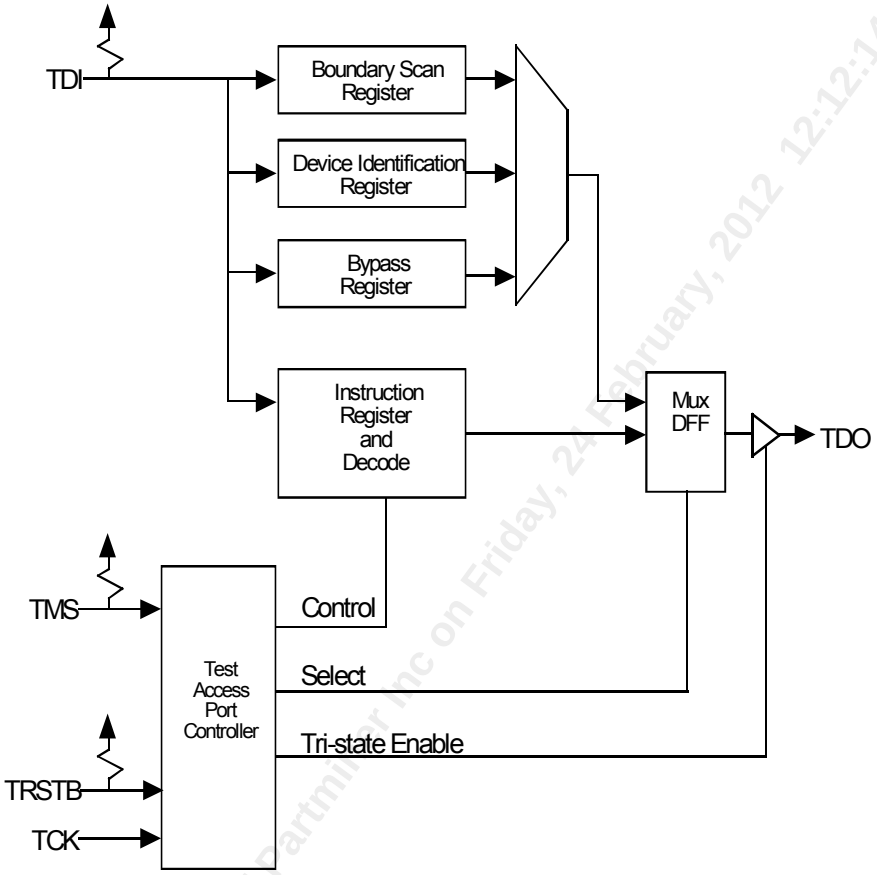
The QuadPHY RT supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins: TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 20.

The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register, and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

JTAG is not supported for the high-speed receive and transmit buffers.

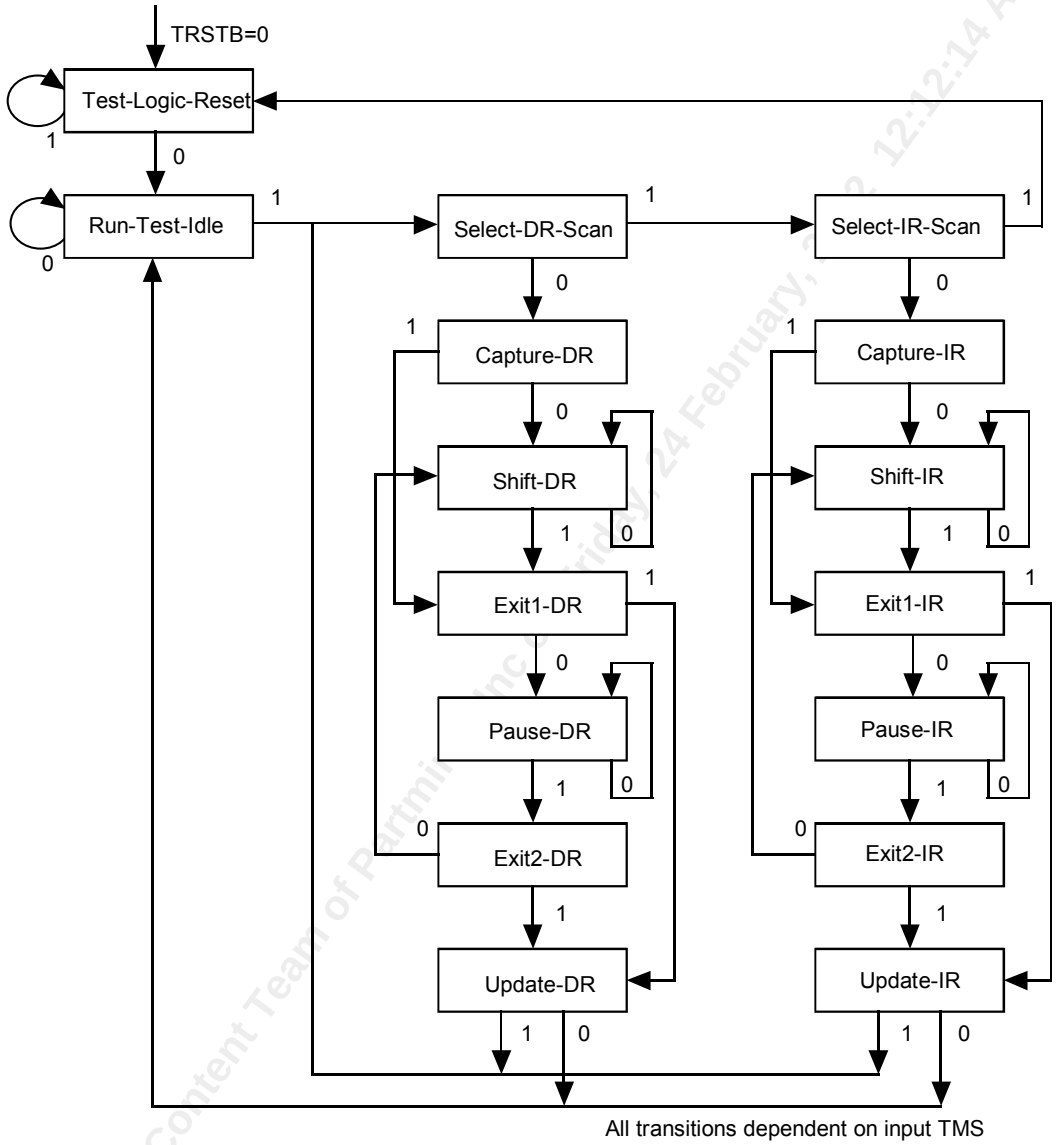
Figure 20 Boundary Scan Architecture



8.10.2 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is shown if Figure 21.

Figure 21 TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

8.10.3 Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

9 Normal Mode Register Description

The registers are used to configure and monitor the operation of the QuadPHY RT and are accessed via the MDC/MDIO management interface or when the TWISEL pin is set to logic 1, the registers are accessed via the two-wire interface.

9.1 Register Memory Map

Table 20 Register Memory Map

Address	Description
Register 0x000	ID
Register 0x001	Revision
Register 0x002	Global Control
Register 0x003	Frame Clk
Register 0x004	Pre-emphasis Control
Register 0x005	High Speed Amplitude Control
Register 0x006	Input Equalization/Loss Level Control
Register 0x007	Unused Port Power Down/ External Cap Control
Register 0x008	Rate Detect State Machine tsync Threshold Values
Register 0x009	Rate Detect State Machine tfail Threshold Values
Register 0x00A	DLOL INTRB Masks
Register 0x00B	LCV Threshold
Register 0x00C	CRC32 Threshold
Register 0x00D	Clear Error Counters
Register 0x00E	Unused
Register 0x00F	Unused
Register 0x010	Retimer and Monitor Configuration Port 0
Register 0x011	Retimer and Monitor Status Port 0
Register 0x012	Retimer and Monitor LCV Error Count Port 0
Register 0x013	Retimer and Monitor CRC Error Count Port 0
Register 0x014	Reserved
Register 0x015	Reserved
Register 0x016	Reserved
Register 0x017	Reserved
Register 0x018	Reserved
Register 0x019	Reserved
Register 0x01A – Register 0x01F	Unused
Register 0x020	Retimer and Monitor Configuration Port 1
Register 0x021	Retimer and Monitor Status Port 1
Register 0x022	Retimer and Monitor LCV Error Count Port 1

Register 0x023	Retimer and Monitor CRC Error Count Port 1
Register 0x024	Reserved
Register 0x025	Reserved
Register 0x026	Reserved
Register 0x027	Reserved
Register 0x028	Reserved
Register 0x029	Reserved
Register 0x02A – Register 0x02F	Unused
Register 0x030	Retimer and Monitor Configuration Port 2
Register 0x031	Retimer and Monitor Status Port 2
Register 0x032	Retimer and Monitor LCV Error Count Port 2
Register 0x033	Retimer and Monitor CRC Error Count Port 2
Register 0x034	Reserved
Register 0x035	Reserved
Register 0x036	Reserved
Register 0x037	Reserved
Register 0x038	Reserved
Register 0x039	Reserved
Register 0x03A – Register 0x03F	Unused
Register 0x040	Retimer and Monitor Configuration Port 3
Register 0x041	Retimer and Monitor Status Port 3
Register 0x042	Retimer and Monitor LCV Error Count Port 3
Register 0x043	Retimer and Monitor CRC Error Count Port 3
Register 0x044	Reserved
Register 0x045	Reserved
Register 0x046	Reserved
Register 0x047	Reserved
Register 0x048	Reserved
Register 0x049	Reserved
Register 0x04A – Register 0x0FF	Unused
Register 0x100	Cross connect Control Register
Register 0x101	FC Rate Status Register
Register 0x102	Reserved
Register 0x103	Reserved
Register 0x104	Reserved
Register 0x105	Reserved
Register 0x106	Retimer Connection Map Register
Register 0x107	Reserved
Register 0x108	Reserved

Register 0x109	Interrupt Enable Register
Register 0x10A	Interrupt Status Register
Register 0x10B	Port Status Register
Register 0x10C	Reserved
Register 0x10D	Reserved
Register 0x10E	Reserved
Register 0x10F	Pattern Generator/Comparator Control Register
Register 0x110	Custom Pattern Control Register 1
Register 0x111	Custom Pattern SOF Register 1
Register 0x112	Custom Pattern SOF Register 2
Register 0x113	Custom Pattern SOF Register 3
Register 0x114	Custom Pattern SOF Register 4
Register 0x115	Custom Pattern DATA1 Register 1
Register 0x116	Custom Pattern DATA1 Register 2
Register 0x117	Custom Pattern DATA1 Register 3
Register 0x118	Custom Pattern DATA1 Register 4
Register 0x119	Custom Pattern DATA2 Register 1
Register 0x11A	Custom Pattern DATA2 Register 2
Register 0x11B	Custom Pattern DATA2 Register 3
Register 0x11C	Custom Pattern DATA2 Register 4
Register 0x11D	Custom Pattern CRC Register 1
Register 0x11E	Custom Pattern CRC Register 2
Register 0x11F	Custom Pattern CRC Register 3
Register 0x120	Custom Pattern CRC Register 4
Register 0x121	Custom Pattern EOF Register 1
Register 0x122	Custom Pattern EOF Register 2
Register 0x123	Custom Pattern EOF Register 3
Register 0x124	Custom Pattern EOF Register 4
Register 0x125	Custom Pattern Idle Register 1
Register 0x126	Custom Pattern Idle Register 2
Register 0x127	Custom Pattern Idle Register 3
Register 0x128	Custom Pattern Idle Register 4
Register 0x129	Pattern Comparator SOF Count Register
Register 0x12A	Pattern Comparator EOF Count Register
Register 0x12B	Pattern Comparator Error Count Register
Register 0x12C	BIST Status Register
Register 0x12D	BIST Interrupt Enable Register
Register 0x12E	BIST Done Interrupt Status Register
Register 0x12F– Register 0x1DF	Unused
Register 0x1E0	Reserved
Register 0x1E1	Reserved

Register 0x1E2	Reserved
Register 0x1E3	Reserved
Register 0x1E4	Reserved
Register 0x1E5	Reserved
Register 0x1E6	Reserved
Register 0x1E7	Reserved
Register 0x1E8	Reserved
Register 0x1E9	Reserved
Register 0x1EA	Reserved
Register 0x1EB	Reserved
Register 0x1EC– Register 0x1FF	Unused

9.2 Registers

9.2.1 Device ID Registers

Register 0x000: ID

Bit	Type	Function	Default
15	R	Device ID [15]	1
14	R	Device ID [14]	0
13	R	Device ID [13]	0
12	R	Device ID [12]	0
11	R	Device ID [11]	0
10	R	Device ID [10]	0
9	R	Device ID [9]	1
8	R	Device ID [8]	1
7	R	Device ID [7]	0
6	R	Device ID [6]	1
5	R	Device ID [5]	1
4	R	Device ID [4]	1
3	R	Device ID [3]	0
2	R	Device ID [2]	0
1	R	Device ID [1]	1
0	R	Device ID [0]	0

DeviceId [15:0]

This holds the device ID.

Register 0x001: Revision

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	Reserved	0
3	R	Version [3]	0
2	R	Version [2]	0
1	R	Version [1]	0
0	R	Version [0]	0

Version [3:0]

This field contains the revision number for the part. The initial revision is 0x00. It is incremented for every subsequent mask revision.

9.2.2 Global Control Registers

Register 0x002: Global Control

Bit	Type	Function	Default
15	R/W	Global_Reset	0
14	R/W	Global_Soft_Reset	0
13	R/W	Halfrate Port [3]	0
12	R/W	Halfrate Port [2]	0
11	R/W	Halfrate Port [1]	0
10	R/W	Halfrate Port [0]	0
9	R/W	Cont_alignment	1
8	R/W	Halfrate Control	0
7	R/W	Reserved	0
6	R/W	Autorate_Override	0
5	R/W	EXTCAP Control	0
4	R/W	Pre-emphasis Control	0
3	R/W	Equalization Control	0
2	R/W	DLOLB filter [2]	0
1	R/W	DLOLB filter [1]	1
0	R/W	DLOLB filter [0]	0

Global_Reset

Setting this bit to logic 1 resets all the ports in the QuadPHY RT. This action sets the status and control registers to their default states. As a consequence, this action changes the internal states of the QuadPHY RT. The QuadPHY RT is not required to accept a write transaction to the control register until logic 0 is written back to this register bit. Writes to bits of the control register other than bit 15 will have no effect until the reset process is completed.

Global_Soft_Reset

Setting this bit to logic 1 resets all of the state machines for all ports in the QuadPHY RT. This action does not change the status and control registers of any ports. Register settings are not affected but all FIFOs are cleared. Global Soft Reset will reset the active map of the crossbar to the default and the 'Load Standby Reg' bit must be written with a logic 1 in order to reload the map.

Halfrate Port [3:0]

When AUTO_RATE_SEL pin is set to logic 0 and the Halfrate Control register is set to logic 1, these bits control the rate of operation of each corresponding port. When set to logic 1, the corresponding port will run at 1.0625 / 1.25 Gbit/s. When set to logic 0, the corresponding port will run at 2.125 Gbit/s.

Cont_alignment

Setting this bit to logic 1 continuously adjusts the current byte boundary whenever a comma is detected. When this bit is set to logic 0, the byte boundary can only be adjusted whenever the word synch state machine determines loss of synch has occurred.

Halfrate Control

Setting this bit to logic 1 when AUTO_RATE_SEL is set to logic 0 allows the Halfrate Port registers to control the rate of operation on per-port basis. It masks the HALF_RATE pin from controlling the rate. Setting this bit to logic 0 when AUTO_RATE_SEL is set to logic 0 allows the HALF_RATE pin to control the rate of operation for all ports. Note that when AUTO_RATE_SEL is set to logic 1, the HALF_RATE pin and Halfrate Port registers will be ignored and the rate of operation of each port will be determined by the automatic rate detection logic (see Table 21).

Table 21 Rate Control

AUTO_ RATE_SEL (input pin)	Autorate_Override (Reg 0x002, bit 6)	Halfrate Control (Reg 0x002, bit 8)	HALF_RATE (input pin)	Halfrate Port (Reg 0x002, bits 13:10)	Rate of Operation
0	0	0	0	X	2.125 Gbit/s
0	0	0	1	X	1.0625 / 1.25 Gbit/s
0	0	1	X	0	2.125 Gbit/s
0	0	1	X	1	1.0625 / 1.25 Gbit/s
0	1	X	X	X	As Detected
1	0	X	X	X	As Detected
1	1	0	0	X	2.125 Gbit/s
1	1	0	1	X	1.0625 / 1.25 Gbit/s
1	1	1	X	0	2.125 Gbit/s
1	1	1	X	1	1.0625 / 1.25 Gbit/s

Autorate_Override

When this bit set to logic 1, the AUTO_RATE_SEL pin value will be inverted for use. When this bit is set to logic 0, the AUTO_RATE_SEL pin will control automatic rate detection as described in the pin description.

EXTCAP Control

Setting this bit to logic 1 allows the EXTCAP registers to control the AC-Coupling on per-port basis. It masks the pins from controlling the AC-Couple. Setting this bit to logic 0 allows the pins to control the AC-Coupling for all ports.

Pre-emphasis Control

Setting this bit to logic 1 allows the pre-emphasis registers to control the pre-emphasis level on per-port basis. It masks the pins from controlling the levels. Setting this bit to logic 0 allows the pins to control the pre-emphasis levels for all ports.

Equalization Control

Setting this bit to logic 1 allows the equalization registers to control the receive equalization level on per-port basis. It masks the pins from controlling the levels. Setting this bit to logic 0 allows the pins to control the input equalization levels for all ports.

DLOLB filter [2:0]

These bits determine the number of Frame Clk intervals to filter each PORT_DLOLB. Setting bits[2:0] in this register to logic 0 disables the generation of Frame Clk. For optimal operation, the default setting of 2 is recommended.

Table 22 DLOLB Filter Time Constant

Bits[2:0]	Time
000	0 Frame Clks
001	1 Frame Clks
010	2 Frame Clks
011	3 Frame Clks
100	4 Frame Clks
101	5 Frame Clks
110	6 Frame Clks
111	7 Frame Clks

Register 0x003: Frame Clk

Bit	Type	Function	Default
15	R/W	Frame Clk [15]	0
14	R/W	Frame Clk [14]	0
13	R/W	Frame Clk [13]	1
12	R/W	Frame Clk [12]	0
11	R/W	Frame Clk [11]	0
10	R/W	Frame Clk [10]	0
9	R/W	Frame Clk [9]	0
8	R/W	Frame Clk [8]	0
7	R/W	Frame Clk [7]	0
6	R/W	Frame Clk [6]	0
5	R/W	Frame Clk [5]	0
4	R/W	Frame Clk [4]	0
3	R/W	Frame Clk [3]	0
2	R/W	Frame Clk [2]	0
1	R/W	Frame Clk [1]	0
0	R/W	Frame Clk [0]	0

Frame Clk[15:0]

Setting these bits sets the frame clk period. The value in the field sets the period of the frame clock in units of 1/106.25 MHz. The register value is used to count down the number of clock periods. The recommended value for this register should be greater than the max frame size. Setting this register to 0x09 or less will disable frame clock generation. When Frame Clk is turned off, there will be no indication whether the port is receiving valid data and all error statuses should be ignored.

Register 0x004: Pre-emphasis Control

Bit	Type	Function	Default
15	-	Unused	0
14	-	Unused	0
13	-	Unused	0
12	-	Unused	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Pre-emphasis Port 2 [1]	0
6	R/W	Pre-emphasis Port 2 [0]	0
5	R/W	Pre-emphasis Port 1 [1]	0
4	R/W	Pre-emphasis Port 1 [0]	0
3	R/W	Pre-emphasis Port 0 [1]	0
2	R/W	Pre-emphasis Port 0 [0]	0
1	R/W	Pre-emphasis Port 3 [1]	0
0	R/W	Pre-emphasis Port 3 [0]	0

Pre-emphasis Port [1:0]

Setting the bits on **Error! Reference source not found.** determines the Pre-emphasis levels for the respective ports. Pre-emphasis is not supported in half rate mode. The amount of pre-emphasis is dictated by the following equation:

$a\text{-}bz^{-1}$, where the coefficients a and b are set :

Table 23 Typical Pre-emphasis Levels

Bits[1:0]	a	b	Pre-emphasis
00	1	0	0 dB (off)
01	0.875	0.125	2.5dB
10	0.75	0.25	6.0dB
11	0.667	0.333	9.5dB

Register 0x005: High Speed Amplitude Control

Bit	Type	Function	Default
15	-	Unused	0
14	-	Unused	0
13	-	Unused	0
12	-	Unused	0
11	-	Unused	0
10	-	Unused	0
9	-	Unused	0
8	-	Unused	0
7	R/W	HC Port 2 [1]	1
6	R/W	HC Port 2 [0]	0
5	R/W	HC Port 1 [1]	1
4	R/W	HC Port 1 [0]	0
3	R/W	HC Port 0 [1]	1
2	R/W	HC Port 0 [0]	0
1	R/W	HC Port 3 [1]	1
0	R/W	HC Port 3 [0]	0

HC Port [1:0]

Setting HC Port bits as in Table 24 sets the Amplitude levels for all High-speed outputs.

Table 24 High Speed Amplitude Control

HC Port [1:0]	Output Levels
00	Low Swing
01	Unused
10	High Swing
11	Mid Swing

Register 0x006: Input Equalization/Loss Level Control

Bit	Type	Function	Default
15	R/W	LOSLVL Port 3 [1]	0
14	R/W	LOSLVL Port 3 [0]	0
13	R/W	LOSLVL Port 2 [1]	0
12	R/W	LOSLVL Port 2 [0]	0
11	R/W	LOSLVL Port 1 [1]	0
10	R/W	LOSLVL Port 1 [0]	0
9	R/W	LOSLVL Port 0 [1]	0
8	R/W	LOSLVL Port 0 [0]	0
7	R/W	Input Equalization Port 3 [1]	1
6	R/W	Input Equalization Port 3 [0]	0
5	R/W	Input Equalization Port 2 [1]	1
4	R/W	Input Equalization Port 2 [0]	0
3	R/W	Input Equalization Port 1 [1]	1
2	R/W	Input Equalization Port 1 [0]	0
1	R/W	Input Equalization Port 0 [1]	1
0	R/W	Input Equalization Port 0 [0]	0

LOSLVL Port [1:0]

Setting the bits in Table 25 sets the loss of signal level for the corresponding port. LOSLVL Port selects the differential peak-peak voltage for Loss of Signal. LOS=1 if signal < min and LOS=0 if signal > max. Range between min and max is uncertainty region

Table 25 Loss of Signal levels

LOSLVL Port [1:0]	LOS range[1] [min, max]
00	[0, 330] mVppd
01	[50, 450] mVppd
10	[100, 475] mVppd
11	Reserved – do not use

Notes

1. These LOS thresholds apply to CJTPAT.

Input Equalization Port [1:0]

These bits set the input equalization per port. See Table 9 for the levels.

Table 26 Input Equalization

Input Equalization Port [1:0]	Equalization	Comments
00	Max Equalization	Both stages enabled
01	Moderate-equalization	Do Not Use.
10	Moderate Equalization	default
11	No Equalization	1st & 2nd Stage Eq-off

Register 0x007: Unused Port Power Down/ External Cap Control

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13	R/W	FORCE_LCV_IDLE	0
12	R/W	LCV_IDLE_CAUSE	0
11	R/W	EXTCAP Port [3]	0
10	R/W	EXTCAP Port [2]	0
9	R/W	EXTCAP Port [1]	0
8	R/W	EXTCAP Port [0]	0
7	R/W	Power down TX Port [2]	0
6	R/W	Power down TX Port [1]	0
5	R/W	Power down TX Port [0]	0
4	R/W	Power down TX Port [3]	0
3	R/W	Power down RX Port [3]	0
2	R/W	Power down RX Port [2]	0
1	R/W	Power down RX Port [1]	0
0	R/W	Power down RX Port [0]	0

FORCE_LCV_IDLE

When set to logic 1, idles with positive running disparity will be substituted for received data either when an analog signal is not detected at the receiver or when loss of synchronization has occurred as determined by the LCV_IDLE_CAUSE bit. When set to logic 0, the data received will be output even if analog signal is not detected or synchronization is lost.

LCV_IDLE_CAUSE

This bit selects the error that will cause idles with the wrong disparity to be substituted for received data when FORCE_LCV_IDLE is set to logic 1. When this bit is set to logic 1, loss of synchronization or analog signal not detected will cause the substitution. When set to logic 0, only analog signal not detected will cause the substitution. This bit is ignored when FORCE_LCV_IDLE is set to logic 0.

EXTCAP Port [3:0]

This register bit selects the use of external or internal coupling capacitors. When set to logic 1, an external coupling capacitor is required and a biasing 1V voltage is forced through the corresponding port. When set to logic 0, the internal coupling capacitor is used for the corresponding port.

Power down TX Port [3:0]

When any of these bits are set to logic 1, the corresponding ports' PISO and TX buffer will be disabled. When any of these bits are set to logic 0, the corresponding ports' TX buffer and PISO will be active.

Power down RX Port [3:0]

When any of these bits are set to logic 1, the corresponding ports' CDRU and RX buffer will be disabled. When any of these bits are set to logic 0, the corresponding ports' RX buffer and CDRU will be active.

Register 0x008: Rate Detect State Machine tsync Threshold Values

Bit	Type	Function	Default
15	R/W	TSYNC_TIMEOUT_THR [11]	0
14	R/W	TSYNC_TIMEOUT_THR [10]	0
13	R/W	TSYNC_TIMEOUT_THR [9]	1
12	R/W	TSYNC_TIMEOUT_THR [8]	1
11	R/W	TSYNC_TIMEOUT_THR [7]	1
10	R/W	TSYNC_TIMEOUT_THR [6]	1
9	R/W	TSYNC_TIMEOUT_THR [5]	1
8	R/W	TSYNC_TIMEOUT_THR [4]	0
7	R/W	TSYNC_TIMEOUT_THR [3]	1
6	R/W	TSYNC_TIMEOUT_THR [2]	0
5	R/W	TSYNC_TIMEOUT_THR [1]	0
4	R/W	TSYNC_TIMEOUT_THR [0]	0
3	R/W	TSYNC_MULTIPLIER [3]	0
2	R/W	TSYNC_MULTIPLIER [2]	0
1	R/W	TSYNC_MULTIPLIER [1]	0
0	R/W	TSYNC_MULTIPLIER [0]	0

TSYNC_TIMEOUT_THR [11:0]

TSYNC Timeout Threshold. These bits are the number of 4 byte words multiplied by $2^{TSYNC\_MULTIPLIER}$ allowed when waiting for word synchronization to be acquired before changing the rate. The default value is 1000 words.

TSYNC_MULTIPLIER[3:0]

TSYNC Multiplier. These bits represent the exponent x in the term 2^x that makes up the multiplier that is used to enable longer timeout thresholds. The timeout value for TSYNC would be TSYNC_TIMEOUT_THR * $2^{TSYNC\_MULTIPLIER}$ words. The default multiplier is 2^0.

Note the threshold word count value is based on a data rate of 2.125 GB/s. If the data rate of the traffic is 1.0625 GB/s, the threshold will actually be half the programmed value. The same amount of time will elapse in both cases.

Register 0x009: Rate Detect State Machine tfail Threshold Values

Bit	Type	Function	Default
15	R/W	TFAIL_TIMEOUT_THR [11]	0
14	R/W	TFAIL_TIMEOUT_THR [10]	0
13	R/W	TFAIL_TIMEOUT_THR [9]	1
12	R/W	TFAIL_TIMEOUT_THR [8]	1
11	R/W	TFAIL_TIMEOUT_THR [7]	1
10	R/W	TFAIL_TIMEOUT_THR [6]	1
9	R/W	TFAIL_TIMEOUT_THR [5]	1
8	R/W	TFAIL_TIMEOUT_THR [4]	0
7	R/W	TFAIL_TIMEOUT_THR [3]	1
6	R/W	TFAIL_TIMEOUT_THR [2]	0
5	R/W	TFAIL_TIMEOUT_THR [1]	0
4	R/W	TFAIL_TIMEOUT_THR [0]	0
3	R/W	TFAIL_MULTIPLIER [3]	0
2	R/W	TFAIL_MULTIPLIER [2]	0
1	R/W	TFAIL_MULTIPLIER [1]	0
0	R/W	TFAIL_MULTIPLIER [0]	0

TFAIL_TIMEOUT_THR [11:0]

TFAIL Timeout Threshold. These bits are the number of bytes multiplied by $2^{TFAIL\_MULTIPLIER}$ allowed when waiting for word synchronization to be acquired before changing the rate. The default value is 1000 bytes.

TFAIL_MULTIPLIER[3:0]

TFAIL Multiplier. These bits represent the exponent x in the term 2^x that makes up the multiplier that is used to enable longer timeout thresholds. The timeout value for TFAIL would be TFAIL_TIMEOUT_THR * $2^{TFAIL\_MULTIPLIER}$ bytes. The default multiplier is 2^0.

Note the threshold byte count value is based on a data rate of 2.125 GB/s. If the data rate of the traffic is 1.0625 GB/s, the threshold will actually be half the programmed value. The same amount of time will elapse in both cases.

Register 0x00A: DLOL INTRB Masks

Bit	Type	Function	Default
15	-	Unused	0
14	-	Unused	0
13	-	Unused	0
12	-	Unused	0
11	-	Unused	0
10	-	Unused	0
9	-	Unused	0
8	-	Unused	0
7	R/W	Mask INTRB	0
6	R/W	Mask ASD	0
5	R/W	Mask CDV	0
4	R/W	Mask LOS	0
3	R/W	Mask LCV Rate	0
2	R/W	Mask CRC32 Rate	0
1	R/W	Mask LCV Absolute	1
0	R/W	Mask CRC32 Absolute	1

Mask INTRB

When this bit is set to logic 1, all ports mask INTRB condition. When this bit is set to logic 0, all unmasked interrupt conditions assert INTRB.

Mask ASD

When this bit is set to logic 1, all ports mask the Analog Signal Detect condition to calculate DLOL and the corresponding error indication bit in the Retimer and Monitor Status register. When this bit is set to logic 0, the Analog Signal Detect condition is used to calculate DLOL and the status bit is unmasked.

Mask CDV

When this bit is set to logic 1, all ports mask the Comma Density violation to calculate DLOL and the corresponding error indication bit in Retimer and Monitor Status register. When this bit is set to logic 0, the Comma Density Violation condition is used to calculate DLOL and the status bit is unmasked. When the pin FC_GE_RET_SEL is set to 0, this bit is treated as 1 regardless of its' value.

Mask LOS

When this bit is set to logic 1, all ports mask the Loss of Synchronization to calculate DLOL and the corresponding error indication bit in Retimer and Monitor Status register. When this bit is set to logic 0, the Loss of Synchronization condition is used to calculate DLOL and the status bit is unmasked.

Mask LCV Rate

When this bit is set to logic 1, all ports mask the Line Code Violations and Disparity rate errors to calculate DLOL and the corresponding error indication bit in the Retimer and Monitor Status register. When this bit is set to logic 0, the Line Code Violations and Disparity error rates are used to calculate DLOL and the status bit is unmasked.

Mask CRC32 Rate

When this bit is set to logic 1, all ports mask CRC32 errors to calculate DLOL and the corresponding error indication bit in the Retimer and Monitor Status register. When this bit is set to logic 0, CRC32 rate errors are used to calculate DLOL and the status bit is unmasked. When the pin FC_GE_RET_SEL is set to 0, this bit is treated as 1 regardless of its value.

Mask LCV Absolute

When this bit is set to logic 1, all ports mask the Line Code Violations and Disparity errors to calculate DLOL and the corresponding error indication bit in the Retimer and Monitor Status register. When this bit is set to logic 0, the Line Code Violations and Disparity errors are used to calculate DLOL and the status bit is unmasked. When the pin FC_GE_RET_SEL is set to 0, this bit is treated as 1 regardless of its' value.

Mask CRC32 Absolute

When this bit is set to logic 1, all ports mask CRC32 errors to calculate DLOL and the corresponding error indication bit in the Retimer and Monitor Status register. When this bit is set to logic 0, CRC32 errors are used to calculate DLOL and the status bit is unmasked. When the pin FC_GE_RET_SEL is set to 0, this bit is treated as 1 regardless of its' value.

Register 0x00B: LCV Threshold

Bit	Type	Function	Default
15	R/W	LCV Threshold [15]	0
14	R/W	LCV Threshold [14]	0
13	R/W	LCV Threshold [13]	0
12	R/W	LCV Threshold [12]	0
11	R/W	LCV Threshold [11]	0
10	R/W	LCV Threshold [10]	0
9	R/W	LCV Threshold [9]	0
8	R/W	LCV Threshold [8]	0
7	R/W	LCV Threshold [7]	0
6	R/W	LCV Threshold [6]	0
5	R/W	LCV Threshold [5]	0
4	R/W	LCV Threshold [4]	0
3	R/W	LCV Threshold [3]	0
2	R/W	LCV Threshold [2]	0
1	R/W	LCV Threshold [1]	0
0	R/W	LCV Threshold [0]	0

LCV Threshold [15:0]

Setting these bits determines the threshold for Line Code Violations within a Frame Clk period. Bits [7:0] set the threshold for LCV rate counter. Bits [15:0] set the threshold for LCV absolute counter. The threshold value is the value represented by the register bits plus one. Setting all bits to be at logic 0 will cause internal error signal to set after the 1st error.

Register 0x00C: CRC32 Threshold

Bit	Type	Function	Default
15	R/W	CRC32 Threshold [15]	0
14	R/W	CRC32 Threshold [14]	0
13	R/W	CRC32 Threshold [13]	0
12	R/W	CRC32 Threshold [12]	0
11	R/W	CRC32 Threshold [11]	0
10	R/W	CRC32 Threshold [10]	0
9	R/W	CRC32 Threshold [9]	0
8	R/W	CRC32 Threshold [8]	0
7	R/W	CRC32 Threshold [7]	0
6	R/W	CRC32 Threshold [6]	0
5	R/W	CRC32 Threshold [5]	0
4	R/W	CRC32 Threshold [4]	0
3	R/W	CRC32 Threshold [3]	0
2	R/W	CRC32 Threshold [2]	0
1	R/W	CRC32 Threshold [1]	0
0	R/W	CRC32 Threshold [0]	0

CRC32 Threshold [15:0]

Setting these bits determines the threshold for CRC32 errors within a Frame Clk period. Bits [7:0] set the threshold for CRC32 rate counter. Bits [15:0] set the threshold for CRC32 absolute counter. The threshold value is the value represented by the register bits plus one. Setting all bits to be at logic 0 will cause internal error signal to set after the 1st error.

Register 0x00D: Clear Error Counters

Bit	Type	Function	Default
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	Reserved	0
5	R	Reserved	0
4	R	Reserved	0
3	R	Reserved	0
2	R	Reserved	0
1	R	Reserved	0
0	R	Clear Error Counters	0

Clear Error Counters

Writing any value to this register causes the values of all performance monitor counters to be latched into shadow registers, after which the performance monitor counters are cleared. The shadow registers can be read by the management interface. When this bit is read as logic 1, the transfer is in progress. When this bit is read as logic 0, the transfer has completed and the performance monitor counters have been cleared. Writing to this bit also updates the error status bits in the Retimer and Monitor Status register.

9.2.3 Receive Port Registers

Each receive port is configured using the 8 registers described in this section. The registers are listed once and apply to all 4 ports. The following table provides the starting and ending register address for each port.

Table 27 Receive Port Register Table

Port #	Start Addr	End Addr
0	010	017
1	020	027
2	030	037
3	040	047

Register 0x010, 0x020, 0x030, 0x040 : Retimer and Monitor Configuration

Bit	Type	Function	Default
15	R/W	GE FIFO Reset	0
14	R/W	FC FIFO Reset	0
13	-	Unused	0
12	-	Unused	0
11	-	Unused	0
10	-	Unused	0
9	-	Unused	0
8	R/W	Reserved	0
7	-	Unused	0
6	-	Unused	0
5	R/W	Overflow Mask	1
4	R/W	Underflow Mask	1
3	R/W	Reserved	1
2	R/W	Force Realign	0
1	R/W	Clear counters	0
0	R/W	Soft reset	0

GE FIFO Reset

Setting this bit to logic '1' holds the GE FIFO in reset. This bit is not self clearing. This bit should only be set to logic '1' in Fibre Channel mode. Setting this bit high is optional and will reduce power consumption.

FC FIFO Reset

Setting this bit to logic '1' holds the FC FIFO in reset. This bit is not self clearing. This bit should only be set to logic '1' in Gigabit Ethernet mode. Setting this bit high is optional and will reduce power consumption.

Overflow Mask

Setting this bit to logic 1 masks the FIFO overflow interrupt generation and its contribution to DLOL. The register status will be disabled and held at logic 0. When this bit is set to logic 0, the FIFO overflow condition is used to calculate DLOL and the status bit is unmasked.

Underflow Mask

Setting this bit to logic 1 masks the FIFO underflow interrupt generation and its contribution to DLOL. The register status will be disabled and held at logic 0. When this bit is set to logic 0, the FIFO underflow condition is used to calculate DLOL and the status bit is unmasked.

Force Realign

Setting this bit to logic 1 forces the byte alignment and word alignment blocks to realign.

Clear Counters

Setting this bit to logic 1 clears all the counters for the corresponding Receive monitor port to their reset values, and clears the error status bits in the Retimer and Monitor Status register as well. This bit also triggers the update of the shadow registers of the LCV and CRC absolute error counters. This bit must be written back to logic 0 after setting to 1.

Soft reset

Software Reset. Setting this bit to logic 1 resets the state machines and logic to their default values. Register values remain unchanged.

Register 0x011, 0x021, 0x031, 0x041 : Retimer and Monitor Status

Bit	Type	Function	Default
15	-	Unused	0
14	-	Unused	0
13	-	Unused	0
12	-	Unused	0
11	-	Unused	0
10	-	Unused	0
9	R	DLOL	0
8	R	ASD Error	0
7	R	Underflow Error	0
6	R	Overflow Error	0
5	R	CDV Error	0
4	R	CRC Abs Error	0
3	R	CRC Rate Error	0
2	R	LCV Abs Error	0
1	R	LCV Rate Error	0
0	R	Loss of Sync	0

DLOL

When this bit is logic 1 it indicates that a Digital Loss of Link signal has been generated. This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

ASD Error

When this bit is logic 1 it indicates that an analog loss of signal has been continuously detected for one Frame Clk period. This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

Underflow Error

When this bit is logic 1 it indicates that a FIFO underflow has occurred. This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

Overflow Error

When this bit is logic 1 it indicates that a FIFO overflow has occurred. This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

CDV Error

When this bit is logic 1 it indicates that a comma character was not detected within a Frame Clk period. This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

CRC Abs Error

When this bit is logic 1 it indicates that the CRC absolute error counter has exceeded its threshold (CRC_THRESHOLD[15:0]). This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

CRC Rate Error

When this bit is logic 1 it indicates that the CRC rate error counter has exceeded its threshold (CRC_THRESHOLD[7:0]) within a Frame Clk period. This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

LCV Abs Error

When this bit is logic 1 it indicates that the LCV absolute error counter has exceeded its threshold (LCV_THRESHOLD[15:0]). This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

LCV Rate Error

When this bit is logic 1 it indicates that the LCV rate error counter has exceeded its threshold (LCV_THRESHOLD[7:0]) within a Frame Clk period. This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

Loss of Sync

When this bit is logic 1 it indicates that the word synchronization state machine has lost sync at least once in a Frame Clk period. This bit clears upon writing a 1 to the Clear Counters bit in the respective Retimer and Monitor Configuration Register. To update this bit, a 1 must be written to the Clear Error Counters bit in the Clear Error Counters Register.

Register 0x012, 0x022, 0x032, 0x042: Retimer and Monitor LCV Error Count

Bit	Type	Function	Default
15	R	LCV Error Count [15]	0
14	R	LCV Error Count [14]	0
13	R	LCV Error Count [13]	0
12	R	LCV Error Count [12]	0
11	R	LCV Error Count [11]	0
10	R	LCV Error Count [10]	0
9	R	LCV Error Count [9]	0
8	R	LCV Error Count [8]	0
7	R	LCV Error Count [7]	0
6	R	LCV Error Count [6]	0
5	R	LCV Error Count [5]	0
4	R	LCV Error Count [4]	0
3	R	LCV Error Count [3]	0
2	R	LCV Error Count [2]	0
1	R	LCV Error Count [1]	0
0	R	LCV Error Count [0]	0

LCV Error Count [15:0]

This register is a shadow of the 16-bit absolute LCV error counter. It counts all the line code violations/disparity errors detected by the 8B/10B decoder. The counter associated with this register can be cleared by writing the Clear Counters bit for the corresponding port or by writing to the global Clear Error Counters bit. The counter saturates at 0xFFFF. This counter is disabled when DLOLBYP_MASK pin is set to logic 1.

Register 0x013, 0x023, 0x033, 0x043 : Retimer and Monitor CRC Error Count

Bit	Type	Function	Default
15	R	CRC Error Count [15]	0
14	R	CRC Error Count [14]	0
13	R	CRC Error Count [13]	0
12	R	CRC Error Count [12]	0
11	R	CRC Error Count [11]	0
10	R	CRC Error Count [10]	0
9	R	CRC Error Count [9]	0
8	R	CRC Error Count [8]	0
7	R	CRC Error Count [7]	0
6	R	CRC Error Count [6]	0
5	R	CRC Error Count [5]	0
4	R	CRC Error Count [4]	0
3	R	CRC Error Count [3]	0
2	R	CRC Error Count [2]	0
1	R	CRC Error Count [1]	0
0	R	CRC Error Count [0]	0

CRC Error Count [15:0]

This register is a shadow of the 16-bit absolute CRC error counter. It counts all the CRC32 errors detected by the CRC checker. The counter associated with this register may be cleared by writing the Clear Counters bit for the corresponding port or by writing to the global Clear Error Counters bit. The counter saturates at 0xFFFF. This counter is disabled when DLOLBYP_MASK pin is set to logic 1.

9.2.4 Cross connect Configuration Registers

The following registers are used to manually configure the cross connect in QuadPHY RT.

Register 0x100: Cross Connect Control Register

Bit	Type	Function	Default
15	R/W	SOFT_RESET	0
14	R/W	Reserved	0
13	R/W	Reserved	0
12	R/W	Reserved	0
11	R/W	Reserved	0
10	R/W	Reserved	0
9	R/W	Reserved	0
8	R/W	Reserved	0
7	R/W	Reserved	1
6	R/W	Reserved	1
5	R/W	Reserved	1
4	R/W	Reserved	1
3	R/W	Reserved	1
2	R/W	Reserved	1
1	R/W	Reserved	0
0	R/W	Reserved	0

SOFT_RESET

When this bit is set to logic 1, all state machines and counters are reset. When this bit is set to logic 0, the state machines are released from the reset state. This bit does not affect the state of the crossbar configuration registers.

Register 0x101: FC Rate Status Register

Bit	Type	Function	Default
15	-	Unused	0
14	-	Unused	0
13	-	Unused	0
12	-	Unused	0
11	-	Unused	0
10	-	Unused	0
9	-	Unused	0
8	-	Unused	0
7	R	FC Rate Valid [3]	X
6	R	FC Rate Valid [2]	X
5	R	FC Rate Valid [1]	X
4	R	FC Rate Valid [0]	X
3	R	FC Rate Status [3]	X
2	R	FC Rate Status [2]	X
1	R	FC Rate Status [1]	X
0	R	FC Rate Status [0]	X

FC Rate Valid [3:0]

The FC Rate Valid bits indicates the validity of FC Rate Status bits. When a bit is set to logic 1, the corresponding FC Rate Status bit is indicating a valid Fibre Channel rate. When a bit is set to logic 0, the corresponding FC Rate Status bit is not valid. The 1G/2G rate detection logic upstream of the SWPBC_4 TSB has not detected a valid rate.

FC Rate Status [3:0]

FC Rate Status [3:0]The FC Rate Status bits reflect the rate to which the rate detection state machine is trying to sync. This value is the Fibre Channel rate detected by the 1G/2G rate detection logic upstream of the SWPBC_4 TSB on the corresponding port. When a bit is set to logic 1, the rate detected is 1.0625 Gbit/s. When a bit is set to logic 0, the rate detected is 2.125 Gbit/s.

Register 0x106: Retimer Mode Connection Map Register

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11	R/W	Retimer Port 2 [2]	0
10	R/W	Retimer Port 2 [1]	1
9	R/W	Retimer Port 2 [0]	0
8	R/W	Retimer Port 1 [2]	0
7	R/W	Retimer Port 1 [1]	0
6	R/W	Retimer Port 1 [0]	1
5	R/W	Retimer Port 0 [2]	0
4	R/W	Retimer Port 0 [1]	0
3	R/W	Retimer Port 0 [0]	0
2	R/W	Retimer Port 3 [2]	0
1	R/W	Retimer Port 3 [1]	1
0	R/W	Retimer Port 3 [0]	1

Retimer Port 3 [2:0]

The three bits of this register (MSB is bit 2) hold a binary value representative of the port whose output is connected to the Transmit path of Port 3 when the TSB is in Retimer mode. The default value of this register is 3, which implies that the Receive of Port 3 is connected via the retimer to Port 3. This value can be re-programmed to any valid port number from 0 through 4, where port 4 connects to the Pattern Generator. If the value programmed exceeds 4, then the crossbar logic will override it, connecting the Transmit path of Port 3 to the Receive of Port 0.

Retimer Port 2 [2:0]

The three bits of this register (MSB is bit 11) hold a binary value representative of the port whose output is connected to the Transmit path of Port 2 when the TSB is in Retimer Mode. The default value of this register is 2, which implies that the Receive of Port 2 is connected via the retimer to Port 2. This value can be re-programmed to any valid port number from 0 through 4, where port 4 connects to the Pattern Generator. If the value programmed exceeds 4, then the crossbar logic will override it, connecting the Transmit path of Port 2 to the Receive of Port 0.

Retimer Port 1 [2:0]

The three bits of this register (MSB is bit 8) hold a binary value representative of the port whose output is connected to the Transmit path of Port 1 when the TSB is in mode. The default value of this register is 1, which implies that the Receive of Port 1 is connected via the retimer to Port 1. This value can be re-programmed to any valid port number from 0 through 4, where port 4 connects to the Pattern Generator. If the value programmed exceeds 4, then the crossbar logic will override it, connecting the Transmit path of Port 1 to the Receive of Port 0.

Retimer Port 0 [2:0]

The three bits of this register (MSB is bit 5) hold a binary value representative of the port whose output is connected to the Transmit path of Port 0 when the TSB is in mode. The default value of this register is 0, which implies that the Receive of Port 0 is connected via the retimer to Port 0. This value can be re-programmed to any valid port number from 0 through 4, where port 4 connects to the Pattern Generator. If the value programmed exceeds 4, then the crossbar logic will override it, connecting the Transmit path of Port 0 to the Receive of Port 0.

9.2.5 Interrupt Enable and Status Registers

These registers are used to enable the interrupts based on DLOLB generation. Each condition can be enabled per port. When enabled, the INTRB pin will assert if the interrupt conditions are valid. If the INTRB pin is masked, the status registers for each condition will update.

Register 0x109: Interrupt Enable Register

Bit	Type	Function	Default
15	RW	FC Rate Int En [3]	0
14	RW	FC Rate Int En [2]	0
13	RW	FC Rate Int En [1]	0
12	RW	FC Rate Int En [0]	0
11	R/W	DLOLB Int En [3]	0
10	R/W	DLOLB Int En [2]	0
9	R/W	DLOLB Int En [1]	0
8	R/W	DLOLB Int En [0]	0
7	R/W	Reserved	0
6	R/W	Reserved	0
5	R/W	Reserved	0
4	R/W	Reserved	0
3	R/W	Reserved	0
2	R/W	Reserved	0
1	R/W	Reserved	0
0	R/W	Reserved	0

FC Rate Int En [3:0]

When a bit of this register is set to logic 1, the assertion of the corresponding port's FC Rate Interrupt will cause the INTRB output pin to be asserted. When a bit of this register is set to logic 0, the assertion of the corresponding port's FC Rate Interrupt will not cause the INTRB output pin to be asserted. These bits however, do not affect the FC Rate Status Registers of the corresponding ports from updating themselves.

DLOLB Int En [3:0]

When a bit of this register is set to logic 1, the assertion of the corresponding port's DLOLB Interrupt will cause the INTRB output pin to be asserted. When a bit of this register is set to logic 0, the assertion of the corresponding port's DLOLB Interrupt will not cause the INTRB output pin to be asserted. These bits however, do not affect the DLOLB Status Registers of the corresponding ports from updating themselves.

Register 0x10A: Interrupt Status Register

Bit	Type	Function	Default
15	R	FC Rate Int Status [3]	X
14	R	FC Rate Int Status [2]	X
13	R	FC Rate Int Status [1]	X
12	R	FC Rate Int Status [0]	X
11	R	DLOLB Int Status [3]	X
10	R	DLOLB Int Status [2]	X
9	R	DLOLB Int Status [1]	X
8	R	DLOLB Int Status [0]	X
7	R	Reserved	X
6	R	Reserved	X
5	R	Reserved	X
4	R	Reserved	X
3	R	Reserved	X
2	R	Reserved	X
1	R	Reserved	X
0	R	Reserved	X

FC Rate Int Status [3:0]

When a bit of this register is set to logic 1, it indicates that the corresponding port had a transition in its detected FC rate. All bits of this register clear to logic 0 when the register is read.

DLOLB Int Status [3:0]

When a bit of this register is set to logic 1, it indicates that the corresponding port had a transition in the post-masked DLOLB. All bits of this register clear to logic 0 when the register is read.

9.2.6 Port Status Registers

These registers are for status of the ports. If any of the DLOLB bits in the register are set, the corresponding port is bypassed.

Register 0x10B: Port Status Register

Bit	Type	Function	Default
15	R	Unused	X
14	R	DLOLB Status 3	X
13	R	Reserved	X
12	R	Reserved	X
11	R	Unused	X
10	R	DLOLB Status 2	X
9	R	Reserved	X
8	R	Reserved	X
7	R	Unused	X
6	R	DLOLB Status 1	X
5	R	Reserved	X
4	R	Reserved	X
3	R	Unused	X
2	R	DLOLB Status 0	X
1	R	Reserved	X
0	R	Reserved	X

DLOLB Status 3

This bit reflects the current value of the PORT_DLOLB signal for port 3, post-masking.

DLOLB Status 2

This bit reflects the current value of the PORT_DLOLB signal for port 2, post-masking.

DLOLB Status 1

This bit reflects the current value of the PORT_DLOLB signal for port 1, post-masking.

DLOLB Status 0

This bit reflects the current value of the PORT_DLOLB signal for port 0, post-masking.

9.2.7 Pattern Generator Comparator

Register 0x10F: Pattern Generator/Comparator Control Register 1

Bit	Type	Function	Default
15	R/W	Reserved	0
14	R/W	Gen Half Rate [2]	0
13	R/W	Gen Half Rate [1]	0
12	R/W	Gen Half Rate [0]	0
11	R/W	Gen Half Rate [3]	0
10	R/W	Comparator Port [2]	0
9	R/W	Comparator Port [1]	0
8	R/W	Comparator Port [0]	0
7	R/W	BIST_EN	0
6	R/W	Check_Idles	0
5	R/W	En Pattern Generator	0
4	R/W	En Pattern Comparator	0
3	R/W	Reserved	0
2	R/W	Test Pattern Type [2]	0
1	R/W	Test Pattern Type [1]	0
0	R/W	Test Pattern Type [0]	0

Gen Half Rate [3:0]

When Gen Half Rate bit is set to logic 1, the Packet Generator outputs data in Half Rate format for the corresponding port. Packet Generator outputs each 10-bit word of the selected test pattern across two 10-bit words by repeating each bit in the word. When the Crossbar is configured to connect transmit Port N to the Packet Generator (Port 4), the generator data is transmitted on Port N in the format indicated by the Gen Half Rate [N] bit. When the Comparator Port [2:0] bits are set to 4 to connect the data from the Packet Generator to the Packet Comparator, the format of the data is always controlled by Gen Half Rate [0].

Comparator Port [2:0]

The three bits of this register (MSB is bit 10) hold a binary value representative of the port whose output is connected to the input of the Pattern Comparator (Port 4) through the Retimer. The default value of this register is 0, which implies that the Receive of Port 0 is connected via the retimer to the Pattern Comparator. This value can be re-programmed to any valid port number from 0 through 4.

BIST_EN

The BIST_EN bit, when set to logic 1, enables both the pattern comparator and the pattern generator, and puts the QuadPHY RTQuadPHY RT is in self-test mode. The completion of a BIST cycle is indicated by the BIST Done Interrupt and the BIST Status [3:0] bits are updated to report the status of the self-test. The RET_MODE input pin should be set to logic 0 when BIST_EN is set high. When BIST_EN is set to logic 0, self-test mode is disabled.

Check_Idles

This bit works in conjunction with the Pattern Comparator. When this bit is set to logic 1, and the En Pattern Comparator bit is set to logic 1, the Pattern Comparator checks for Idles in between patterns. When the CUSTOM Pattern pattern type is selected using the Test Pattern Type[2:0] bits, the value of the Idles is programmed using the Custom Pattern Idle Registers. When this bit is set to logic 0, the Pattern Comparator does not look for Idle columns.

En Pattern Generator

Setting this bit to logic 1 enables the Pattern Generator. The Packet Generator must be enabled only after configuring all the pattern settings.

En Pattern Comparator

Setting this bit to logic to 1 enables the Pattern Comparator. The Packet Comparator must be enabled only after configuring all the pattern settings.

Test Pattern Type [2:0]

The Test Pattern Type holds a three-bit value that indicates the type of pattern that the Pattern Generator generates and the Pattern Comparator uses for comparison. The various patterns are summarized in Table 28.

Table 28 Test Pattern Types for Register 0x010F bits [2:0]

000	Compliant RPAT
001	Low Transition Density Pattern
010	Compliant Jitter Tolerance Pattern
011	Half Rate and Quarter Rate Pattern
100	Low Frequency Pattern
101	Supply Noise Pattern
110	Custom Pattern

Register 0x110: Custom Pattern Control Register

Bit	Type	Function	Default
15	R/W	Data Repeat [8]	0
14	R/W	Data Repeat [7]	0
13	R/W	Data Repeat [6]	1
12	R/W	Data Repeat [5]	0
11	R/W	Data Repeat [4]	0
10	R/W	Data Repeat [3]	0
9	R/W	Data Repeat [2]	0
8	R/W	Data Repeat [1]	0
7	R/W	Data Repeat [0]	0
6	R/W	Idle Repeat [6]	0
5	R/W	Idle Repeat [5]	0
4	R/W	Idle Repeat [4]	0
3	R/W	Idle Repeat [3]	0
2	R/W	Idle Repeat [2]	1
1	R/W	Idle Repeat [1]	1
0	R/W	Idle Repeat [0]	0

Data Repeat [8:0]

The nine bits of this register (MSB is bit 15) hold a binary value that represents the number of times the values held in the Custom Pattern DATA1 and Custom Pattern DATA2 Registers are repeated as a pair, when the Custom Pattern Type is selected when using the Pattern Generator/Comparator. Setting the bits to logic 0 is invalid.

Idle Repeat [6:0]

The seven bits of this register (MSB is bit 6) hold a binary value that represents the number of times the value held in the Custom Pattern Idle Registers are repeated, when the Custom Pattern Type is selected when using the Pattern Generator/Comparator. Setting the bits to logic 0 is invalid.

Register 0x111: Custom Pattern SOF Register 1

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	SOF Character 1 [9]	0
8	R/W	SOF Character 1 [8]	1
7	R/W	SOF Character 1 [7]	0
6	R/W	SOF Character 1 [6]	1
5	R/W	SOF Character 1 [5]	1
4	R/W	SOF Character 1 [4]	1
3	R/W	SOF Character 1 [3]	1
2	R/W	SOF Character 1 [2]	1
1	R/W	SOF Character 1 [1]	0
0	R/W	SOF Character 1 [0]	0

SOF Character 1 [9:0]

The SOF Character 1[9:0] bits form the first character of the SOF sent out for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x112: Custom Pattern SOF Register 2

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	SOF Character 2 [9]	0
8	R/W	SOF Character 2 [8]	1
7	R/W	SOF Character 2 [7]	0
6	R/W	SOF Character 2 [6]	1
5	R/W	SOF Character 2 [5]	0
4	R/W	SOF Character 2 [4]	1
3	R/W	SOF Character 2 [3]	0
2	R/W	SOF Character 2 [2]	1
1	R/W	SOF Character 2 [1]	0
0	R/W	SOF Character 2 [0]	1

SOF Character 2 [9:0]

The SOF Character 2[9:0] bits form the second character of the SOF sent out for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x113: Custom Pattern SOF Register 3

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	SOF Character 3 [9]	1
8	R/W	SOF Character 3 [8]	0
7	R/W	SOF Character 3 [7]	0
6	R/W	SOF Character 3 [6]	1
5	R/W	SOF Character 3 [5]	1
4	R/W	SOF Character 3 [4]	0
3	R/W	SOF Character 3 [3]	1
2	R/W	SOF Character 3 [2]	0
1	R/W	SOF Character 3 [1]	0
0	R/W	SOF Character 3 [0]	0

SOF Character 3 [9:0]

The SOF Character 3[9:0] bits form the third character of the SOF sent out for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x114: Custom Pattern SOF Register 4

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	SOF Character 4 [9]	1
8	R/W	SOF Character 4 [8]	0
7	R/W	SOF Character 4 [7]	0
6	R/W	SOF Character 4 [6]	1
5	R/W	SOF Character 4 [5]	0
4	R/W	SOF Character 4 [4]	1
3	R/W	SOF Character 4 [3]	0
2	R/W	SOF Character 4 [2]	1
1	R/W	SOF Character 4 [1]	1
0	R/W	SOF Character 4 [0]	1

SOF Character 4 [9:0]

The SOF Character 4[9:0] bits form the fourth and last character of the SOF sent out for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x115: Custom Pattern DATA1 Register 1

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	DATA1 Character 1 [9]	0
8	R/W	DATA1 Character 1 [8]	0
7	R/W	DATA1 Character 1 [7]	1
6	R/W	DATA1 Character 1 [6]	0
5	R/W	DATA1 Character 1 [5]	1
4	R/W	DATA1 Character 1 [4]	0
3	R/W	DATA1 Character 1 [3]	0
2	R/W	DATA1 Character 1 [2]	0
1	R/W	DATA1 Character 1 [1]	1
0	R/W	DATA1 Character 1 [0]	1

DATA1 Character 1 [9:0]

The DATA1 Character 1[9:0] bits form the first character of the DATA1 pattern sent out after the SOF pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x116: Custom Pattern DATA1 Register 2

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	DATA1 Character 2 [9]	0
8	R/W	DATA1 Character 2 [8]	0
7	R/W	DATA1 Character 2 [7]	1
6	R/W	DATA1 Character 2 [6]	0
5	R/W	DATA1 Character 2 [5]	1
4	R/W	DATA1 Character 2 [4]	0
3	R/W	DATA1 Character 2 [3]	1
2	R/W	DATA1 Character 2 [2]	1
1	R/W	DATA1 Character 2 [1]	0
0	R/W	DATA1 Character 2 [0]	1

DATA1 Character 2 [9:0]

The DATA1 Character 2 [9:0] bits form the second character of the DATA1 pattern sent out after the SOF pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x117: Custom Pattern DATA1 Register 3

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	DATA1 Character 3 [9]	0
8	R/W	DATA1 Character 3 [8]	0
7	R/W	DATA1 Character 3 [7]	1
6	R/W	DATA1 Character 3 [6]	0
5	R/W	DATA1 Character 3 [5]	1
4	R/W	DATA1 Character 3 [4]	0
3	R/W	DATA1 Character 3 [3]	1
2	R/W	DATA1 Character 3 [2]	1
1	R/W	DATA1 Character 3 [1]	1
0	R/W	DATA1 Character 3 [0]	0

DATA1 Character 3 [9:0]

The DATA1 Character 3[9:0] bits form the third character of the DATA1 pattern sent out after the SOF pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x118: Custom Pattern DATA1 Register 4

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	DATA1 Character 4 [9]	0
8	R/W	DATA1 Character 4 [8]	0
7	R/W	DATA1 Character 4 [7]	1
6	R/W	DATA1 Character 4 [6]	0
5	R/W	DATA1 Character 4 [5]	1
4	R/W	DATA1 Character 4 [4]	1
3	R/W	DATA1 Character 4 [3]	1
2	R/W	DATA1 Character 4 [2]	0
1	R/W	DATA1 Character 4 [1]	0
0	R/W	DATA1 Character 4 [0]	1

DATA1 Character 4 [9:0]

The DATA1 Character 4[9:0] bits form the fourth and final character of the DATA1 pattern sent out after the SOF pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x119: Custom Pattern DATA2 Register 1

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	DATA2 Character 1 [9]	0
8	R/W	DATA2 Character 1 [8]	0
7	R/W	DATA2 Character 1 [7]	1
6	R/W	DATA2 Character 1 [6]	0
5	R/W	DATA2 Character 1 [5]	1
4	R/W	DATA2 Character 1 [4]	1
3	R/W	DATA2 Character 1 [3]	1
2	R/W	DATA2 Character 1 [2]	0
1	R/W	DATA2 Character 1 [1]	0
0	R/W	DATA2 Character 1 [0]	1

DATA2 Character 1 [9:0]

The DATA2 Character 1[9:0] bits form the first character of the DATA2 pattern sent out after the DATA1 pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x11A: Custom Pattern DATA2 Register 2

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	DATA2 Character 2 [9]	0
8	R/W	DATA2 Character 2 [8]	0
7	R/W	DATA2 Character 2 [7]	1
6	R/W	DATA2 Character 2 [6]	0
5	R/W	DATA2 Character 2 [5]	1
4	R/W	DATA2 Character 2 [4]	0
3	R/W	DATA2 Character 2 [3]	1
2	R/W	DATA2 Character 2 [2]	1
1	R/W	DATA2 Character 2 [1]	1
0	R/W	DATA2 Character 2 [0]	0

DATA2 Character 2 [9:0]

The DATA2 Character 2[9:0] bits form the second character of the DATA2 pattern sent out after the DATA1 pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x11B: Custom Pattern DATA2 Register 3

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	DATA2 Character 3 [9]	0
8	R/W	DATA2 Character 3 [8]	0
7	R/W	DATA2 Character 3 [7]	1
6	R/W	DATA2 Character 3 [6]	0
5	R/W	DATA2 Character 3 [5]	1
4	R/W	DATA2 Character 3 [4]	0
3	R/W	DATA2 Character 3 [3]	1
2	R/W	DATA2 Character 3 [2]	1
1	R/W	DATA2 Character 3 [1]	0
0	R/W	DATA2 Character 3 [0]	1

DATA2 Character 3 [9:0]

The DATA2 Character 3[9:0] bits form the third character of the DATA2 pattern sent out after the DATA1 pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x11C: Custom Pattern DATA2 Register 4

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	DATA2 Character 4 [9]	1
8	R/W	DATA2 Character 4 [8]	1
7	R/W	DATA2 Character 4 [7]	0
6	R/W	DATA2 Character 4 [6]	1
5	R/W	DATA2 Character 4 [5]	1
4	R/W	DATA2 Character 4 [4]	0
3	R/W	DATA2 Character 4 [3]	0
2	R/W	DATA2 Character 4 [2]	0
1	R/W	DATA2 Character 4 [1]	1
0	R/W	DATA2 Character 4 [0]	1

DATA2 Character 4 [9:0]

The DATA2 Character 4[9:0] bits form the fourth and final character of the DATA2 pattern sent out after the DATA1 pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x11D: Custom Pattern CRC Register 1

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	CRC Character 1 [9]	0
8	R/W	CRC Character 1 [8]	1
7	R/W	CRC Character 1 [7]	0
6	R/W	CRC Character 1 [6]	1
5	R/W	CRC Character 1 [5]	1
4	R/W	CRC Character 1 [4]	0
3	R/W	CRC Character 1 [3]	0
2	R/W	CRC Character 1 [2]	0
1	R/W	CRC Character 1 [1]	0
0	R/W	CRC Character 1 [0]	1

CRC Character 1 [9:0]

The CRC Character 1[9:0] bits form the first character of the CRC pattern sent out after the DATA2 pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x11E: Custom Pattern CRC Register 2

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	CRC Character 2 [9]	1
8	R/W	CRC Character 2 [8]	0
7	R/W	CRC Character 2 [7]	0
6	R/W	CRC Character 2 [6]	1
5	R/W	CRC Character 2 [5]	0
4	R/W	CRC Character 2 [4]	1
3	R/W	CRC Character 2 [3]	0
2	R/W	CRC Character 2 [2]	1
1	R/W	CRC Character 2 [1]	1
0	R/W	CRC Character 2 [0]	1

CRC Character 2 [9:0]

The CRC Character 2[9:0] bits form the second character of the CRC pattern sent out after the DATA2 pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x11F: Custom Pattern CRC Register 3

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	CRC Character 3 [9]	0
8	R/W	CRC Character 3 [8]	1
7	R/W	CRC Character 3 [7]	0
6	R/W	CRC Character 3 [6]	1
5	R/W	CRC Character 3 [5]	1
4	R/W	CRC Character 3 [4]	0
3	R/W	CRC Character 3 [3]	0
2	R/W	CRC Character 3 [2]	1
1	R/W	CRC Character 3 [1]	0
0	R/W	CRC Character 3 [0]	0

CRC Character 3 [9:0]

The CRC Character 3[9:0] bits form the third character of the CRC pattern sent out after the DATA2 pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x120: Custom Pattern CRC Register 4

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	CRC Character 4 [9]	1
8	R/W	CRC Character 4 [8]	0
7	R/W	CRC Character 4 [7]	1
6	R/W	CRC Character 4 [6]	0
5	R/W	CRC Character 4 [5]	1
4	R/W	CRC Character 4 [4]	1
3	R/W	CRC Character 4 [3]	0
2	R/W	CRC Character 4 [2]	0
1	R/W	CRC Character 4 [1]	0
0	R/W	CRC Character 4 [0]	1

CRC Character 4 [9:0]

The CRC Character 4[9:0] bits form the fourth and final character of the CRC pattern sent out after the DATA2 pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x121: Custom Pattern EOF Register 1

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	EOF Character 1 [9]	0
8	R/W	EOF Character 1 [8]	1
7	R/W	EOF Character 1 [7]	0
6	R/W	EOF Character 1 [6]	1
5	R/W	EOF Character 1 [5]	1
4	R/W	EOF Character 1 [4]	1
3	R/W	EOF Character 1 [3]	1
2	R/W	EOF Character 1 [2]	1
1	R/W	EOF Character 1 [1]	0
0	R/W	EOF Character 1 [0]	0

EOF Character 1 [9:0]

The EOF Character 1[9:0] bits form the first character of the EOF pattern sent out after the CRC pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x122: Custom Pattern EOF Register 2

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	EOF Character 2 [9]	0
8	R/W	EOF Character 2 [8]	1
7	R/W	EOF Character 2 [7]	0
6	R/W	EOF Character 2 [6]	0
5	R/W	EOF Character 2 [5]	0
4	R/W	EOF Character 2 [4]	1
3	R/W	EOF Character 2 [3]	0
2	R/W	EOF Character 2 [2]	1
1	R/W	EOF Character 2 [1]	0
0	R/W	EOF Character 2 [0]	1

EOF Character 2 [9:0]

The EOF Character 2[9:0] bits form the second character of the EOF pattern sent out after the CRC pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x123: Custom Pattern EOF Register 3

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	EOF Character 3 [9]	0
8	R/W	EOF Character 3 [8]	1
7	R/W	EOF Character 3 [7]	1
6	R/W	EOF Character 3 [6]	0
5	R/W	EOF Character 3 [5]	0
4	R/W	EOF Character 3 [4]	1
3	R/W	EOF Character 3 [3]	0
2	R/W	EOF Character 3 [2]	1
1	R/W	EOF Character 3 [1]	0
0	R/W	EOF Character 3 [0]	1

EOF Character 3 [9:0]

The EOF Character 3[9:0] bits form the third character of the EOF pattern sent out after the CRC pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x124: Custom Pattern EOF Register 4

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	EOF Character 4 [9]	0
8	R/W	EOF Character 4 [8]	1
7	R/W	EOF Character 4 [7]	1
6	R/W	EOF Character 4 [6]	0
5	R/W	EOF Character 4 [5]	0
4	R/W	EOF Character 4 [4]	1
3	R/W	EOF Character 4 [3]	0
2	R/W	EOF Character 4 [2]	1
1	R/W	EOF Character 4 [1]	0
0	R/W	EOF Character 4 [0]	1

EOF Character 4 [9:0]

The EOF Character 4[9:0] bits form the fourth and final character of the EOF pattern sent out after the CRC pattern for the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x125: Custom Pattern Idle Register 1

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	Idle Character 1 [9]	0
8	R/W	Idle Character 1 [8]	1
7	R/W	Idle Character 1 [7]	0
6	R/W	Idle Character 1 [6]	1
5	R/W	Idle Character 1 [5]	1
4	R/W	Idle Character 1 [4]	1
3	R/W	Idle Character 1 [3]	1
2	R/W	Idle Character 1 [2]	1
1	R/W	Idle Character 1 [1]	0
0	R/W	Idle Character 1 [0]	0

Idle Character 1 [9:0]

The Idle Character 1[9:0] bits form the first character of the Idle pattern sent out before the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x126: Custom Pattern Idle Register 2

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	Idle Character 2 [9]	0
8	R/W	Idle Character 2 [8]	1
7	R/W	Idle Character 2 [7]	0
6	R/W	Idle Character 2 [6]	0
5	R/W	Idle Character 2 [5]	0
4	R/W	Idle Character 2 [4]	1
3	R/W	Idle Character 2 [3]	0
2	R/W	Idle Character 2 [2]	1
1	R/W	Idle Character 2 [1]	0
0	R/W	Idle Character 2 [0]	1

Idle Character 2 [9:0]

The Idle Character 2[9:0] bits form the second character of the Idle pattern sent out before the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x127: Custom Pattern Idle Register 3

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	Idle Character 3 [9]	0
8	R/W	Idle Character 3 [8]	1
7	R/W	Idle Character 3 [7]	0
6	R/W	Idle Character 3 [6]	1
5	R/W	Idle Character 3 [5]	0
4	R/W	Idle Character 3 [4]	1
3	R/W	Idle Character 3 [3]	0
2	R/W	Idle Character 3 [2]	1
1	R/W	Idle Character 3 [1]	0
0	R/W	Idle Character 3 [0]	1

Idle Character 3 [9:0]

The Idle Character 3[9:0] bits form the third character of the Idle pattern sent out before the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x128: Custom Pattern Idle Register 4

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9	R/W	Idle Character 4 [9]	0
8	R/W	Idle Character 4 [8]	1
7	R/W	Idle Character 4 [7]	0
6	R/W	Idle Character 4 [6]	1
5	R/W	Idle Character 4 [5]	0
4	R/W	Idle Character 4 [4]	1
3	R/W	Idle Character 4 [3]	0
2	R/W	Idle Character 4 [2]	1
1	R/W	Idle Character 4 [1]	0
0	R/W	Idle Character 4 [0]	1

Idle Character 4 [9:0]

The Idle Character 4 [9:0] bits form the last character of the Idle pattern sent out before the Custom pattern, when the Pattern Generator is selected to operate in the Custom Pattern Mode. Bit 9 is the MSB, while bit 0 is the LSB.

Register 0x129: Pattern Comparator SOF Count Register

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9		Unused	-
8		Unused	-
7	R	SOF Count [7]	0
6	R	SOF Count [6]	0
5	R	SOF Count [5]	0
4	R	SOF Count [4]	0
3	R	SOF Count [3]	0
2	R	SOF Count [2]	0
1	R	SOF Count [1]	0
0	R	SOF Count [0]	0

SOF Count [7:0]

The SOF Count Register, gives a count of the number of valid SOFs received by the Pattern Comparator. This counter saturates at 0xFF. This register is cleared when Clear Error Counters bit is written.

Register 0x12A: Pattern Comparator EOF Count Register

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9		Unused	-
8		Unused	-
7	R	EOF Count [7]	0
6	R	EOF Count [6]	0
5	R	EOF Count [5]	0
4	R	EOF Count [4]	0
3	R	EOF Count [3]	0
2	R	EOF Count [2]	0
1	R	EOF Count [1]	0
0	R	EOF Count [0]	0

EOF Count [7:0]

The EOF Count Register, gives a count of the number of valid EOFs received by the Pattern Comparator. This counter saturates at 0xFF. This register is cleared when Clear_Error Counters bit is written to.

Register 0x12B: Pattern Comparator Error Count Register

Bit	Type	Function	Default
15	R	Error Count [15]	0
14	R	Error Count [14]	0
13	R	Error Count [13]	0
12	R	Error Count [12]	0
11	R	Error Count [11]	0
10	R	Error Count [10]	0
9	R	Error Count [9]	0
8	R	Error Count [8]	0
7	R	Error Count [7]	0
6	R	Error Count [6]	0
5	R	Error Count [5]	0
4	R	Error Count [4]	0
3	R	Error Count [3]	0
2	R	Error Count [2]	0
1	R	Error Count [1]	0
0	R	Error Count [0]	0

Error Count [15:0]

The Error Count Register gives a count of the total number of errors received by the Pattern Comparator. The counter value reflects the total number of bad packets received. This counter saturates at 0xFFFF. This register is cleared when Clear Error Counters register bit is written to.

Register 0x12C: BIST STATUS Register

Bit	Type	Function	Default
15		Unused	-
14		Unused	-
13		Unused	-
12		Unused	-
11		Unused	-
10		Unused	-
9		Unused	-
8		Unused	-
7		Unused	-
6		Unused	-
5		Unused	-
4		Unused	-
3	R	BIST STATUS [3]	0
2	R	BIST STATUS [2]	0
1	R	BIST STATUS [1]	0
0	R	BIST STATUS [0]	0

BIST STATUS [3:0]

When a bit of this register is read as logic 1, it indicates that the corresponding port received at least one error during the BIST procedure and has FAILED the test. When a bit of this register is read as logic 0, it means that the corresponding port has passed the BIST procedure. These registers are automatically cleared when BIST_EN bit 7 in register 0x10F is set to logic 0 and then set to logic 1. These bits are only valid after the BIST DONE bit (see Register 0x12E: BIST Done Interrupt Status Register) is asserted.

Setting the BIST_EN bit in Register 0x10F to logic 1 enables the BIST procedure.

Register 0x12D: BIST Interrupt Enable Register

Bit	Type	Function	Default
15		Unused	0
14		Unused	0
13		Unused	0
12		Unused	0
11		Unused	0
10		Unused	0
9		Unused	0
8		Unused	0
7		Unused	0
6		Unused	0
5		Unused	0
4		Unused	0
3		Unused	0
2		Unused	0
1		Unused	0
0	R/W	BIST Interrupt Enable	0

BIST Interrupt Enable

When this bit is set to logic 1, the assertion of the BIST_DONE interrupt bit will cause INTRB to be asserted. When this bit is set to logic 0, BIST_DONE will have no effect on INTRB.

Register 0x12E: BIST Done Interrupt Status Register

Bit	Type	Function	Default
15		Unused	0
14		Unused	0
13		Unused	0
12		Unused	0
11		Unused	0
10		Unused	0
9		Unused	0
8		Unused	0
7		Unused	0
6		Unused	0
5		Unused	0
4		Unused	0
3		Unused	0
2		Unused	0
1		Unused	0
0	R	BIST DONE	0

BIST DONE

If this bit is read as logic 1, it indicates that the BIST operation is complete and the BIST STATUS Registers have been updated with their final values. This bit remains asserted as long as BIST_EN bit in register 0x10F is set, and clears to logic 0 upon read only after BIST_EN bit is cleared.

10 Test Features Description

10.1 Boundary Scan Cells

10.1.1 Boundary Scan Instructions

Table 29 Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 30 Identification Register

Length	32 bits
Version number	0H
Part Number	8372H
Manufacturer's identification code	0CDH
Device identification	083720CDH

10.1.2 Boundary Scan Registers

Table 31 Boundary Scan Registers

```
Boundary Scan Chain Information
================================


JTAG ID value (scanned out of TDO during IDCODE test): 0x0x083720CD


Note: Register bit 73 is the boundary scan cell
      closest to TDI (bit 0 is closest to TDO).

Name                    Register Bit  Cell Type
----------------------- ------------  ---------
```

OEB_MDIO_SDA	73	OUT_CELL
MDIO_SDA	72	IO_CELL
SCAN_EN	71	IN_CELL
SCANB	70	IN_CELL
CLK_SEL	69	IN_CELL
HALF_RATE	68	IN_CELL
RECEQUALIZE[1]	67	IN_CELL
RECEQUALIZE[0]	66	IN_CELL
OEB_PORT_DLOLB[0]	65	OUT_CELL
PORT_DLOLB[0]	64	OUT_CELL
OEB_PORT_DLOLB[1]	63	OUT_CELL
PORT_DLOLB[1]	62	OUT_CELL
OEB_PORT_DLOLB[2]	61	OUT_CELL
PORT_DLOLB[2]	60	OUT_CELL
OEB_PORT_DLOLB[3]	59	OUT_CELL
PORT_DLOLB[3]	58	OUT_CELL
BYPASSB[0]	57	IN_CELL
BYPASSB[1]	56	IN_CELL
OEB_RX100_150[3]	55	OUT_CELL
RX100_150[3]	54	IO_CELL
OEB_RX100_150[2]	53	OUT_CELL
RX100_150[2]	52	IO_CELL
OEB_RX100_150[1]	51	OUT_CELL
RX100_150[1]	50	IO_CELL
OEB_RX100_150[0]	49	OUT_CELL
RX100_150[0]	48	IO_CELL
OEB_TX100_150[2]	47	OUT_CELL
TX100_150[2]	46	IO_CELL
OEB_TX100_150[1]	45	OUT_CELL
TX100_150[1]	44	IO_CELL
OEB_TX100_150[0]	43	OUT_CELL
TX100_150[0]	42	IO_CELL
OEB_TX100_150[3]	41	OUT_CELL
TX100_150[3]	40	IO_CELL
RET_MODE	39	IN_CELL
RET_LPBK	38	IN_CELL
FC_GE_RET_SEL	37	IN_CELL
OEB_PORT_2G_RATE[3]	36	OUT_CELL
PORT_2G_RATE[3]	35	OUT_CELL
OEB_PORT_2G_RATE[2]	34	OUT_CELL
PORT_2G_RATE[2]	33	OUT_CELL
OEB_PORT_2G_RATE[1]	32	OUT_CELL
PORT_2G_RATE[1]	31	OUT_CELL
OEB_PORT_2G_RATE[0]	30	OUT_CELL
PORT_2G_RATE[0]	29	OUT_CELL
AUTO_RATE_SEL	28	IN_CELL
BYPASSB[2]	27	IN_CELL
BYPASSB[3]	26	IN_CELL
OEB_DVPRTAD[4]	25	OUT_CELL
DVPRTAD[4]	24	IO_CELL
OEB_DVPRTAD[3]	23	OUT_CELL
DVPRTAD[3]	22	IO_CELL
OEB_DVPRTAD[2]	21	OUT_CELL
DVPRTAD[2]	20	IO_CELL

OEB_DVPRTAD[1]	19	OUT_CELL
DVPRTAD[1]	18	IO_CELL
OEB_DVPRTAD[0]	17	OUT_CELL
DVPRTAD[0]	16	IO_CELL
TWISEL	15	IN_CELL
OENB	14	IN_CELL
DEVBYPSB	13	IN_CELL
DLOLBYP_MASK	12	IN_CELL
EXTCAP	11	IN_CELL
PREEMPH[1]	10	IN_CELL
PREEMPH[0]	9	IN_CELL
RECRET_SEL	8	IN_CELL
TRUST_MODE	7	IN_CELL
MON_BYP_PORT	6	IN_CELL
OEB_INTRB	5	OUT_CELL
INTRB	4	OUT_CELL
OEB_DLOLB	3	OUT_CELL
DLOLB	2	OUT_CELL
RESETB	1	IN_CELL
MDC_SCL	0	IN_CELL

11 Operation

11.1 Power-up

The QuadPHY RT device can start in hardware only mode, without any management interface in all its operational modes. However, management interface is required for testing, debugging and for configuring device in manual modes as well as for the pattern generation and checking modes. All error counters can be disabled by holding the DLOLBYP_MASK pin to logic 1. After configuring the device in the users application specific mode, a Global Soft Reset , register 0x002 bit 14, must be issued to reset all state machines. Soft reset must be asserted for minimum of 200 ns. The user must issue a soft reset after changing any of the device configuration registers.

To read all dynamic counters and status registers in the device, the clear error counter bit must be written to. This will reset the current value and transfer the old value to shadow registers to be read by the management interface. It is recommended that Clear_Error_counter register bit be set after a soft reset.

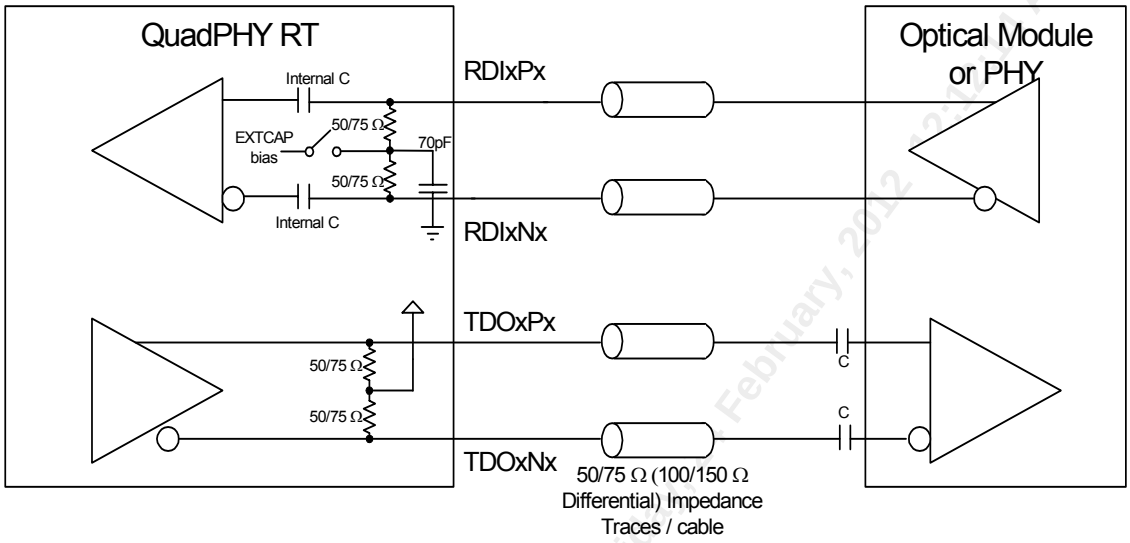
11.2 High-Speed Serial Interface

As shown in Figure 22, the high-speed serial interface is a set of differential drivers and receivers operating over 50 or 75 Ω transmission lines. The serial transmit outputs are internally terminated, complementary current-sourcing drivers. The serial receive inputs are differential receivers with internal 100 Ω differential terminations when the corresponding RX100/150 input is set to logic 0 or with 150 Ω differential terminations when the corresponding RX100/150 input is set to logic 1.

For proper operation, all high-speed inputs must be capacitively coupled, as shown in Figure 22. In this case, the EXTCAP pin (or equivalent registers) must be set to 1. However, the internal AC coupling can be used without extra external coupling caps if both inputs signals are guaranteed to be at all times between 0 and VDD_18 volts (single-ended measurement). The QuadPHY RT is internally biased to the proper DC operating point.

The skew between the P and N signals for the high-speed inputs should be less than or equal to 50 ps. The equivalent line length difference for FR4 material would be less than or equal to 5/16 of an inch.

Figure 22 High-Speed Serial Interfaces



11.3 Clock Requirements

REFCLK (single ended or differential) is a maximum 125 MHz ±100 ppm 40/60 or better oscillator. The maxmum jitter allowed is 50 ps peak to peak, or approximately 7 ps rms. REFCLK feeds 2.5/1.8 V CMOS input. The oscillator requires good power supply rejection to provide a low jitter clock input to the device. The driving crystal oscillator may be capacitively coupled to REFCLK and biased around the switching threshold of the REFCLK input.

Differential REFCLK (REFCLK_P/N) must be AC-coupled.

11.4 Analog Considerations

A precision resistor must be connected between the RPRES terminal and ground. It is used as a reference for internal bias circuits. The value of RPRES must be 10 kΩ ± 1%.

11.5 JTAG Considerations

A pull-down resister connected to the QuadPHY RT device's TRSTB pin is recommended to assure that the JTAG TAP Controller remains in a reset state during normal operation of the device.

11.6 Board Design Recommendations

Refer to PM8372 PBC4x2G Evaluation Board Design Document (PMC-2031155) for board design guidelines and recommendation.

11.7 MDC/MDIO Interface

The MDIO implementation on the QuadPHY RT is logically compliant to the MDIO protocol as defined in the IEEE 802.3ae however the signaling levels (3.3V) are not compliant with those defined in IEEE802.3ae (1.2V). The MDC/MDIO interface is a 2-wire single master, multi-slave protocol. The master device sources the clock (MDC) to all slaves. The tri-state data (MDIO) wire is attached to all devices and is used for reading and writing. Figure 23 contains functional timing for an MDC/MDIO write cycle. A 32-bit preamble (PRE) can optionally be skipped if the Station Management Entity (STA) determines that all PHY devices can handle management frames without it. The MDC/MDIO interface requires that a full 32 bit preamble be applied prior to the start of each transaction.

Figure 23 MDC/MDIO Write Cycle

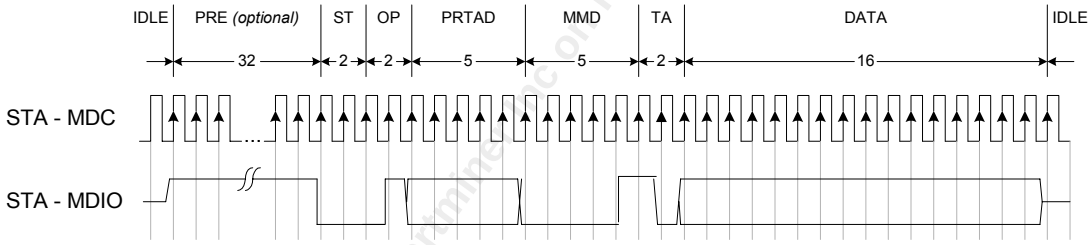
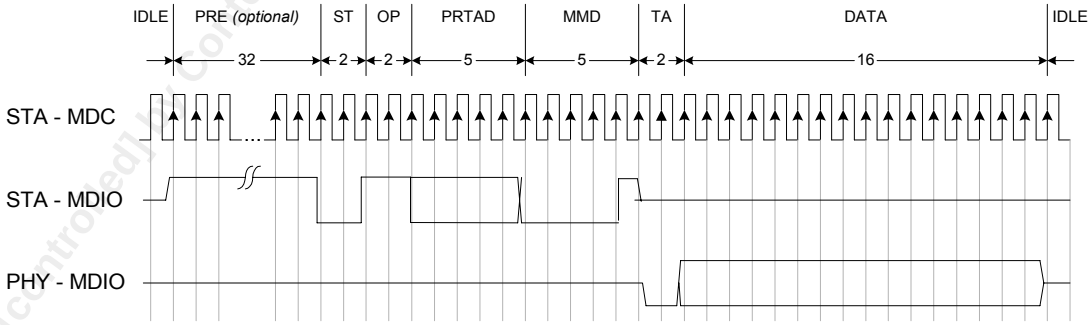


Figure 24 demonstrates an MDC/MDIO read cycle. Here too, the 32-bit preamble can be optionally skipped if the STA determines that all the PHY devices can handle management frames without it.

Figure 24 MDC/MDIO Read Cycle



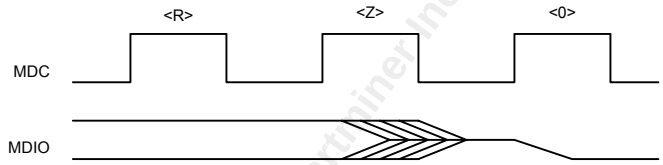
It is required for a preamble to be applied to the MDC/MDIO interface whenever an error has occurred during an access. This allows the interface to recover from the error. In the case of a free running MDC clock, this can be accomplished by having a pause in the interface, since the MDIO pin is pulled-up when not in use.

Notes:

1. IDLE – Idle. The period when data transfer on MDIO is inactive. The MDC clock may stall until the next transfer or continue to run.
2. PRE [31:0] – Preamble. An optional stream of 32 - 1's which assures the receive logic that a transfer is about to occur.
3. ST[1:0] – Start bits. This is always a 0b00.
4. OP[1:0] – Operation Code. Address is a 0b00, a write is a 0b01, a read is a 0b11, and a read increment is a 0b10.
5. PRTAD[[4:0] – PHY Address. This is the 5 bit address must match the DVAD[4:0] pins on the device for the QuadPHY RT to respond to the access.
6. MMD[4:0] – The QuadPHY RT operates as a PMA/PMD. These bits must be set to 0b00001.
7. TA[1:0] – Turn Around Cycle. This is a 2-bit time spacing interval that exists to avoid contention on the MDIO net during a read cycle.
8. DATA[15:0] – Data. This is either read data supplied by the slave or write data supplied by the master.

Figure 25 shows how the MDIO signal transitions during the turn around cycles of a read transaction. These turn around cycles are necessary to avoid contention on the MDIO net.

Figure 25 Behavior of MDIO During TA Field of a Read Transaction



11.8 Two Wire Interface

Figure 26 TWI Functional Timing

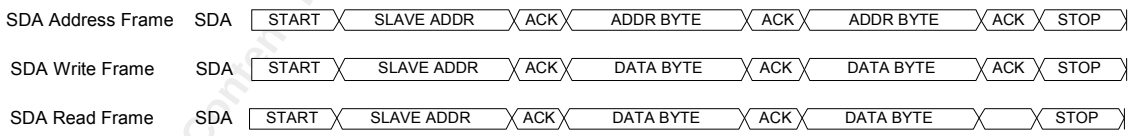


Figure 26 shows the 3 basic types of TWI transfers on the SDA primary bi-directional pin. The SCL clock is not shown for simplicity.

12 Absolute Maximum Ratings

Maximum rating is the worst-case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 32 Maximum Ratings

Storage Temperature	-40 °C to +125 °C
1.8V Supply Voltage (VDD_18/VDDA)	-0.5 V to +2.5 V
3.3V Supply Voltage (VDD_33)	-0.5 to +4.6 V
Input pad tolerance	-2 V < Vpin < VDD_33 +2 V for 10 ns, 100 mA Max
Output pad overshoot limits	-2 V < Vpin < VDD_33 +2 V for 10 ns, 100 mA Max
Voltage on Any Digital Pin	-0.3 V to VDD_33+0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead/Ball Temperature	+225 +0/-5 °C
Absolute Maximum Junction Temperature	+150 °C

13 Power Information

13.1 Power Requirements

Table 33 Typical Power requirements

Operation mode	Parameter	Typ	Power for Thermal Calculations	Max Current	Units
2G Fiber Channel (2 ports)	IDDOP VDD_18	410	-	651	mA
	IDDOP VDDA	39	-	83	mA
	IDDOP VDD_33	1	-	2.26	mA
	Total Power	0.81	1.03	—	W
2G Fiber Channel (3 ports)	IDDOP VDD_18	515	-	751	mA
	IDDOP VDDA	39	-	83	mA
	IDDOP VDD_33	1	-	2.26	mA
	Total Power	1.00	1.23	—	W
2G Fiber Channel (4 ports)	IDDOP VDD_18	614	-	844	mA
	IDDOP VDDA	39	-	83	mA
	IDDOP VDD_33	1	-	3	mA
	Total Power	1.18	1.4	—	W
GE Retimer (4 ports)	IDDOP VDD_18	606	-	807	mA
	IDDOP VDDA	40	-	85	mA
	IDDOP VDD_33	1	-	2	mA
	Total Power	1.16	1.38	—	W

Notes:

Power values are calculated using the formula:

$$\text{Power} = \sum i(\text{VDD} \times \text{IDD})$$

Where i denotes all the various power supplies on the device, VDDNomi is the voltage for supply i, and IDDTyp is the current for supply i .

13.2 Power Supply Filtering

1. Use a single plane for both digital and analog grounds.

2. Provide separate analog and digital supplies. Otherwise connect the supply voltages together at one point close to the connector where the voltage is brought to the card.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

13.3 Power Supply Decoupling

Figure 27 illustrates the scheme required for power supply conditioning. Component values may need adjustment to match the characteristics of the board in which the conditioning will be applied.

The 10uF Ceramic caps are X5R (X7R) type, and not Tantalum or Y5V, for best frequency response and lowest ESR. Recommended components are Taiyo Yuden PN # LMK325BJ106MN or Panasonic PN # ECJ-3YB0J106K.

Boards that meet the following criteria may use a distributed decoupling scheme, with 0.1 uF capacitors placed on a one-inch grid.

- VDD and VDDQ pins are connected to large power planes with a minimum area of 20 square inches (~ 130 cm2) adjacent to a ground plane.
- Board stack-up has a maximum power plane to ground plane spacing of 0.006 inches (~ 0.15 mm)

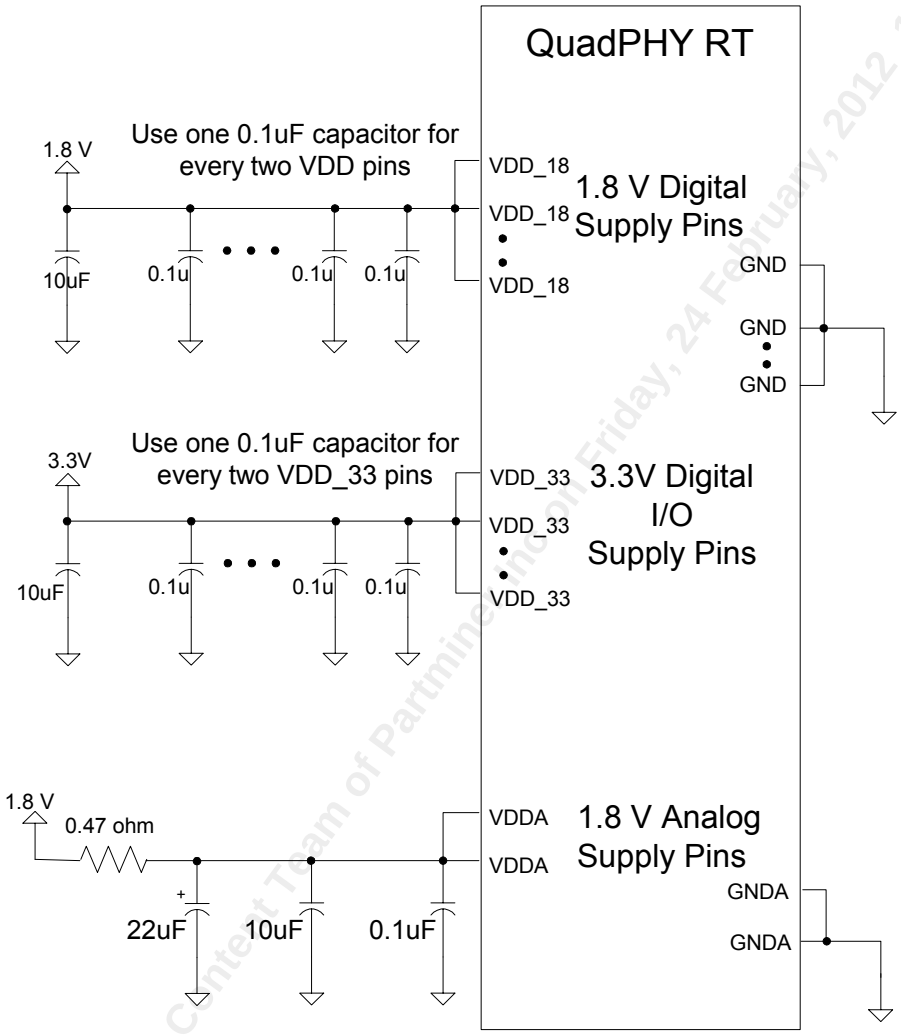
A distributed decoupling capacitor placement offers significant improvements compared to grouped placement of capacitors.

On boards that do not meet these criteria, one capacitor should be used for every two VDD_18 (or every two VDD_33) pins. The 0.1 uF capacitors should be placed as close as possible to each power pin and to ground layer. The traces from the capacitors to the QuadPHY RT power pins and to the ground plane should be as short as possible to limit series inductance.

For further information regarding power supply filtering, please refer to the Digital Power Supply Bypass Guidelines Application Note [PMC-2012008].

In order to minimize the intrinsic jitter on the TDO outputs, RC filtering of the VDDA supply voltage is required. The values shown in Figure 27 were chosen to minimize the IR drop on the VDDA supply voltage, yet provide sufficient filtering of power supply noise at low frequencies.

Figure 27 Recommended Power Supply Decoupling



14 D.C. Characteristics

Unless otherwise stated, the following parameters are provided given the following conditions: Ta = -40° C to Tj = 125° C, VDD_33= 3.3 V ±5%, VDDA/VDD_18 = 1.8 V ±5%

Table 34 D.C. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDDA	Supply voltage		1.71	1.8	1.89	V
VDD_33	Low-speed Quiet I/O Supply Voltage for 3.3V applications		3.135	3.3	3.465	V
VDD_18	Analog 1.8 V Supply Voltage		1.71	1.8	1.89	V
V_{OH}	Output or Bi-directional High Voltage	Output high voltage at VDD_33 = 3.135 IOH=10mA for mdio_sda, IOH=6mA for others	2.4	2.7		V
V_{OL}	Output Low Voltage for outputs	Output low voltage at VDD_33 = 3.135 and IOL=-10mA for mdio_sda, IOH=6mA for others		0.1	0.4	V
V_{IH}	Input High Voltage for inputs	Input High voltage	2.0		VDDQ+0.5	V
V_{IL}	Input Low Voltage for inputs	Input Low voltage	-0.5		0.8	V
I_{IL}	Input Low Current for inputs	Input Low current	-10	0	+10	µA
I_{IH}	Input High Current for inputs	Input High current	-10	0	+10	µA
V_{IH_DIFF}	REFCLKP, REFCLKN Input High Voltage[1,2]	Pins must be AC-coupled	800		1600	mVppd
V_{IH}	REFCLKS[3] Input High Voltage	Single ended ref clk	0.8*V_{DD}		V_{DD}+ 0.3	V
V_{IL}	REFCLKS[3] Input Low Voltage	Single ended ref clk	0.2*V_{DD}		0.35*V_{DD}	V
C_{IN}	Input Capacitance for digital inputs	Including Package, Package Typically 2 pF		7.0		pF
C_{IN}	Input Capacitance for High Speed inputs	Including Package, Package Typically 2pF		3.0		pF
Cout	Output capacitance for digital outputs	Including Package, Package Typically 2 pF		7.0		pF
CIO	Bi-directional Capacitance	Including Package, Package Typically 2 pF		7.0		pF

Notes:

Input pin or bi-directional pin with internal pull-up resistor

1. LVPECL buffer should use and external 0.1uF coupling capacitor on both P and N inputs.
2. REFCLK specifications apply to PCB side of AC coupling capacitors
3. This buffer is 3.3V tolerant.

15 Interface Timing Characteristics

Unless otherwise stated, the following parameters are provided given the following conditions: Ta = -40° C to Tj = 125° C, VDD_33 = 3.3 V ±5%, , VDDA/VDD_18 = 1.8 V ±5%

15.1 Reference Clock

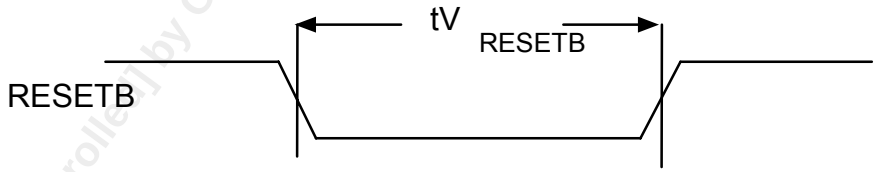
Table 35 Reference Clock Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{REFCLK}	REFCLK Frequency					MHz
	GE Mode		125 – 100ppm	125	125 + 100ppm	
	FC Mode		106.25 – 100ppm	106.25	106.25 + 100ppm	
f_{R_PECL}	REFCLK Rise/Fall Time (at receiving Device)	$V_{IL\_PECL(Max)}$ to $VI_{H\_PECL(min)}$			800	ps
Peak to peak jitter on REFCLK	Wideband Peak to peak jitter on REFCLK (Maximum). (RMS jitter is peak to peak jitter divided by 7)				50	ps
	Narrowband peak to peak jitter on REFCLK (12 KHz – 20 MHz)				20	
F_lock	Frequency lock after reset with REFCLK active				500	µs

15.2 Asynchronous Reset

Figure 28 QuadPHY RT's Reset Timing

Symbol	Description	Min	Max	Units
tVRESETB	RESETB Pulse Width	100	-	us



Note that RESETB should not be asserted for very long periods of time (many minutes or more).

After RESETB has been set high, the CSU may require up to 200 uS to regain lock.

15.3 MII Management Interface (MDC/MDIO)

Table 36 MDIO Timing

Symbol	Description	Min	Max	Units
f_{MDCMAX}	Clock Frequency (MDC)	0	10	MHz
$t_{MDCHIGH}$	MDC High Pulse Width	45	—	ns
t_{MDCLOW}	MDC Low Pulse Width	45	—	ns
$t_{MDCRISE}$	MDC Rise Time [1]	—	5	ns
$t_{MDCFALL}$	MDC Fall Time [1]	—	5	ns
$t_{MDIORISE}$	MDIO Input Rise Time [1]	—	5	ns
$t_{MDIOFALL}$	MDIO Input Fall Time [1]	—	5	ns
t_{MDIO_S}	MDIO Setup Time	10	—	ns
t_{MDIO_H}	MDIO Hold Time	10	—	ns
t_{pMDIO}	MDC to MDIO valid data	0	11	ns
t_{zMDIO}	MDC to MDIO high-impedence	—	10	ns

Notes:

1. MDC or MDIO rise times and fall times are measure from 10% to 90%.
2. For proper operation at the specified Maximum MDC frequency, the MDIO load capacitance must not exceed 100 pf.

Figure 29 MDIO Timing Diagram

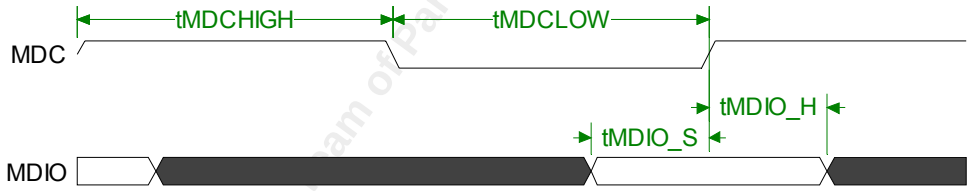
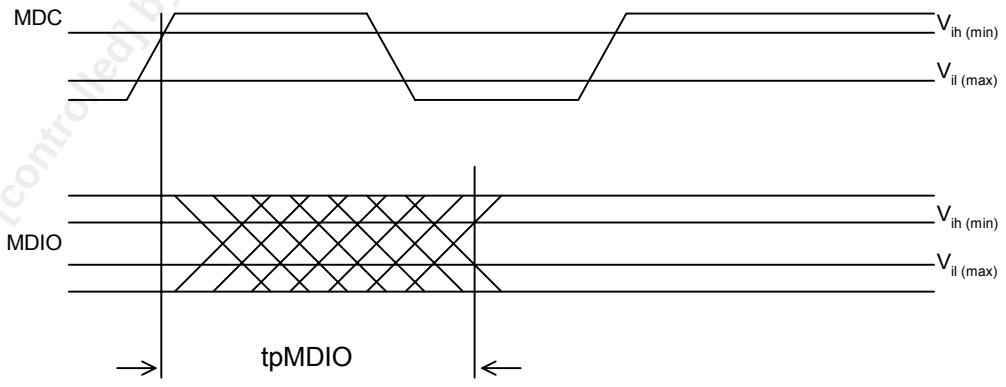


Figure 30 MDIO Sourced by PHY



15.4 Two-Wire Interface

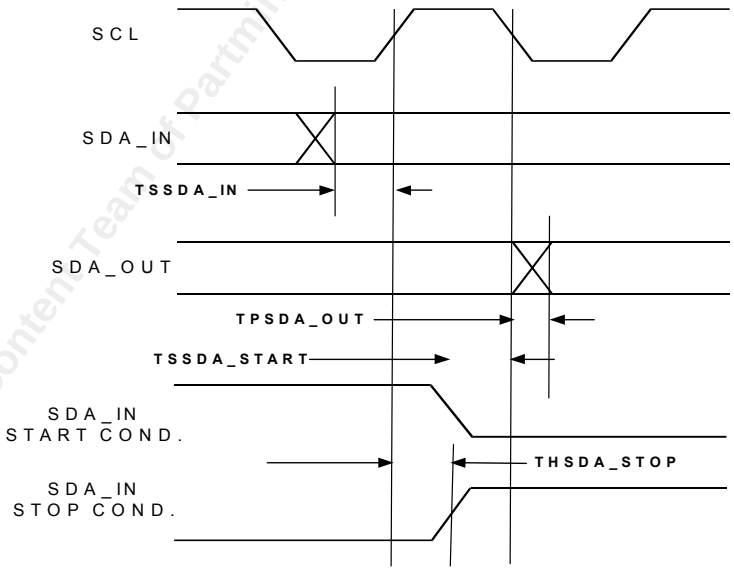
Table 37 TWI Bus Rate

Freq	Mode
0 – 100 Khz	Standard
100 – 400 Khz	Fast
400kHz – 3.4 Mhz	High Speed

Table 38 TWI Data Timing

Symbol	Description	Min	Typ	Max	Units
TSSDA_IN	SDA_IN Setup time	10			ns
TPSDA_OUT	SDA_OUT propagation delay	0		70	ns
TSSDA_START	SDA_IN START COND. Setup time	160			ns
THSDA_STOP	SDA_IN STOP COND. Hold time	160			ns

Figure 31 TWI Data AC Timing Characteristic



15.5 JTAG

Figure 32 JTAG Port Interface Timing

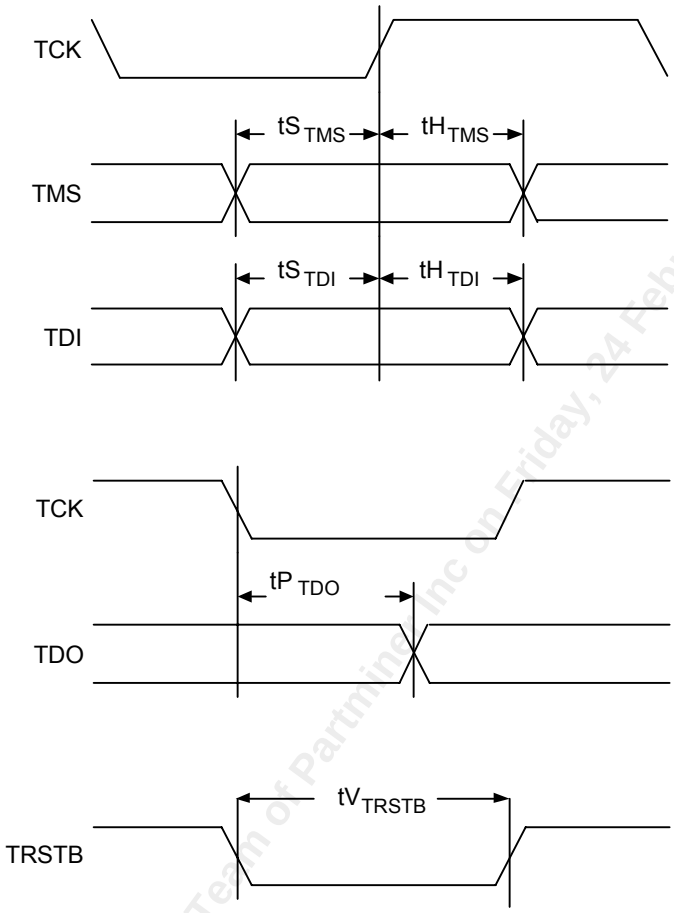


Table 39 JTAG Port Interface

Symbol	Description	Min	Max	Units
—	TCK Frequency	—	1	MHz
—	TCK Duty Cycle	40	60	%
t_{STMS}	TMS Set-up time to TCK	50	—	ns
t_{HTMS}	TMS Hold time to TCK	50	—	ns
t_{STDI}	TDI Set-up time to TCK	50	—	ns
t_{HTDI}	TDI Hold time to TCK	50	—	ns
t_{PTDO}	TCK Low to TDO Valid	2	50	ns
t_{VTRSTB}	TRSTB Pulse Width	100	—	ns
$t_{TRSTBRISE}$	TRSTB Rise Time	—	10	ns

15.6 Latency

Table 40 Latency

Parameter	Min	Typ	Max	Unit
Latency of RDI_P/N[n] -> TDO_P/N[n] via the Reclocker path	—	7	—	ns
Latency of RDI_P/N[n] -> TDO_P/N[m] via the Retimer path in FC mode	—	240	360	Bits
Latency of RDI_P/N[n] -> TDO_P/N[m] via the Retimer path in GE mode	—	275	365	Bits

15.7 High-speed Serial Timing Characteristics

Figure 33 1.0625 to 2.5 Gbits/s Serial I/O Block Diagram

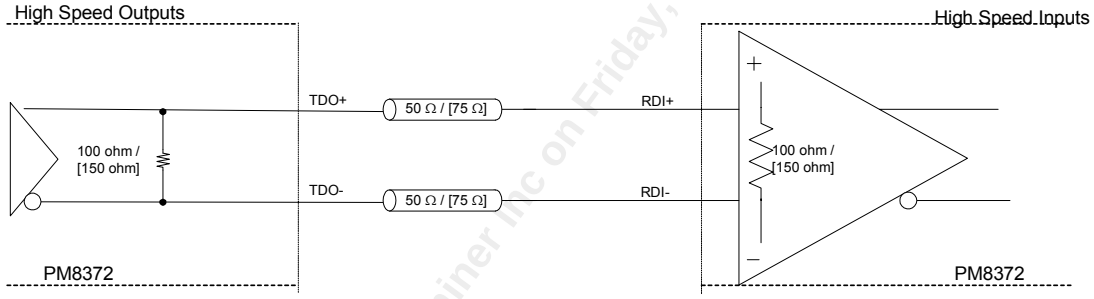
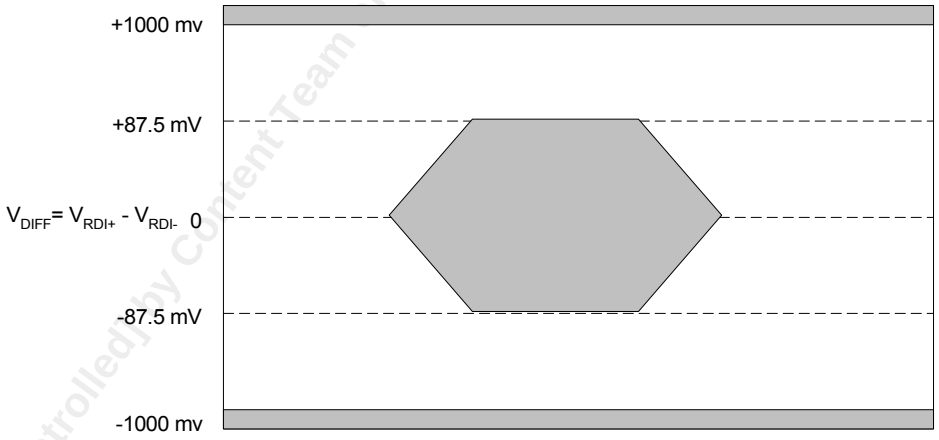


Figure 34 Differential Peak-Peak Receiver Eye Diagram



Note:

- Minimum differential sensitivity (peak to peak) is 20 the magnitude of the minimum physical potential that can be expected across the differential pair.

V_{DIFF} can be +100 mV for logic 1 or –100 mV for logic 0.

When viewing a data eye on an oscilloscope using a differential probe across signals A and B, the top and bottom of the eye will have a Maximum separation of $V_{diff\ peak\ to\ peak}$. If the same signal is measured using a single ended probe attached to signal A and referenced to GND, the top and bottom of the eye will have a Maximum vertical separation of $|V_{diff}|$. The single ended measurement technique will yield a vertical eye opening equal to ½ the vertical eye opening of the differential measurement technique.

Table 41 High-speed I/O Characteristic Definitions

Definitions	
Vdiff	Voltage of signal A – Voltage of signal B. Vdiff swings both positive and negative in value.
|Vdiff|	The magnitude of Vdiff. Vdiff is always a positive number and represents the Maximum voltage that can exist between signals A and B.
Vdiff peak-to-peak	Represents the peak-to-peak difference of the differential voltage Vdiff. Vdiff p-p will always be twice the magnitude of the Maximum voltage that can exist between signals A and B.

Table 42 High-speed I/O Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
$\|V_{RDI+} - V_{RDI-}\|$	High-speed input differential voltage magnitude	87.5	—	1000	mV pk differential
$V_{ID(ppk)}$	High-speed input peak-peak differential voltage	150	—	2000	mV pk – pk differential
$V_{OD(ppk)}$	High-speed output peak-peak differential voltage Pre-emphasis off (High Swing Mode)	1218	—	2040	mV pk – pk differential
$V_{OD(ppk)}$	High-speed output peak-peak differential voltage Pre-emphasis off (Medium Swing Mode)	972	—	1666	mV pk – pk differential
$V_{OD(ppk)}$	High-speed output peak-peak differential voltage Pre-emphasis off (Low Swing Mode)	684	—	1208	mV pk – pk differential
$V_{deemphasized}$	High-speed output deemphasized level, PREEMPH[1:0]=01		75%		peak-peak differential voltage with Pre-emphasis off
$V_{deemphasized}$	High-speed output deemphasized level, PREEMPH[1:0]=10		50%		peak-peak differential voltage with Pre-emphasis off
$V_{deemphasized}$	High-speed output deemphasized level, PREEMPH[1:0]=11		33%		peak-peak differential voltage with Pre-emphasis off
tr, tf	High-speed rise and fall times, 20 % – 80 %	100	—	200	ps
t_{SKEW}	Differential Output Skew between high-speed output signals TDOP/N	—	—	30	ps
1G FC					
T_J,	Total output jitter	—	—	0.23	UI (beta T point, no sine jitter)
T_{DJ}	Deterministic output jitter	—	—	0.11	UI (beta T point)
R_{RJT}[1]	Total Jitter Tolerance	0.68			UI (beta R point, including 0.1UI sine jitter)
R_{DJT}	Deterministic Jitter Tolerance	0.37			UI (beta R point)
2G FC					
T_J,	Total output jitter	—	—	0.330	UI (beta T point, no sine jitter)
T_{DJ}	Deterministic output jitter	—	—	0.200	UI (beta T point)
R_{RJT}[1]	Total Jitter Tolerance	0.620			UI (beta R point, including 0.1UI sine jitter)

R_{DJT}	Deterministic Jitter Tolerance	0.330			UI (beta R point)
1GE					
T_J,	Total output jitter	—	—	0.240	UI (beta T point, no sine jitter)
T_{DJ}	Deterministic output jitter	—	—	0.100	UI (beta T point)
R_{RJT}[1]	Total Jitter Tolerance	0.749			UI (beta R point, including 0.1UI sine jitter)
R_{DJT}	Deterministic Jitter Tolerance	0.462			UI (beta R point)

Notes:

1. Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter.
2. The jitter values that are specified in Table 42 assume the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit.
3. The QuadPHY RT is compliant with the Fibre Channel – Methodologies for Jitter and Signal Quality Specification (MJSQ) Rev. 13
4. $V_{OD(ppk)}$ without preemphasis are A.C. values, measured at the pin into an ideal termination.
5. High Speed output peak-peak differential voltage (Vodppk) are measured with 100 ohm external differential termination at the pin of the device.
6. Rise and Fall times (tr, tf) are measured with board trace, connector and approximately 2.5pf load.

16 Rx Differential Return Loss

Table 43 Rx Differential Return Loss

Symbol	Parameter	Min	Typ.	Max	Units
Diff Ret loss,RX	Differential Return loss, 0 – 1 GHz, for high-speed input signals RDI_P/_N		15		dB

17 Thermal Information

This product is designed to operate over a wide temperature range and is suited for outside plant equipment[1].

Table 44 Outside Plant Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125°C
Minimum ambient temperature (T_A)	-40 °C

Table 45 Thermal Resistance vs. Air Flow[2,3]

Airflow	Natural Convection	1 m/s	2 m/s
θ_{JA} (°C/W)	32.48	28.93	31.54

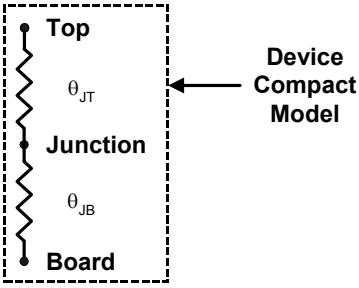


Table 46 Device Compact Model[4]

Junction-to-Top Thermal Resistance, θ_{JT}	8.5 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	23.7 °C/W

Table 47 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[5]	The sum of $\theta_{SA} + \theta_{CS}$ must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}]$ °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package[5]
	θ_{SA} and θ_{CS} are required for long-term operation

Power depends upon the operating mode. To obtain power information, refer to 'High' power values in section 13.1 Power Requirements.

Notes

1. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core; for more information about this standard, see [**12**]
2. θJA, the total junction to ambient thermal resistance, is measured according to JEDEC Standard JESD51 (2S2P); for more information about this standard, see [**10**]

3. θJB, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8 (for more information about this standard, see [**10**]) and θJT, the junction-to-top thermal resistance, is obtained by simulating conditions described in SEMI Standard G30-88 (for more information about this standard, see [**13**])

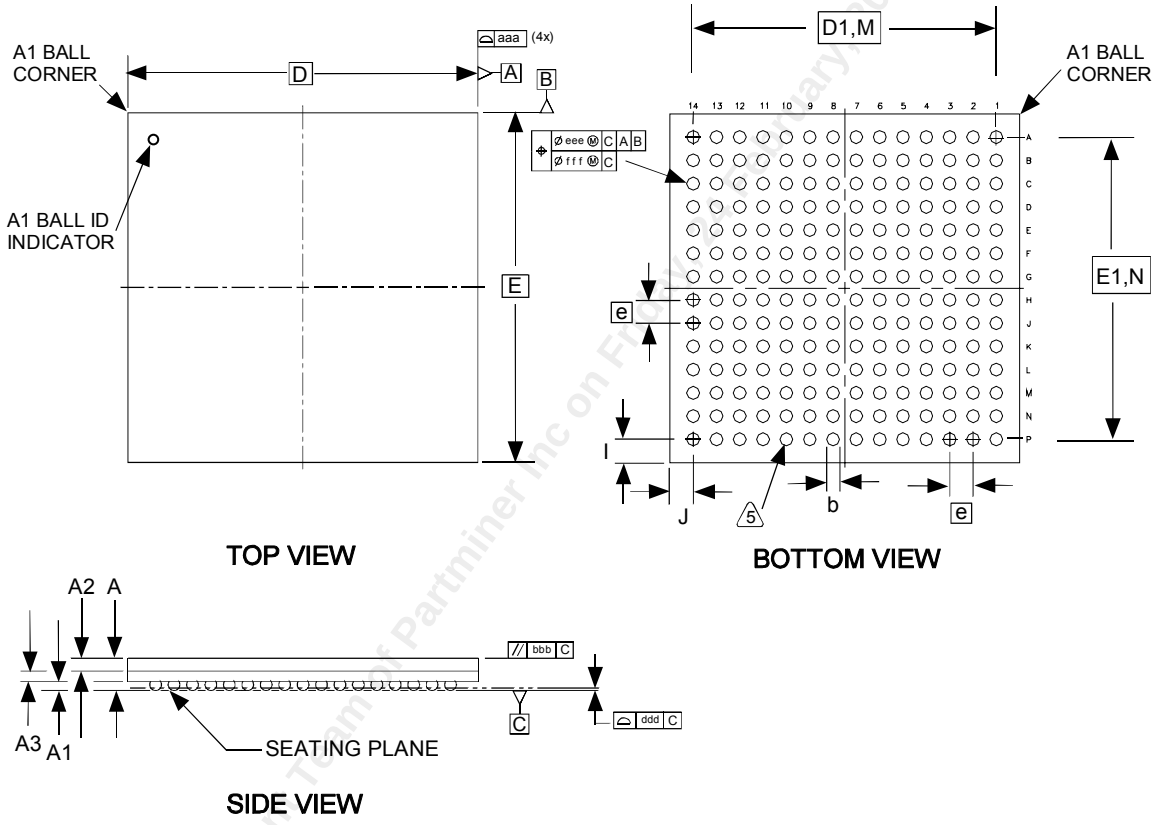
4. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8; for more information about this standard, see [**11**]

5. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place

18 Mechanical Information

This mechanical package diagram QuadPHY RT device's 196-pin Chip Array Ball Grid Array (CABGA) Package is shown in Figure 35. After assembly, the QuadPHY RT is tested to meet or exceed a 0.15 mm (5.9 mil) co planarity specification.

Figure 35 Mechanical Drawing 196 Pin Chip Array BGA



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) SOLDER MASK OPENING 0.435 +/- 0.03 MM DIAMETER (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MO-192, VARIATION AAE-1.

PACKAGE TYPE : 196 CHIP ARRAY BALL GRID ARRAY - CABGA																		
BODY SIZE : 15 x 15 x 1.40 MM																		
Dim.	A	A_1	A_2	A_3	D	D_1	E	E_1	M,N	I	J	b	e	aaa	bbb	ddd	eee	f f f
Min.	1.30	0.31	0.65	0.34	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Nom.	1.40	0.36	0.70	0.34	15.00 BSC	13.00 BSC	15.00 BSC	13.00 BSC	14x14	1.00	1.00	0.46	1.00 BSC	-	-	-	-	-
Max.	1.50	0.41	0.75	0.34	-	-	-	-	-	-	-	-	-	0.10	0.10	0.12	0.15	0.08

Notes