

MC14015B

Dual 4-Bit Static Shift Register

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design —
Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|------------------------------------|--|--------------------------------|------|
| V _{DD} | DC Supply Voltage | - 0.5 to + 18.0 | V |
| V _{in} , V _{out} | Input or Output Voltage (DC or Transient) | - 0.5 to V _{DD} + 0.5 | V |
| I _{in} , I _{out} | Input or Output Current (DC or Transient), per Pin | ± 10 | mA |
| P _D | Power Dissipation, per Package† | 500 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L | Lead Temperature (8-Second Soldering) | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

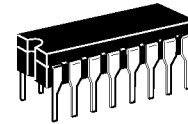
TRUTH TABLE

| C | D | R | Q ₀ | Q _n |
|---|---|---|----------------|------------------|
| ↗ | 0 | 0 | 0 | Q _{n-1} |
| ↗ | 1 | 0 | 1 | Q _{n-1} |
| ↘ | X | 0 | No Change | No Change |
| X | X | 1 | 0 | 0 |

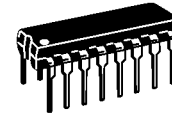
X = Don't Care

Q_n = Q₀, Q₁, Q₂, or Q₃, as applicable.

Q_{n-1} = Output of prior stage.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

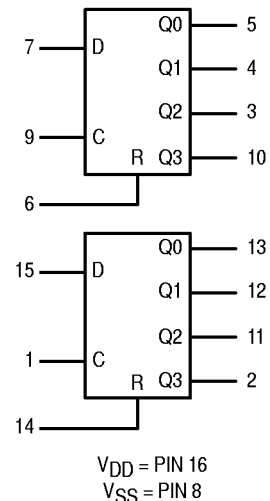


D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC
T_A = - 55° to 125°C for all packages.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | -55°C | | 25°C | | | 125°C | | Unit | |
|---|---|------------------------|--|-------|-------|----------|-------|-------|-------|------|------|
| | | | Min | Max | Min | Typ # | Max | Min | Max | | |
| Output Voltage "0" Level V _{in} = V _{DD} or 0 | V _{OL} | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc | |
| | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | | |
| V _{in} = 0 or V _{DD} "1" Level | V _{OH} | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc | |
| | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | | |
| Input Voltage "0" Level (V _O = 4.5 or .05 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | V _{IL} | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | Vdc | |
| | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | | |
| | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | | |
| | (V _O = 0.5 or 4.5 Vdc) "1" Level (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) | V _{IH} | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | Vdc |
| | | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | | 15 | 11 | — | 11 | 8.25 | — | 11 | — | |
| Output Drive Current (V _{OH} = 2.5 Vdc) Source (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | I _{OH} | 5.0 | -3.0 | — | -2.4 | -4.2 | — | -1.7 | — | mAdc | |
| | | 5.0 | -0.64 | — | -0.51 | -0.88 | — | -0.36 | — | | |
| | | 10 | -1.6 | — | -1.3 | -2.25 | — | -0.9 | — | | |
| | (V _{OL} = 0.4 Vdc) Sink (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc) | I _{OL} | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc |
| | | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| | | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | |
| Input Current | I _{in} | 15 | — | ± 0.1 | — | ±0.00001 | ± 0.1 | — | ± 1.0 | μAdc | |
| Input Capacitance (V _{in} = 0) | C _{in} | — | — | — | — | 5.0 | 7.5 | — | — | pF | |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μAdc | |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | | |
| Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 | I _T = (1.2 μA/kHz)f + I _{DD} | | | | | | | μAdc | |
| | | 10 | I _T = (2.4 μA/kHz)f + I _{DD} | | | | | | | | |
| | | 15 | I _T = (3.6 μA/kHz)f + I _{DD} | | | | | | | | |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

| | | | |
|-----------------|-----|----|-----------------|
| C _B | 1 ● | 16 | V _{DD} |
| Q3 _B | 2 | 15 | D _B |
| Q2 _A | 3 | 14 | R _B |
| Q1 _A | 4 | 13 | Q0 _B |
| Q0 _A | 5 | 12 | Q1 _B |
| R _A | 6 | 11 | Q2 _B |
| D _A | 7 | 10 | Q3 _A |
| V _{SS} | 8 | 9 | C _A |

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V _{DD} | Min | Typ # | Max | Unit |
|---|-------------------------|-----------------|-------------------|-------------------|--------------------|---------------|
| Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | $t_{TLH},$ t_{THL} | 5.0 10 15 | — — — | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time Clock, Data to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 225 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ Reset to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 375 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 95 \text{ ns}$ | $t_{PLH},$ t_{PHL} | 5.0 10 15 | — — — | 310 125 90 | 750 250 170 | ns |
| Clock Pulse Width | t_{WH} | 5.0 10 15 | 400 175 135 | 185 85 55 | — — — | ns |
| Clock Pulse Frequency | f_{cl} | 5.0 10 15 | — — — | 2.0 6.0 7.5 | 1.5 3.0 3.75 | MHz |
| Clock Pulse Rise and Fall Times | t_{TLH}, t_{THL} | 5.0 10 15 | — — — | — — — | 15 5 4 | μs |
| Reset Pulse Width | t_{WH} | 5.0 10 15 | 400 160 120 | 200 80 60 | — — — | ns |
| Setup Time | t_{su} | 5.0 10 15 | 350 100 75 | 100 50 40 | — — — | ns |

* The formulas given are for typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

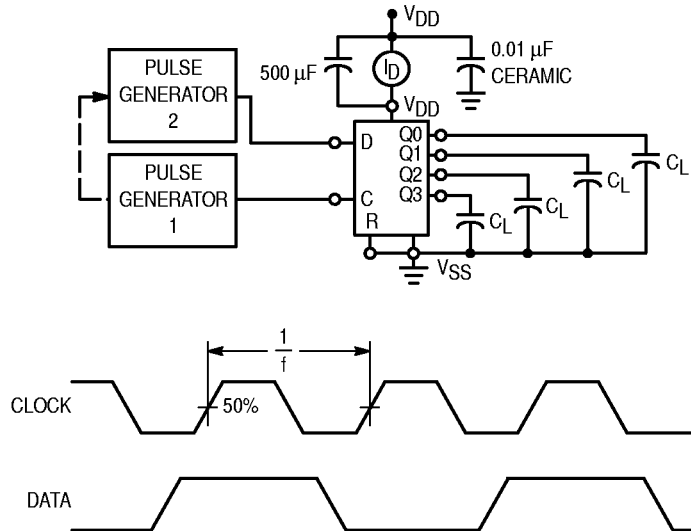


Figure 1. Power Dissipation Test Circuit and Waveform

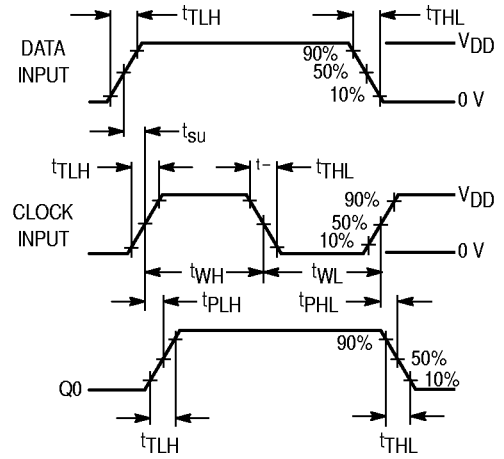
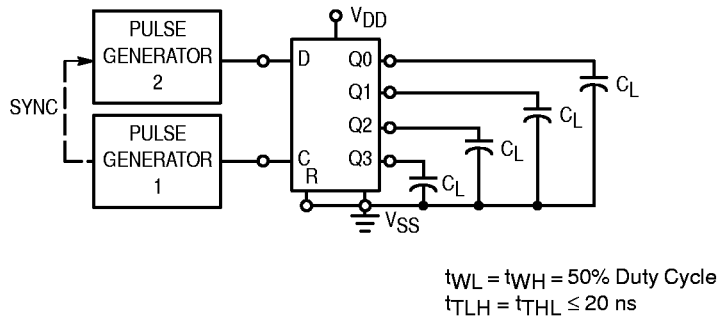


Figure 2. Switching Test Circuit and Waveforms

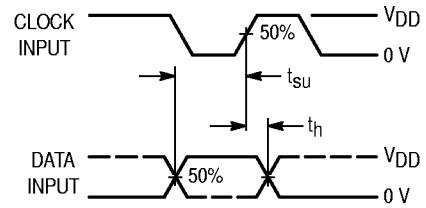
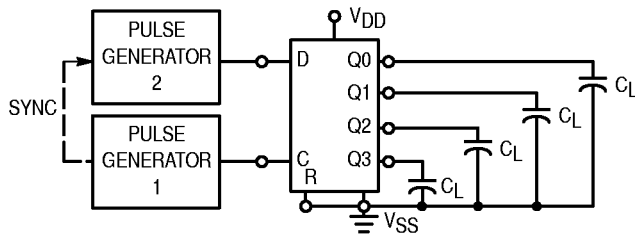
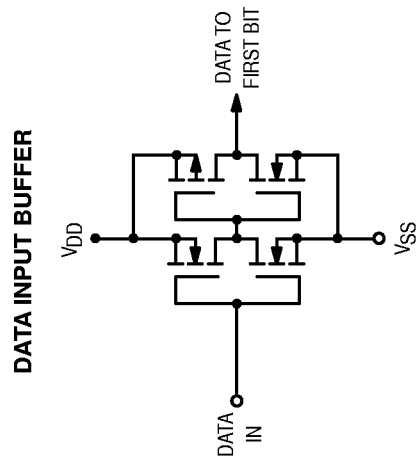
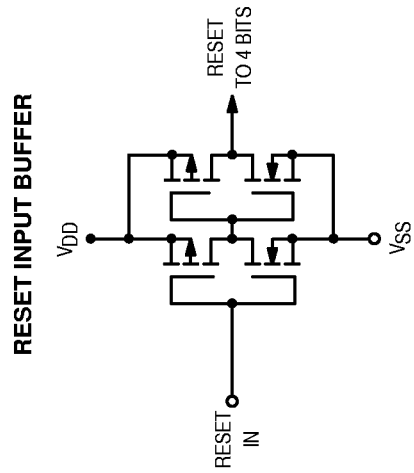
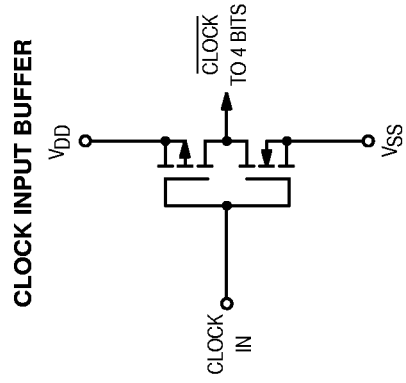
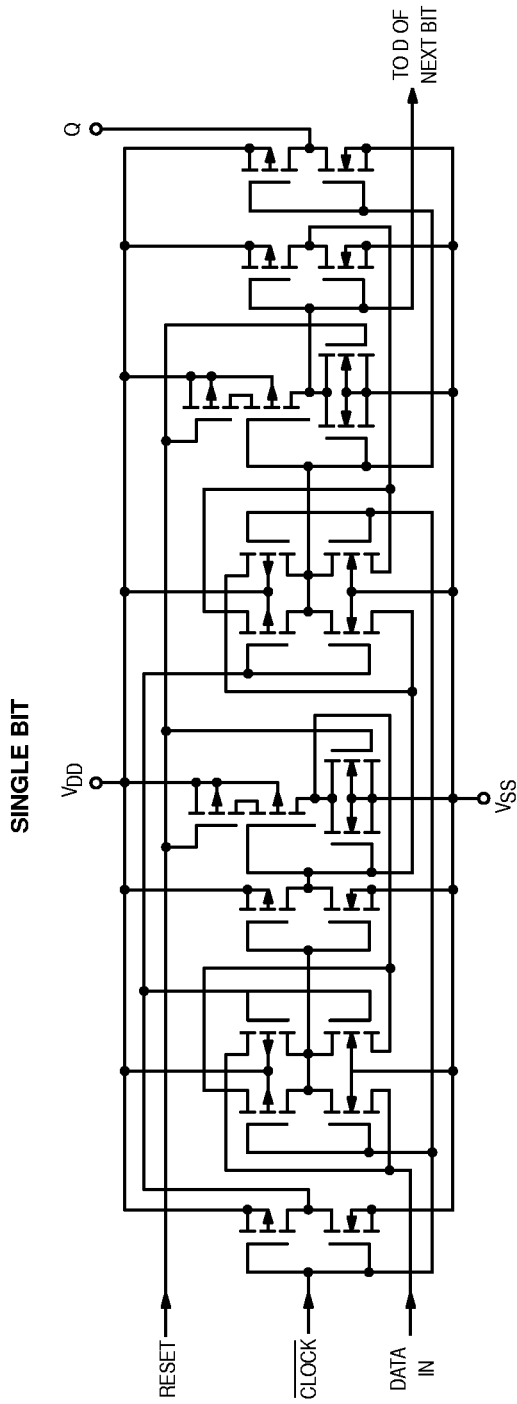


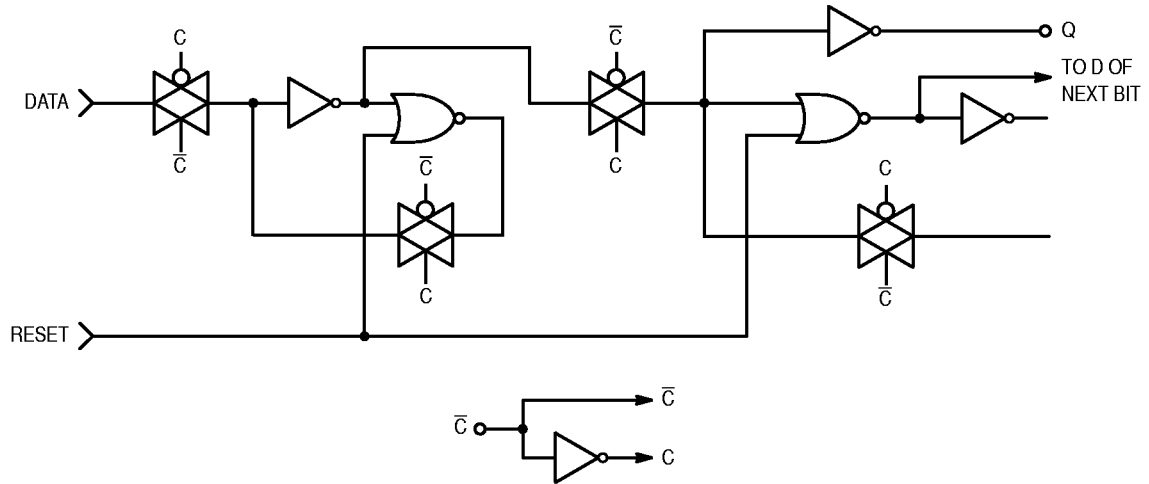
Figure 3. Setup and Hold Time Test Circuit and Waveforms

CIRCUIT SCHEMATICS

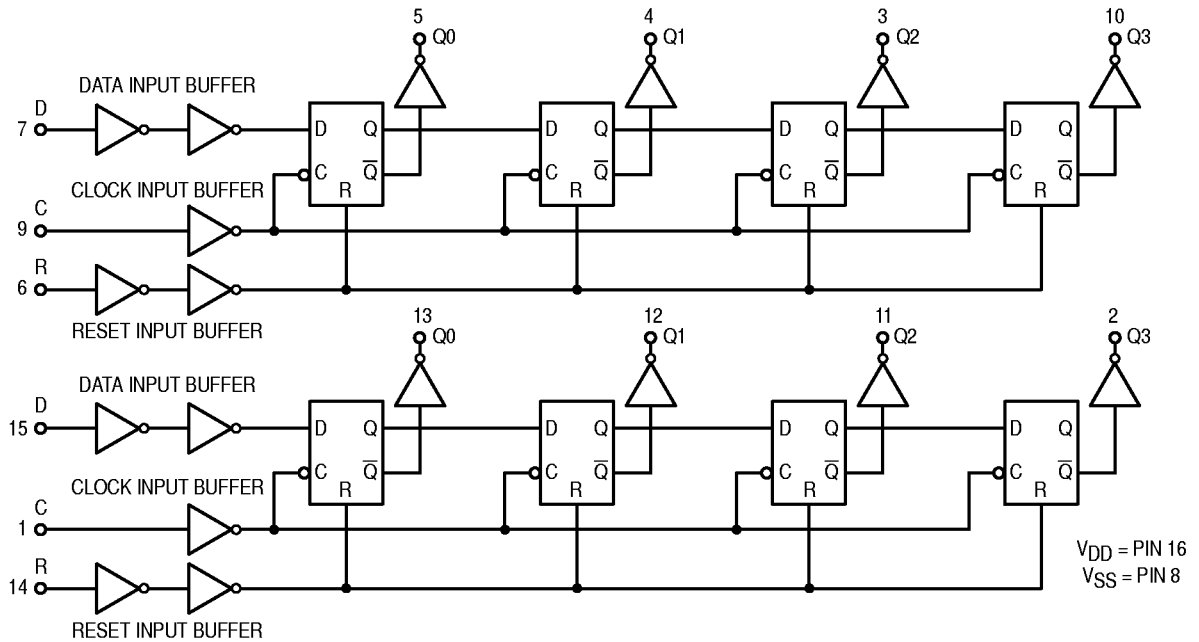


LOGIC DIAGRAMS

SINGLE BIT

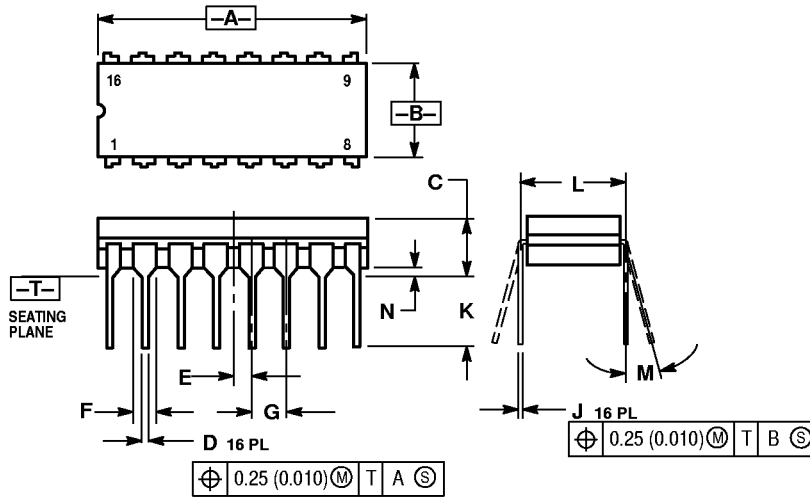


COMPLETE DEVICE



OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

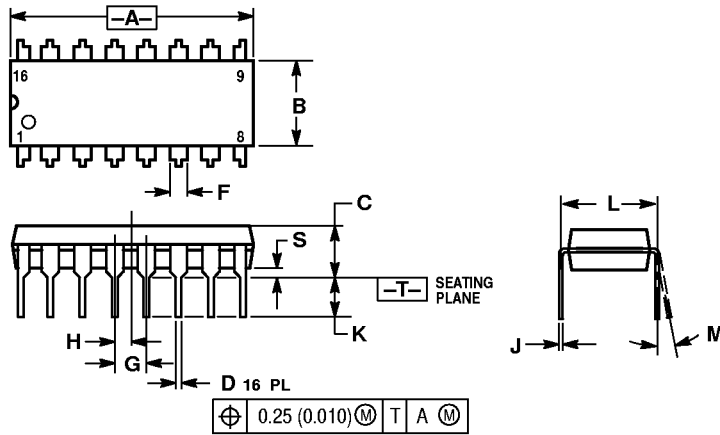


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.750 | 0.785 | 19.05 | 19.93 |
| B | 0.240 | 0.295 | 6.10 | 7.49 |
| C | — | 0.200 | — | 5.08 |
| D | 0.015 | 0.020 | 0.39 | 0.50 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.055 | 0.065 | 1.40 | 1.65 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.125 | 0.170 | 3.18 | 4.31 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° 15° | | 0° 15° | |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



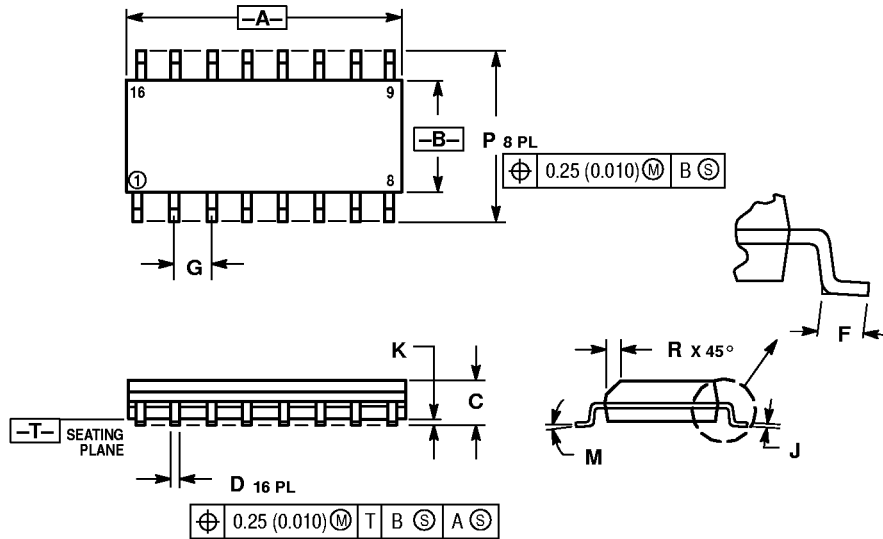
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° 10° | | 0° 10° | |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

OUTLINE DIMENSIONS


D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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MC14015B/D

