μA9706 • μA9706A

MULTI-CHANNEL, 12-BIT ACCURATE, μP COMPATIBLE, D/A CONVERTERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

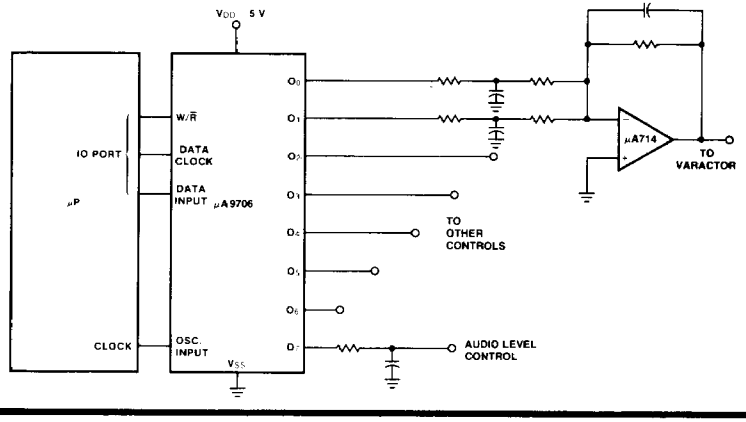
GENERAL DESCRIPTION — The μA9706 and μA9706A are digital-to-analog-converters which allow a microprocessor system to interface and control analog systems. The μA9706 is programmed by 9-bit words, accepted in a serial format, while the μA9706A accepts 9-bit words in parallel 3-bit groups. Both the μA9706 and μA9706A provide conversions on all channels simultaneously and continuously as long as the oscillator signal is present. Digital-to-analog conversion is accomplished using a pulse-width ratio technique for directly controlling the duty cycle of the output pulse streams. Each channel, when appropriately filtered, supplies 6-bit resolution, or 64 discrete analog levels. By properly summing two outputs, the resolution may be controlled up to 12 bits, or 4096 discrete levels. The μA9706 provides 8-channel operation, whereas the μA9706A provides 7-channel operation. Each channel output maintains 12-bit, or ±.01% full-scale, accuracy.

- **MICROPROCESSOR COMPATIBLE**
- **CMOS TECHNOLOGY**
- **LOW COST**
- **8 CHANNELS (μA9706), 7 CHANNELS (μA9706A)**
- **LINEARITY ±0.01%**
- **EXPANDABLE TO 12-BIT RESOLUTION**
- **INTERNAL MEMORY**
- **SINGLE SUPPLY (+5 V)**
- **EXCELLENT STABILITY — NO ADJUSTMENTS**
- **SUITED FOR BUS ORIENTED APPLICATIONS**
  μA9706 — SERIAL INPUT FORMAT
  μA9706A — PARALLEL INPUT FORMAT

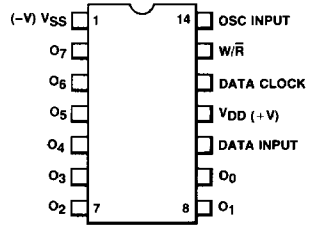
APPLICATIONS

- **Remote Control TV — Tuning, Volume, Color Contrast, Intensity, Hue**
- **Remote Control Audio Systems — Stereo Quadraphonic**
- **Microprocessor Control Systems — Games, Toys Appliances Automotive Industrial Processes Instrumentation**

VARACTOR TUNED 12-BIT RECEIVER SYSTEM



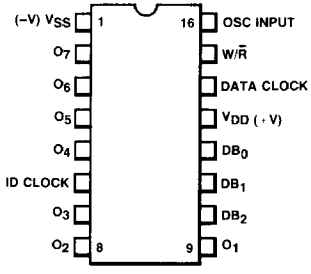
CONNECTION DIAGRAM
μA9706
14-PIN DIP PACKAGE
(TOP VIEW)
PACKAGE OUTLINES 7A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA9706	μA9706PC
μA9706	μA9706DC

CONNECTION DIAGRAM
μA9706A
16-PIN PACKAGE
(TOP VIEW)
PACKAGE OUTLINES 7B 9B
PACKAGE CODES D P

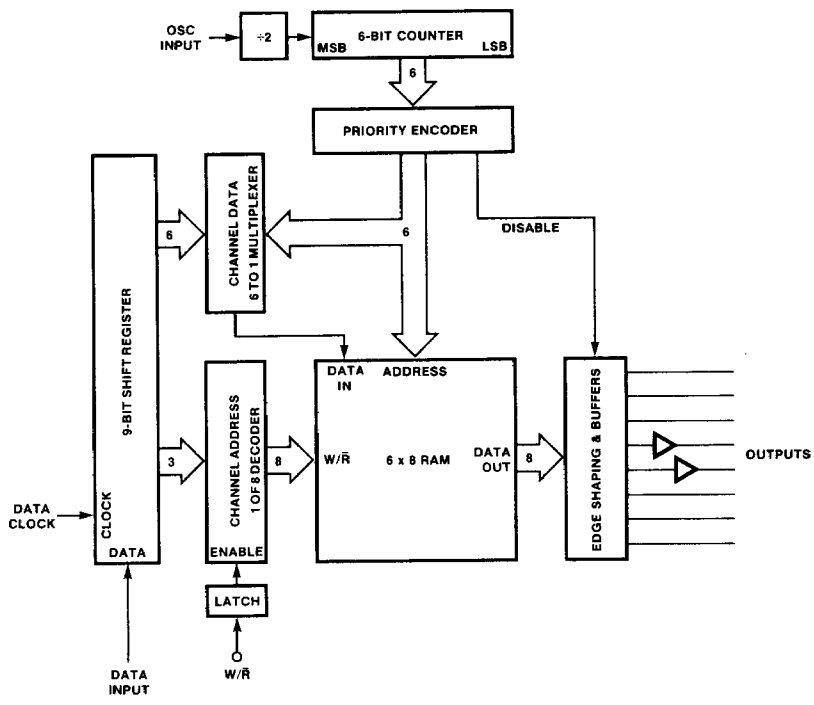


ORDER INFORMATION

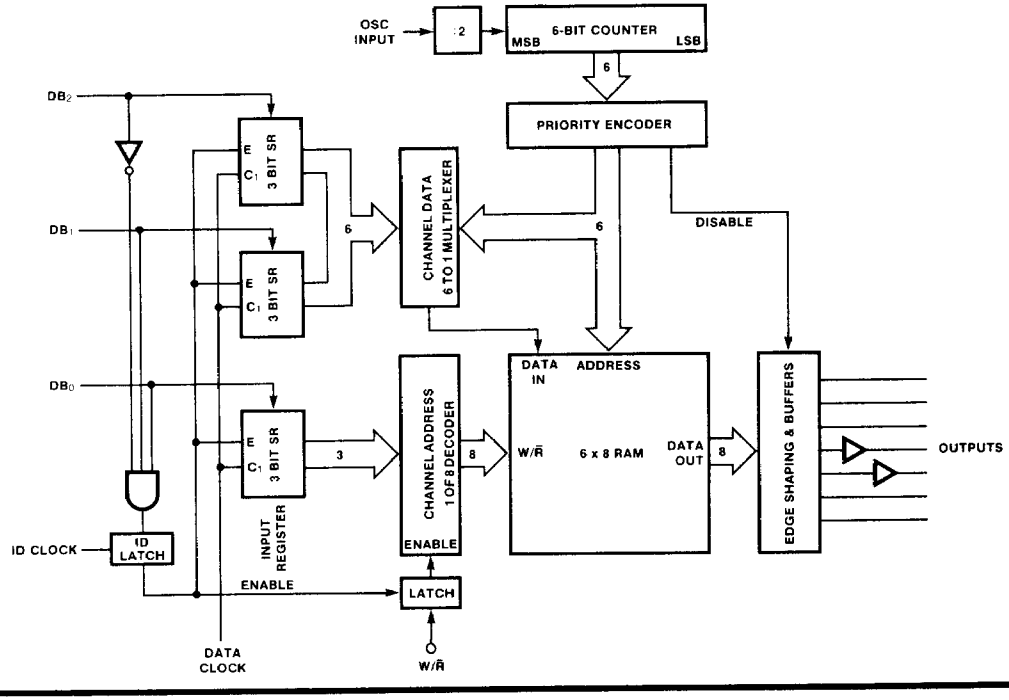
TYPE	PART NO.
μA9706A	μA9706APC
μA9706A	μA9706ADC

FUNCTIONAL DIAGRAMS

μA9706



μA9706A



ABSOLUTE MAXIMUM RATINGS

V_{DD} Relative to V_{SS}	−0.3 V to 5.5 V
Digital Input Range	−0.3 V to V_{DD} +0.3 V
Output Sink or Source Current	25 mA
Operating Temperature	0°C to 85°C
Storage Temperature	−65°C to +150°C
Pin Temperature (Soldering, 10 s)	260°C

ELECTRICAL CHARACTERISTICS: V_{DD} = +5 V, V_{SS} = 0 V, T_A = 0°C to +70°C, f_{osc} = 100 kHz

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS
R_O	Output Resistance (Channels 4 & 5)		30	50	Ω
R_O	Output Resistance (Channels 0, 1, 2, 3, 6, 7)		300	1000	Ω
f_{osc}	Oscillator Frequency	50		2000	kHz
t_H	Data Clock HIGH Time	4			μs
t_L	Data Clock LOW Time	4			μs
$t_{W/\overline{R}}$	W/$\overline{R}$ Pulse Width	4		$128/f_{osc}$	μs
Error	Linearity			0.01	%
V_{IH}	Voltage Input HIGH			2.7	V
V_{IL}	Voltage Input LOW	0.8			V
I_{DD}	Power Supply Current		40	200	μA
I_{IN}	Input Current			50	μA
C_{IN}	Input Capacitance		8		pF
t_r	Input Rise Time			1.0	μs
t_f	Input Fall Time			1.0	μs
t_S	Input Set-up Time			1.0	μs

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FUNCTIONAL DESCRIPTION

The functional blocks of the μA9706 and μA9706A are defined by the pulse-width ratio conversion scheme that they employ. In addition, other requirements which include microprocessor compatibility, multi-channel operation, and simultaneous conversion of all channels add to the basic structure. The μA9706 consists of seven functional blocks: a 6-bit binary counter, a pulse distributor called a priority encoder, 6 x 8 RAM, 1-of-8 channel address decoder, 6-to-1 channel-data multiplexer, 9-bit input shift register, and a set of eight output buffers.

The pulse-width-ratio conversion scheme divides the conversion cycle into binary-weighted time intervals and associates each time interval with a bit position in the 6-bit control word. The control word residing in RAM is then addressed, bit by bit, each bit addressed for the associated time interval. The value of each bit, "1" or "0", controls the output, HIGH or LOW, during this time interval *(see Figure 1)*. In this manner, an output pulse stream is generated with a duty cycle defined by the control word. When the pulse stream is filtered, a dc value is extracted that is proportional to the duty cycle of the pulse stream and, hence, proportional to the control word.

The 6-bit counter generates the fundamental time intervals for the system and may be driven by any open-collector TTL or CMOS logic that produces a square-wave signal with a frequency in the range of 50 kHz to 2 MHz. The time intervals (binary-weighted pulse widths) generated by the counter are decoded by the priority encoder which serves two functions. First, it ensures that each of the six time intervals (control pulses) is used once during the conversion cycle. Second, it distributes the control pulses to both the channel-data multiplexer and to the column-address inputs of the 6 x 8 RAM.

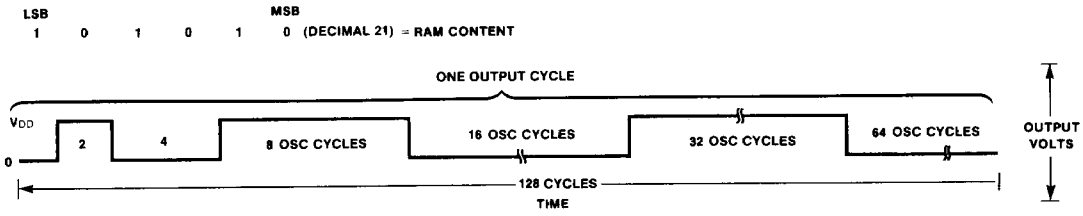


Fig. 1 Output Cycle Example

The channel-data multiplexer is enabled during the write mode so that the 6-bit control word may be written. The 6 x 8 RAM provides the storage capability required for the converter to operate independently of the microprocessor, once the control information has been transferred. Since the control information is stored in RAM, simultaneous conversions continue on all eight channels, unaided by the microprocessor unless changes are required. This is accomplished by addressing a single bit in each of the control words and reading the results out in parallel during each time interval in the conversion cycle. The total cycle time, which is the sum of the six binary-weighted time intervals plus a unit interval (64 clock periods), requires 128 oscillator periods, since the basic oscillator frequency is divided by a factor of two before driving the counter. Conversions may be completed in as little as 64 μs when operating at a 2 MHz clock rate. The control words read from the RAM are directed to the output buffers, six of which have 1 kΩ and two have 50 Ω output impedances. In general, these buffers should drive load impedances larger than the output impedance to reduce the errors caused by the finite output impedance.

Each output is capable of providing 64 discrete output levels representing 6-bit resolution. Since each output pulse stream is accurate to 12 bits, it is possible to sum two outputs and expand the resolution to 12 bits, providing 4096 discrete output levels. This may be easily accomplished by weighting one of the outputs by a factor of 1/64 before summing.

Loading data is a simple procedure that does not affect the conversion cycle. For the μA9706, the 6-bit control word (channel data) and the 3-bit channel address are serially transferred to the 9-bit shift register on the HIGH-to-LOW transitions of the data clock *(Figure 2)*. The data clock has a maximum frequency of 125 kHz with a minimum HIGH and LOW time of 4 μs. Once the nine bits of data have been transferred into the shift register, the data clock must remain static until the write operation is completed to prevent the data from being shifted out of the register. The write mode may be selected after a minimum setup time of 1 μs and is enabled by a HIGH-going $W/\overline{R}$ control pulse. This sets an internal latch that enables the channel-address decoder, which decodes the 3-bit binary channel address, therefore effecting the transfer of the 6-bit control word from the input register to RAM via the channel-data multiplexer at the beginning of the next conversion cycle. The $W/\overline{R}$ pulse has two restrictions: first, it must be equal to or greater than 4 μs in duration; second, it must be less than $128/f_{OSC}$. This latter restriction is necessary to eliminate the possibility of multiple loads occurring from a single $W/\overline{R}$ pulse that could lead to incorrect control-word transfers under certain conditions.

The μA9706A is basically the same as the μA9706 except for two differences: input structure and pin limitation. The μA9706A has three 3-bit shift registers, used for temporary storage of the 3-bit channel address and 6-bit control word. This structure is bus oriented and provides for parallel 3-bit transfers between the microprocessor and the converter *(Figure 3)*. Also, before any transfers can take place, a 3-bit ID code must be accepted. The ID code is provided in parallel over the ID clock and DB_0, DB_1 and DB_2 inputs. After the nine bits of data are transferred to the shift registers, the operation of the μA9706A is identical to the μA9706. The μA9706A provides 7-channel operation as opposed to the 8-channel operation of the μA9706.

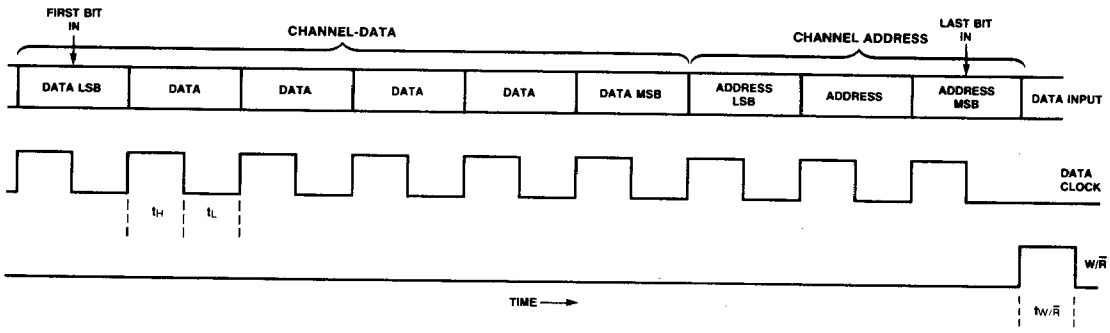


Fig. 2 μA9706 Input Timing and Format

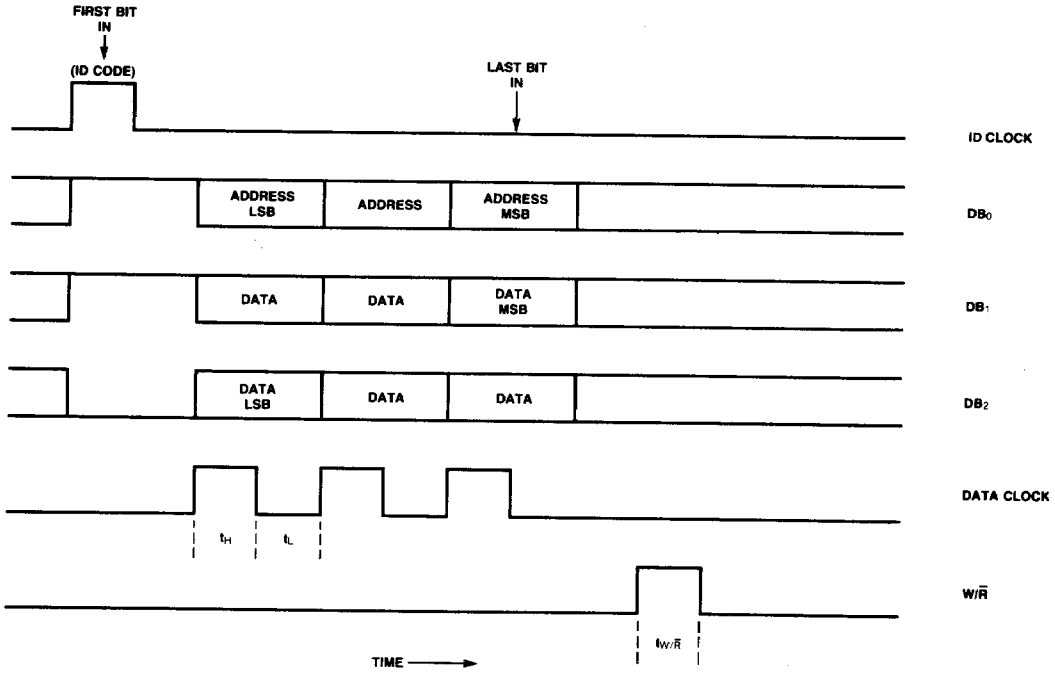
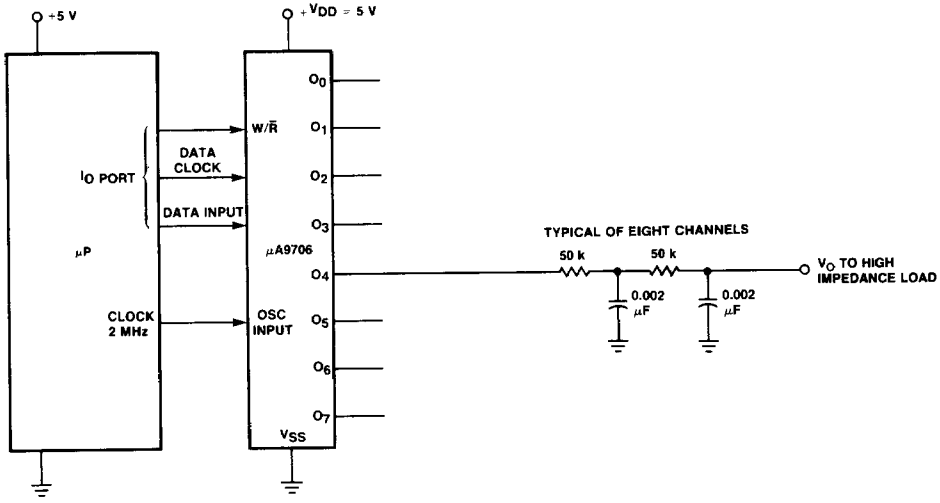


Fig. 3 μA9706A Input Timing and Format

TYPICAL μA9706 SYSTEM



μA9706 F8 OBJECT CODE SUBROUTINE

enter with R_0 = data to be output to 9706
R_1 = address to be output to 9706

entry = H'100'

F8 Object Code

```
M100-130
M0100=20   20 52 20 04 53 20 07
M0108=B0   20 0F B0 40 22 FE 18
M0110=24   0C B0 24 02 B0 40 12
M0118=50   42 12 52 94 EF 41 50
M0120=43   52 70 51 53 40 18 18
M0128=94   E3 20 0B B0 20 0F B0
M0130=1C
```

Port 0 bit 0 = Data Input
Port 0 bit 1 = Data Clock
Port 0 bit 2 = W/$\overline{R}$
Port 0 bit 3 = Scope Trigger

Exit = return, destroyed R_0, R_1, R_2, R_3, Acc

μA9706A F8 OBJECT CODE SUBROUTINE

enter with R_0 = data to be output to 9706A
R_1 = address to be output to 9706A

entry = H'100'

F8 Object Code

```
M100-16D
M0100=20   61 52 53 54 40 18 50
M0108=41   18 51 20 01 F1 13 C2
M0110=52   20 02 F1 C3 53 20 04
M0118=F1   12 C4 54 20 01 F0 13
M0120=13   13 C2 52 20 02 F0 13
M0128=13   C3 53 20 04 F0 13 C4
M0130=54   20 08 F0 12 C2 52 20
M0138=10   F0 12 12 C3 53 20 20
M0140=F0   12 12 12 C4 54 20 3F
M0148=B0   20 7F B0 20 78 B0 20
M0150=79   B0 42 B0 20 10 C2 B0
M0158=43   B0 20 10 C3 B0 44 B0
M0160=20   10 C4 B0 20 7F B0 20
M0168=5F   B0 20 7F B0 1C
```

Port 0 bit 0 = ID clock
Port 0 bit 1 = DB_0
Port 0 bit 2 = DB_1
Port 0 bit 3 = DB_2
Port 0 bit 4 = data clock
Port 0 bit 5 = W/$\overline{R}$
Port 0 bit 6 = scope trigger

Exit = return, destroyed R_0, R_1, R_2, R_3, R_4, Acc