FAIRCHILD
A Schlumberger Company

F6820
Peripheral Interface Adapter (PIA)

Microprocessor Product

Description

The F6820* Peripheral Interface Adapter (PIA) provides the universal means of interfacing peripheral equipment to the F6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

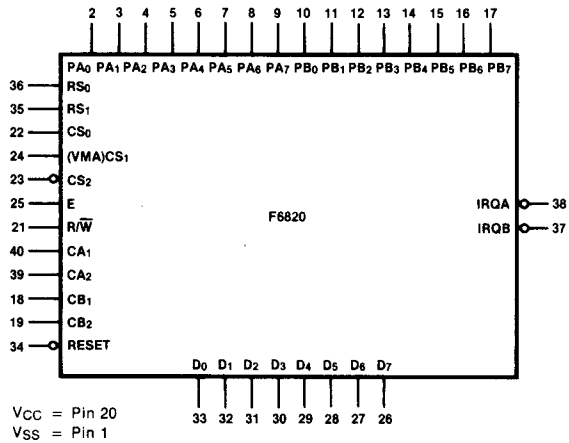
The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

- **8-Bit Bidirectional Data Bus for Communication with the MPU**
- **Two Bidirectional 8-Bit Buses for Interface to Peripherals**
- **Two Programmable Control Registers**
- **Two Programmable Data Direction Registers**
- **Four Individually Controlled Interrupt Input Lines, Two Usable as Peripheral Control Outputs**
- **Handshake Control Logic for Input and Output Peripheral Operation**
- **High-Impedance 3-State and Direct Transistor Drive Peripheral Lines**
- **Program-Controlled Interrupt and Interrupt Disable Capability**
- **CMOS Drive Capability on Side A Peripheral Lines**

Pin Names

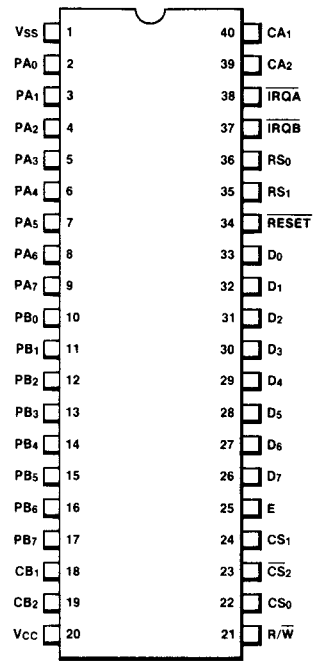
D_0-D_7	Bidirectional Data Bus
PA_0-PA_7	Bidirectional Peripheral Data Bus A
PB_0-PB_7	Bidirectional Peripheral Data Bus B
CS_0, CS_1, $\overline{CS_2}$	Chip Select Inputs
RS_0, RS_1	Register Select Inputs
E	Enable Input
R/$\overline{W}$	Read/Write Input
$\overline{RESET}$	Reset Input
CA_1, CB_1	Interrupt Control Inputs
CA_2, CB_2	Programmable Interrupt Control Input or Peripheral Control Output
$\overline{IRQA}$, $\overline{IRQB}$	Interrupt Request Outputs

Logic Symbol



V_{CC} = Pin 20
V_{SS} = Pin 1

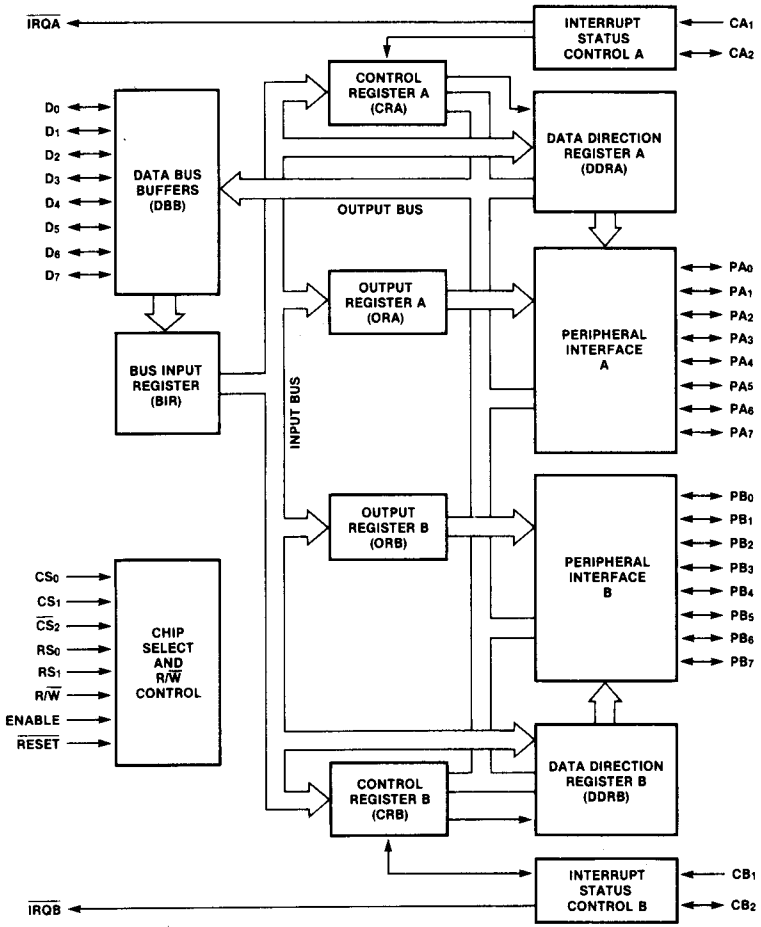
Connection Diagram
40-Pin DIP



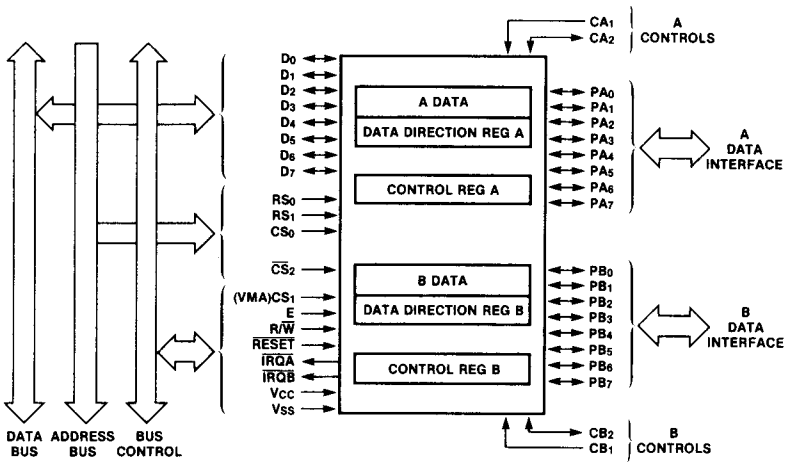
(Top View)

* Not recommended for new designs.

Block Diagram



F6820 PIA Bus Interface



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Functional Description

PIA Interface Signals for MPU
The PIA interfaces to the F6800 MPU with an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, a read/write line, an enable line, and a reset line. These signals, in conjunction with the F6800 VMA output, permit the MPU to have complete control over the PIA. The VMA signal should be utilized in conjunction with an MPU address line into a chip select of the PIA.

PIA Bidirectional Data (D_0-D_7), Pins 26-33 — The bidirectional data lines (D_0-D_7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are 3-state devices that remain in the high-impedance (OFF) state except when the MPU performs a PIA read operation. The read/write line is in the read (HIGH) state when the PIA is selected for a read operation.

PIA Enable (E), Pin 25 — The enable (E) pulse is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal is normally a derivative of the F6800 $\phi 2$ clock.

PIA Read/Write (R/$\overline{W}$), Pin 21 — This signal is generated by the MPU to control the direction of data transfers on the data bus. A LOW on the PIA read/write line enables the input buffers, and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A HIGH on the read/write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the E pulse are present.

$\overline{\text{RESET}}$, Pin 34 — The active-LOW $\overline{\text{RESET}}$ line is used to reset all register bits in the PIA to a logic 0 (LOW). This line can be used as a power-on reset and as a master reset during system operation.

PIA Chip Select (CS_0, CS_1, and $\overline{CS_2}$), Pins 22-24 — These three input signals are used to select the PIA. CS_0 and CS_1 must be HIGH and $\overline{CS_2}$ must be LOW for selection of the device. Data transfers are then performed under the control of the enable and read/write signals. The chip select lines must be stable for the duration of the E pulse. The device is "deselected" when any of the chip selects are in the inactive state.

PIA Register Select (RS_0 and RS_1), Pins 35, 36 — The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal control registers to select a particular register that is to be written to or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

Interrupt Request ($\overline{IRQA}$ and $\overline{IRQB}$), Pins 37, 38 — The active-LOW interrupt request lines act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are open drain (no-load device on the chip). This permits all interrupt request lines to be tied together in a wired-OR configuration.

Each interrupt request line has two internal interrupt flag bits that can cause either line to go LOW. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA that are used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU is accomplished by a software routine that, on a priority basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (set to 0) as a result of an MPU read peripheral data operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled until the PIA is "deselected"during an E pulse. The E pulse is used to condition the interrupt control lines (CA_1, CA_2, CB_1, CB_2). When these lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag is set on the next active transition of the interrupt input pin.

PIA/Peripheral Interface Lines

The PIA provides two 8-bit bidirectional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA_0-PA_7), Pins 2-9 — Each of the peripheral data lines is programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding data direction register bit for those lines which are to be outputs. A "0" in a bit of the data direction register causes the corresponding peripheral data line to act as an input. During an MPU read peripheral data operation, the data on peripheral data lines programmed to act as inputs appears directly on the corresponding MPU data bus lines. In the input mode, the internal pull-up resistor on these lines represents a maximum of one standard TTL load.

The data in output register A appears on the data lines that are programmed to be outputs. A logic "1" written into the register causes a HIGH on the corresponding data line, while a "0" results in a LOW. Data in output register A may be read by an MPU read peripheral data A operation when the corresponding lines are programmed as outputs. This data is read properly if the voltage on the peripheral data lines is greater than 2.0 V for a logic "1" output and less than 0.8 V for a logic "0" output. Loading the output lines so that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a read operation to differ from that contained in the respective bit of output register A.

Section B Peripheral Data (PB_0-PB_7), Pins 10-17 — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA_0-PA_7. However, the output buffers driving these lines differ from those driving lines PA_0-PA_7. They have 3-state capability, allowing them to enter a high-impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB_0-PB_7 is read properly from those lines programmed as outputs even if the voltages are below 2.0 V for a HIGH. As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 mA at 1.5 V to drive the base of a transistor switch directly.

Interrupt Input (CA_1 and CB_1), Pins 18, 40 — Interrupt input lines CA_1 and CB_1 are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA_2), Pin 39 — The peripheral control line CA_2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input, the internal pull-up resistor on this line represents one standard TTL load. The function of this signal line is programmed with control register A.

Peripheral Control (CB_2), Pin 19 — Peripheral control line CB_2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output, it is compatible with standard TTL and may also be used as a source of up to

1 mA at 1.5 V to drive the base of a transistor switch directly. This line is programmed by control register B.

Note
It is recommended that the control lines (CA_1, CA_2, CB_1, CB_2) should be held in a logic "1" state when $\overline{RESET}$ is active to prevent setting of corresponding interrupt flags in the control register when $\overline{RESET}$ goes to an inactive state. Subsequent to $\overline{RESET}$ going inactive, a read of the data registers may be used to clear any undesired interrupt flags.

Internal Controls
There are six locations within the PIA accessible to the MPU data bus: two peripheral registers, two data direction registers, and two control registers. Selection of these locations is controlled by the RS_0 and RS_1 inputs together with bit 2 in the control register, as shown in *Table 1*.

Table 1 Internal Addressing

RS_1	RS_0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

Initialization
A LOW $\overline{RESET}$ line has the effect of zeroing all PIA registers. This sets PA_0-PA_7, PB_0-PB_7, CA_2 and CB_2 as inputs, with all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Possible configurations of the data direction and control registers are as follows.

Data Direction Registers (DDRA and DDRB)
The two data direction registers allow the MPU to control the direction of data through each corresponding peripheral data line. A data direction register bit set at "0" configures the corresponding peripheral data line as an input; a "1" results in an output.

Control Registers (CRA and CRB)
The two control registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA_1, CA_2, CB_1 and CB_2. In addition, they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers are written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA_1, CA_2, CB_1 or CB_2. The format of the control words is shown in *Table 2*.

Table 2 Control Word Format

Bit	CRA	CRB
7	IRQA1	IRQB1
6	IRQA2	IRQB2
5 4 3	CA_2 Control	CB_2 Control
2	DDRA Access	DDRB Access
1 0	CA_1 Control	CB_1 Control

Data Direction Access Control Bit (CRA-2 and CRB-2) — Bit 2 in each control register (CRA and CRB) allows selection of either a peripheral interface register or the data direction register when the proper register select signals are applied to RS_0 and RS_1.

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) — The four interrupt flag bits are set by active transitions of signals on the four interrupt and peripheral control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU data bus and are reset indirectly by a read peripheral data operation on the appropriate section.

Control of CA_1 and CB_1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) — The two lowest order bits of the control registers are used to control the interrupt input lines CA_1 and CB_1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals IRQA and IRQB, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA_1 and CB_1 (see *Table 3*).

Control of CA_2 and CB_2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4 and CRB-5) — Bits 3, 4 and 5 of the two control registers are used to control the CA_2 and CB_2 peripheral control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is LOW, CA_2 (CB_2) is an interrupt input line similar to CA_1 (CB_1) (see *Table 4*). When CRA-5 (CRB-5) is HIGH, CA_2 (CB_2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA_2 and CB_2 have slightly different characteristics (see *Tables 5* and *6*).

Table 3 Control of Interrupt Inputs CA_1 and CB_1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA_1 (CB_1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set HIGH on ↓ of CA_1 (CB_1)	Disabled — $\overline{IRQA}$ ($\overline{IRQB}$) remains HIGH
0	1	↓ Active	Set HIGH on ↓ of CA_1 (CB_1)	Goes LOW when the interrupt flag bit CRA-7 (CRB-7) goes HIGH
1	0	↑ Active	Set HIGH on ↑ of CA_1 (CB_1)	Disabled — $\overline{IRQA}$ ($\overline{IRQB}$) remains HIGH
1	1	↑ Active	Set HIGH on ↑ of CA_1 (CB_1)	Goes LOW when the interrupt flag bit CRA-7 (CRB-7) goes HIGH

Notes

1. ↑ indicates positive transition (LOW-to-HIGH)
2. ↓ indicates negative transition (HIGH-to-LOW)
3. The interrupt flag bit CRA-7 is cleared by an MPU read of the A data register, and CRB-7 is cleared by an MPU read of the B data register.
4. If CRA-0 (CRB-0) is LOW when an interrupt occurs (interrupt disabled) and is later brought HIGH, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-0 (CRB-0) is written to a "1".

Table 4 Control of CA_2 and CB_2 as Interrupt Inputs

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA_2 (CB_2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set HIGH on ↓ of CA_2 (CB_2)	Disabled — $\overline{IRQA}$ ($\overline{IRQB}$) remains HIGH
0	0	1	↓ Active	Set HIGH on ↓ of CA_2 (CB_2)	Goes LOW when the interrupt flag bit CRA-6 (CRB-6) goes HIGH
0	1	0	↑ Active	Set HIGH on ↑ of CA_2 (CB_2)	Disabled — $\overline{IRQA}$ ($\overline{IRQB}$) remains HIGH
0	1	1	↑ Active	Set HIGH on ↑ of CA_2 (CB_2)	Goes LOW when the interrupt flag bit CRA-6 (CRB-6) goes HIGH

Notes

1. ↑ indicates positive transition (LOW-to-HIGH)
2. ↓ indicates negative transition (HIGH-to-LOW)
3. The interrupt flag bit CRA-6 is cleared by an MPU read of the A data register, and CRB-6 is cleared by an MPU read of the B data register.
4. If CRA-3 (CRB-3) is LOW when an interrupt occurs (interrupt disabled) and is later brought HIGH, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-3 (CRB-3) is written to a "1".

Table 5 Control of CB_2 as an Output

CRB-5	CRB-4	CRB-3	CB_2	
			Cleared	Set
1	0	0	LOW on the positive transition of the first E pulse following an MPU write "B" data register operation.	HIGH when the interrupt flag bit CRB-7 is set by an active transition of the CB_1 signal.
1	0	1	LOW on the positive transition of the first E pulse after an MPU write "B" data register operation.	HIGH on the positive edge of the first E pulse following an E pulse that occurred while the part was deselected.
1	1	0	LOW when CRB-3 goes LOW as a result of an MPU write in control register "B".	Always LOW as long as CRB-3 is LOW. Goes HIGH on an MPU write in control register "B" that changes CRB-3 to "1".
1	1	1	Always HIGH as long as CRB-3 is HIGH. Cleared when an MPU write control register "B" results in clearing CRB-3 to "0".	HIGH when CRB-3 goes HIGH as a result of an MPU write into control register "B".

Table 6 Control of CA_2 as an Output

CRA-5	CRA-4	CRA-3	CA_2	
			Cleared	Set
1	0	0	LOW on negative transition of E after an MPU read "A" data operation.	HIGH when the interrupt flag bit CRA-7 is set by an active transition of the CA_1 signal.
1	0	1	LOW on negative transition of E after an MPU read "A" data operation.	HIGH on the negative edge of the first E pulse that occurs during a deselect.
1	1	0	LOW when CRA-3 goes LOW as a result of an MPU write to control register "A".	Always LOW as long as CRA-3 is LOW. Goes HIGH on an MPU write to control register "A" that changes CRA-3 to "1".
1	1	1	Always HIGH as long as CRA-3 is HIGH. Cleared on an MPU write to control register "A" that clears CRA-3 to a "0".	HIGH when CRA-3 goes HIGH as a result of an MPU write to control register "A".

Absolute Maximum Ratings

Supply Voltage	−0.3 V, +7.0 V
Input Voltage	−0.3 V, +7.0 V
Operating Temperature Range	0 °C, +70 °C
Storage Temperature Range	−55 °C, +150 °C
Thermal Resistance	82.5 °C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this hig impedance circuit.

DC Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage Enable Other Inputs	 V_{SS} +2.4 V_{SS} +2.0		 V_{CC} V_{CC}	V	
V_{IL}	Input LOW Voltage Enable Other Inputs	 V_{SS} −0.3 V_{SS} −0.3		 V_{SS} +0.4 V_{SS} +0.8	V	
I_{IN}	Input Leakage Current R/$\overline{W}$, $\overline{RESET}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, Enable		1.0	2.5	μA	V_{IN} = 0 to 5.25 V
I_{TSI}	3-State (OFF State) Input Current D_0-D_7, PB_0-PB_7, CB_2		2.0	10	μA	V_{IN} = 0.4 to 2.4 V
I_{IH}	Input HIGH Current PA_0-PA_7, CA_2	−100	−250		μA	V_{IH} = 2.4 V
I_{IL}	Input LOW Current PA_0-PA_7, CA_2		−1.0	−1.6	mA	V_{IL} = 0.4 V
V_{OH}	Output HIGH Voltage D_0-D_7	V_{SS} +2.4			V	I_{Load} = −205 μA, Enable pulse width <25 μs
	Other Outputs	V_{SS} +2.4			V	I_{Load} = −100 μA, Enable pulse width <25 μs
V_{OL}	Output LOW Voltage			V_{SS} +0.4	V	I_{Load} = 1.6 mA, Enable pulse width <25 μs
I_{OH}	Output HIGH Current (Sourcing) D_0-D_7 Other Outputs	 −205 −100			 μA μA	V_{OH} = 2.4 V
	PB_0-PB_7, CB_2	−1.0	−2.5	−10	mA	V_O = 1.5 V, the current for driving other than TTL, e.g., Darling base
I_{OL}	Output LOW Current (Sinking)	1.6			mA	V_{OL} = 0.4 V
I_{LOH}	Output Leakage Current (OFF State) $\overline{IRQA}$, $\overline{IRQB}$		1.0	10	μA	V_{OH} = 2.4 V
P_D	Power Dissipation			650	mW	
C_{IN}	Input Capacitance Enable D_0-D_7 PA_0-PA_7, PB_0-PB_7, CA_2, CB_2 R/$\overline{W}$, $\overline{RESET}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1			 20 12.5 10 7.5	pF	 V_{IN} = 0, T_A = 25°C, f = 1.0 MHz
C_{OUT}	Output Capacitance $\overline{IRQA}$, $\overline{IRQB}$ PB_0-PB_7			 5.0 10	pF	 V_{IN} = 0, T_A = 25°C f = 1.0 MHz

AC Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_{PDSU}	Peripheral Data Set-up Time	200			ns	*Figure 1*
t_{CA2}	Delay Time, Enable Negative Transition to CA_2 Negative Transition			1.0	μs	*Figures 2, 3*
t_{RS1}	Delay Time, Enable Negative Transition to CA_2 Positive Transition			1.0	μs	*Figure 2*
t_r, t_f	Rise and Fall Times for CA_1 and CA_2 Input Signals			1.0	μs	*Figure 3*
t_{RS2}	Delay Time from CA_1 Active Transition to CA_2 Positive Transition			2.0	μs	*Figure 3*
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid			1.0	μs	*Figures 4, 5*
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid PA_0-PA_7, CA_2			2.0	μs	V_{CC} − 30% V_{CC}, *Figure 4;* *Figure 12,* Load C
t_{CB2}	Delay Time, Enable Positive Transition to CB_2 Negative Transition			1.0	μs	*Figures 6, 7*
t_{DC}	Delay Time, Peripheral Data Valid to CB_2 Negative Transition	20			ns	*Figure 5*
t_{RS1}	Delay Time, Enable Positive Transition to CB_2 Positive Transition			1.0	μs	*Figure 6*
t_r, t_f	Rise and Fall Time for CB_1 and CB_2 Input Signals			1.0	μs	*Figure 7*
t_{RS2}	Delay Time, CB_1 Active Transition to CB_2 Positive Transition			2.0	μs	*Figure 7*
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$			1.6	μs	*Figure 8*
t_{RL}	$\overline{RESET}$ LOW Time	2.0			μs	*Figure 9,* Note 1

Note 1. The $\overline{RESET}$ line must be HIGH a minimum of 1.0 μs before addressing the PIA.

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Bus Timing Characteristics

Read *Figures 10* and *12*

Symbol	Characteristic	Min	Typ	Max	Unit
t_{cycE}	Enable Cycle Time	1.0			μs
PW_{EH}	Enable Pulse Width, HIGH	0.45		25	μs
PW_{EL}	Enable Pulse Width, LOW	0.43			μs
t_{AS}	Set-up Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	160			ns
t_{DDR}	Data Delay Time			320	ns
t_H	Data Hold Time	10			ns
t_{AH}	Address Hold Time	10			ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input			25	ns

Write *Figures 11* and *12*

t_{cycE}	Enable Cycle Time	1.0			μs
PW_{EH}	Enable Pulse Width, HIGH	0.45		25	μs
PW_{EL}	Enable Pulse Width, LOW	0.43			μs
t_{AS}	Set-up Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	160			ns
t_{DSW}	Data Set-up Time	195			ns
t_H	Data Hold Time	10			ns
t_{AH}	Address Hold Time	10			ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input			25	ns

Fig. 1 Peripheral Data Set-up Time (Read Mode)

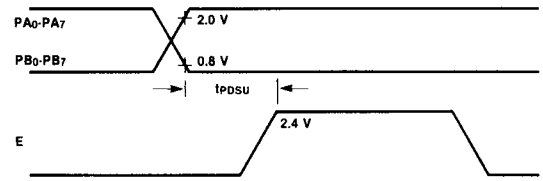
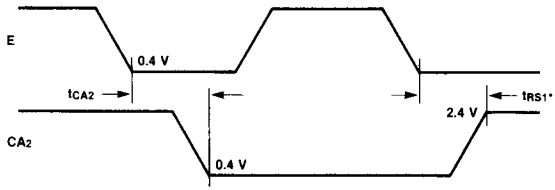


Fig. 2 CA_2 Delay Time (Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during any previous E pulse.

Fig. 3 CA_2 Delay Time (Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

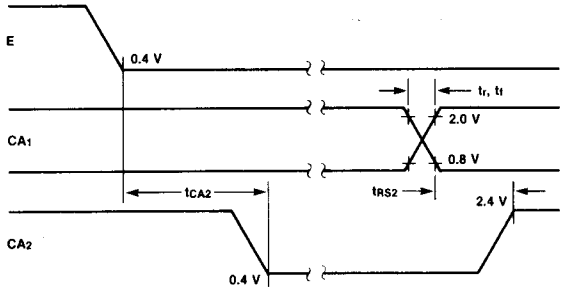


Fig. 4 Peripheral CMOS Data Delay Times (Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

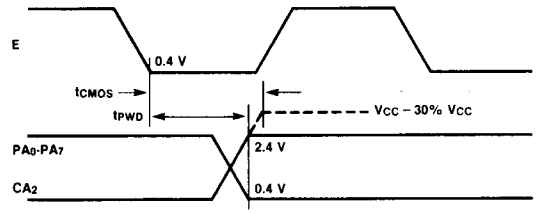
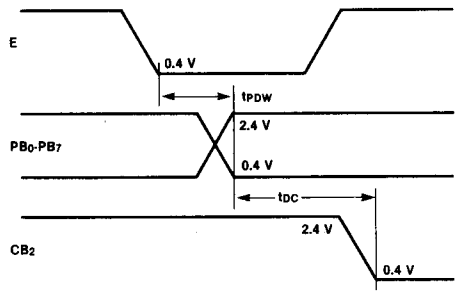
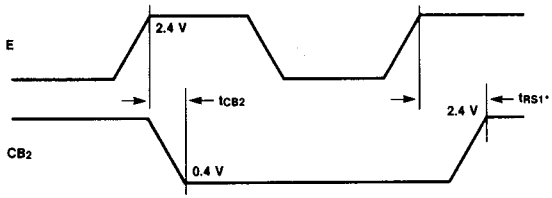


Fig. 5 Peripheral Data and CB_2 Delay Times (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



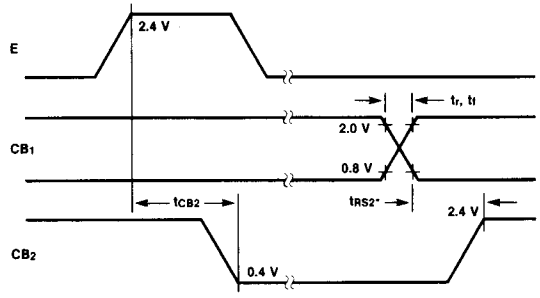
Note CB_2 goes LOW as a result of the positive transition of the E pulse.

Fig. 6 CB_2 Delay Time (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



*Assumes part was deselected during the previous E pulse.

Fig. 7 CB_2 Delay Time (Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during the previous E pulse.

Fig. 8 Interrupt Release Time

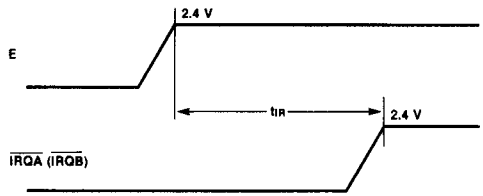
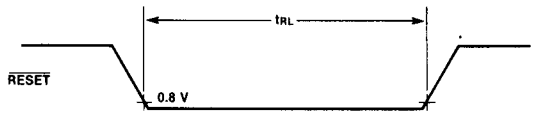


Fig. 9 $\overline{\text{RESET}}$ LOW Time



*The $\overline{\text{RESET}}$ line must be at V_{IH} for a minimum of 1.0 μs before addressing the PIA.

Fig. 10 Bus Read Timing Characteristics (Read Information from PIA)

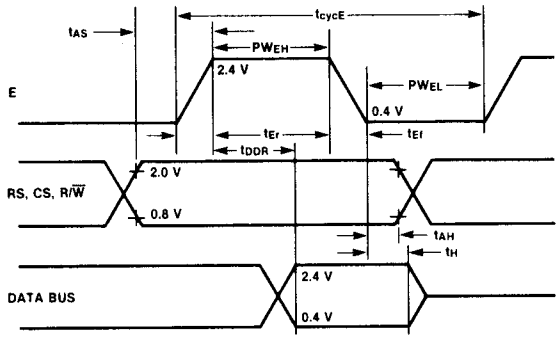


Fig. 11 Bus Write Timing Characteristics (Write Information into PIA)

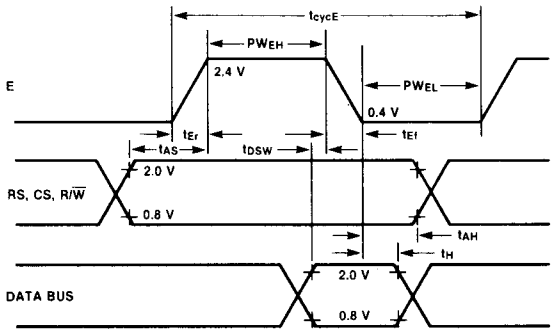
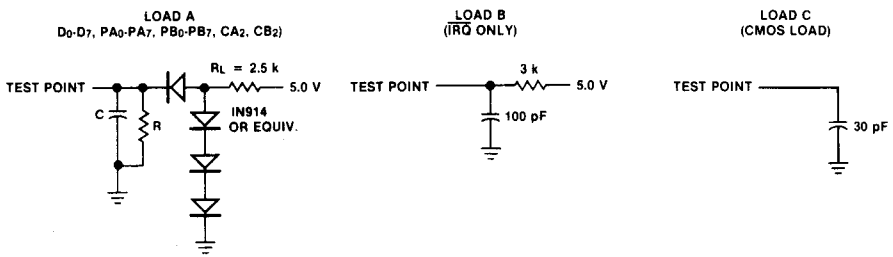


Fig. 12 Bus Timing Test Loads



C = 130 pF for D_0-D_7
= 30 pF for PA_0-PA_7, PB_0-PB_7, CA_2, and CB_2
R = 11.7 kΩ for D_0-D_7
= 24 kΩ for PA_0-PA_7, PB_0-PB_7, CA_2 and CB_2

Ordering Information

Speed	Order Code	Temperature Range
1.0 MHz	F6820P,S	0 °C to + 70 °C

P = Plastic DIP S = Ceramic DIP