MICRO NETWORKS

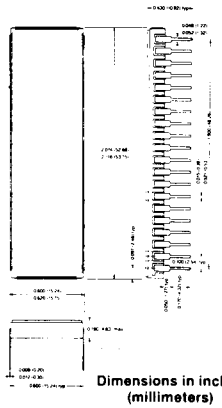
MN7450
MN7451

8-CHANNEL 16-Bit
DATA ACQUISITION SYSTEM

FEATURES

- **Complete DAS:**
  - **Latched Input MUX**
  - **Software Programmable Gain Amplifier**
  - **Buffer Amplifier**
  - **Inherent T/H Function**
  - **Internal Reference**
  - **Internal Clock Option**
  - **16-Bit Self-Calibrating A/D Converter**
- **Small Double-Wide 40-Pin DIP**
- **8X2 Byte Output Format**
- **8 Single-Ended Input Channels**
- **Input Over-Voltage Protection**
- **Full Digital Control:**
  - **MUX Channel**
  - **Gain Range**
  - **Unipolar/Bipolar**
- **Low Initial Gain and Offset Error**

40 PIN SIDE BRAZED DIP



Dimensions in inches (millimeters)

DESCRIPTION

The MN7450 and MN7451 are self-calibrating 8-channel, 16-bit data acquisition systems offered in a small, industry-standard, 40-pin, double-wide dual-in-line package. These units are complete, single-package data acquisition components and contain an input multiplexer, software programmable gain amplifier, input buffer and a 16-bit self-calibrating sampling A/D converter.

The multiplexer features eight single-ended, over-voltage-protected input channels whose latched address inputs are both TTL and CMOS logic compatible. In addition, the input multiplexer features break-before-make operation. The software-programmable gain amplifier features latched selections of gain (1,2,4 or 8) without the need for additional external components. The A/D converter section of this complete DAS features self-calibration and completeness of function. Features include an on-board user-optional internal clock, analog input buffer amplifier, internal reference and data output demultiplexer (8 x 2 output format).

These devices guarantee 16-bit no-missing-codes performance at 25°C and 15-bit no-missing codes over temperature. Gain error is specified as ±0.1% maximum while initial zero errors are specified as ±0.05%FSR maximum (after initial self-calibration). The system can be operated in two modes. In the pipelined mode, signal acquisition is accomplished during the conversion cycle. Maximum throughput in this mode of operation is 47.65kHz. In the non-pipelined mode, analog input channels are selected and then converted in a serial fashion. Throughput in the non-pipelined mode is 17.5kHz.

The small size and completeness of function of the MN7450 and MN7451 make them ideal for applications in high-end industrial and military/aerospace applications where size and performance are paramount considerations. These devices are available with optional Environmental Stress Screening. Contact the factory for availability of MIL-H-38534 compliant devices.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN7450/7451 8-CHANNEL 16-BIT DATA ACQUISITION SYSTEM

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN7450, MN7450J, K	0°C to 6+70°C
MN7450, MN7451S, T	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
$+V_{CC}$ Supply (Pin 13)	0 to +18V
$-V_{CC}$ Supply (Pin 14)	0 to −18V
$+V_{DD}$ Supply (Pin 35)	−0.3 to +6 Volts
$-V_{DD}$ Supply (Pin 37)	+0.3 to −6 Volts
Analog Inputs	$\pm V_{CC}$ ±2 Volts
Digital Inputs	−0.3 to $+V_{DD}$ +0.3 Volts

ORDERING INFORMATION

PART NUMBER **MN7450 T / B CH**

Select MN7450 (0 to +5V, ±5V) or MN7451 (0 to +10V, ±10V).
Select suffix J, K, S, or T for desired performance and specified temperature range.
Add /B to S or T models for Environmental Stress Screening.
Add "CH" to "S/B" or "T/B" models for 100% screening according to MIL-H-38534.
Contact factory for availability of "CH" device types.

DESIGN SPECIFICATIONS ALL UNITS (T_A = +25°C, $\pm V_{CC}$ = ±15V, $\pm V_{DD}$ = ±5V, F_{CLK} = 4MHz (EXTERNAL) unless otherwise indicated) (Note 1)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Input Channels		8 Single-Ended		
Input Voltage Range: MN7450: Unipolar Bipolar MN7451: Unipolar Bipolar		 0 to +5 ±5 0 to +10 ±10		 Volts Volts Volts Volts
Input Bias Current			±10	nA
Input Leakage Current		±1		nA
DIGITAL INPUTS				
Logic Levels: Logic "1" Logic "0"	+2.0		 +0.4	Volts Volts
Logic Currents: Logic "1" (V_{IH} = +2.4V) Logic "0" (V_{IL} = +0.4V)			±10 ±10	µA µA
DIGITAL OUTPUTS				
Output Coding: Unipolar Ranges Bipolar Ranges		Straight Binary Offset Binary		
Logic Levels: Logic "1" (I_{OH} = −40µA) Logic "0" (I_{OL} = +1.6mA)	+2.4		 +0.4	Volts Volts
3-State Output Leakage			±10	µA
REFERENCE OUTPUT				
Reference Voltage	+4.45	+4.5	+4.55	Volts
POWER SUPPLY REQUIREMENTS				
Power Supply Range: $\pm V_{CC}$ Supplies $\pm V_{DD}$ Supplies	±14.55 ±4.5	±15 ±5	±15.45 ±5.5	Volts Volts
Power Supply Rejection Ratio: $\pm V_{CC}$ Supplies $\pm V_{DD}$ Supplies			±0.001 ±0.001	%FSR/%VS %FSR/%VS
Current Drains: $+V_{CC}$ Supply $-V_{CC}$ Supply $+V_{DD}$ Supply $-V_{DD}$ Supply		+18 −17 +13.5 −13.5	+25 −25 +20 −20	mA mA mA mA
Power Consumption		658	950	mW
DYNAMIC CHARACTERISTICS				
Conversion Time Throughput Rate	 47.5	 50	16.5	µsec kHz

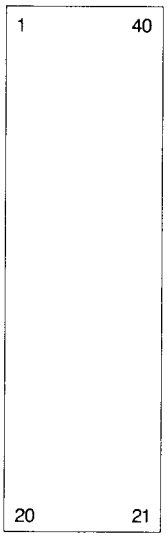
PERFORMANCE SPECIFICATIONS (T_A = +25°C, $\pm V_{CC}$ = ±15V, $\pm V_{DD}$ = ±5V, F_{CLK} = 4MHz unless otherwise indicated)

MODEL	MN7450J MN7451J	MN7450K MN7451K	MN7450S MN7451S	MN7450T MN7451T	UNITS
Integral Linearity Error: Initial (+25°C) (Max.) Over Temperature (Max.)	±0.003 ±0.006	±0.0022 ±0.0045	±0.003 ±0.006	±0.0022 ±0.0045	%FSR %FSR
Resolution for which No Missing Codes is Guaranteed: Initial (25°C) Over Temperature	 15 14	 16 15	 15 14	 16 15	 Bits Bits
Unipolar Offset Error (Max.): Initial (+25°C) Drift	 ±0.06 ±7	 ±0.04 ±5	 ±0.06 ±7	 ±0.04 ±5	 %FSR ppm of FSR/°C
Bipolar Zero Error (Max.): Initial (+25°C) Drift	 ±0.06 ±4	 ±0.04 ±2.5	 ±0.06 ±4	 ±0.04 ±2.5	 %FSR ppm of FSR/°C
Gain Error (Max): Initial (+25°C) Drift	 ±0.1 ±15	 ±0.05 ±10	 ±0.1 ±15	 ±0.05 ±10	 % ppm/°C

SPECIFICATION NOTES:

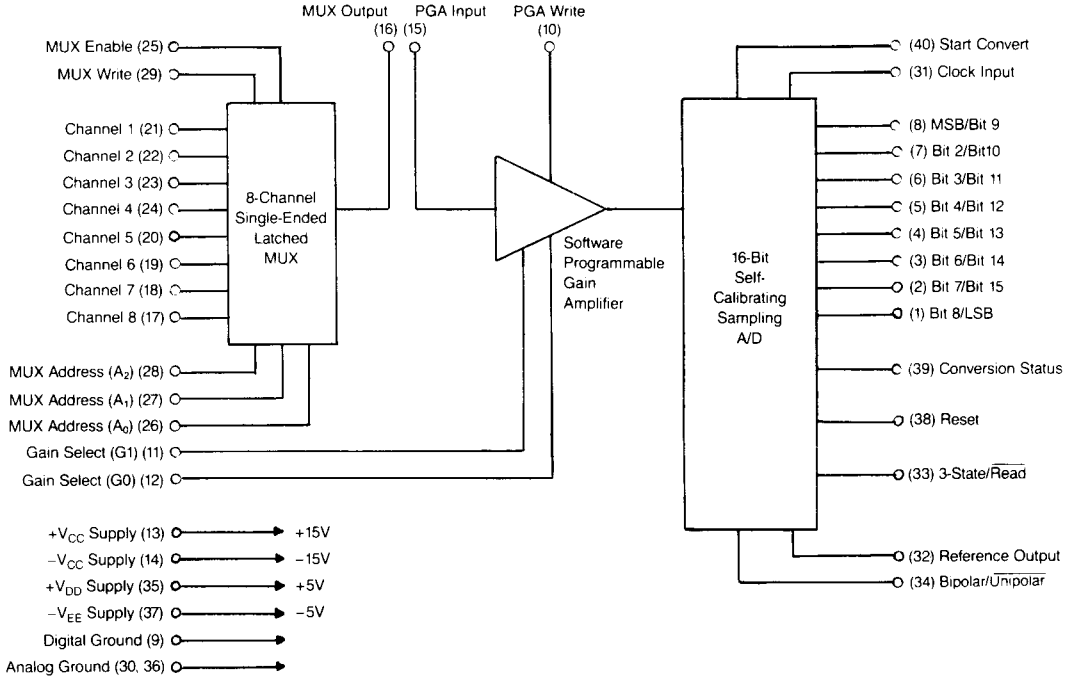
1. Specifications apply after initial calibration following power-up at +25°C.
2. Reference output is to be bypassed to Analog Ground with a 10μF capacitor in parallel with a 0.1μF capacitor. Reference must not be used for application circuitry without buffering.
3. Performance specifications apply to overall system (MUX, PGA, and A/D) with PGA Gain set to G=1.

PIN DESIGNATIONS



1	Bit 8/LSB	40	Start Convert
2	Bit 7/Bit 15	39	Conversion Status
3	Bit 6/Bit 14	38	Reset
4	Bit 5/Bit 13	37	−5V Supply
5	Bit 4/Bit 12	36	Analog Ground
6	Bit 3/Bit 11	35	+5V Supply
7	Bit 2/Bit 10	34	Bipolar/Unipolar
8	MSB/Bit 9	33	3-State/Read
9	Digital Ground	32	Reference Output
10	PGA Write	31	Clock In
11	Gain Select G1	30	Analog Ground
12	Gain Select G0	29	Mux Write
13	+15V Supply	28	Address A2
14	−15V Supply	27	Address A1
15	PGA Input	26	Address A0
16	Mux Output	25	Mux Enable
17	Channel 8	24	Channel 4
18	Channel 7	23	Channel 3
19	Channel 6	22	Channel 2
20	Channel 5	21	Channel 1

BLOCK DIAGRAM



DESCRIPTION OF OPERATION

MUX OPERATON/CHANNEL SELECTION — The 8-channel single-ended multiplexer with latch features overvoltage protection up to ±35V, channel selection and control inputs that are fully compatible with both CMOS and TTL logic levels, and guaranteed break-before-make switching.

The MUX Address input lines A2, A1, and A0 (pins 28, 27, and 26) are used to select 1 of 8 input channels. These address lines can be changed (MUX is in a transparent state similar to unlatched multiplexers) when Mux Write (pin 29) is low and Mux Enable (pin 25) is high. The channel address is latched by bringing Mux Write high. Changes to the Mux Address lines while Mux Write is high do not affect the channel selection, freeing a microprocessor from providing constant address inputs in order to remain on a desired channel. A new channel can be addressed while Mux Write is high although it will not be selected until Mux Write returns low.

MUX Channel Selection

MUX Address A2	A1	A0	MUX Enable	MUX Write	Channel Selected
X	X	X	0	0	None
0	0	0	1	0	1
0	0	1	1	0	2
0	1	0	1	0	3
0	1	1	1	0	4
1	0	0	1	0	5
1	0	1	1	0	6
1	1	0	1	0	7
1	1	1	1	0	8
X	X	X	X	1	Maintains Previous Selection

When MUX Enable and MUX Write are both low, all 8 channels are turned off. This function allows for cascading of additional input channels into the PGA Input (pin 15) or other external series signal conditioning normally connected to the MUX Output (pin 16).

PROGRAMMABLE GAIN AMP OPERATION — The single-ended software-programmable gain amplifier features latched selection of gains of 1, 2, 4 or 8 without the need for external resistors. The digital control inputs PGA Gain Select G1 (pin 11), G0 (pin 12) and PGA Write (pin 10) are TTL compatible.

As with the MUX, the PGA has both a transparent and latched mode of operation. The PGA will respond to changes of the gain select inputs while PGA Write is low. The PGA Gain Select inputs G1 and G0 are latched when PGA Write is brought high, and remain latched until PGA Write is returned low.

In application, PGA Write can be tied to MUX Write and together controlled from the same microprocessor or digital control line. Optimum performance of the DAS with regards to integral linearity drift over the full temperature range is achieved when the PGA is operated at a gain of 2.

PGA Gain Selection

Gain Select G1	G0	PGA Write	Gain
0	0	0	1
0	1	0	2
1	0	0	4
1	1	0	8
X	X	1	Previous State Latched

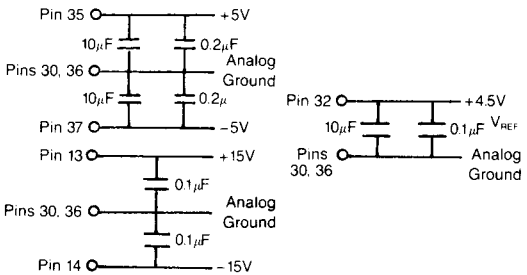
APPLICATIONS INFORMATION

POWER SUPPLIES/REFERENCE VOLTAGE — The DAS is powered from standard supplies of ±15V and ±5V. All supplies are internally connected to analog components and therefore must be of suitable quality. Supplies are decoulped internally to provide power for digital logic functions. It is strongly recommended that the power supplies be externally bypassed in the following manner.
The +15V (pin 13) and −15V (pin 14) supplies should be bypassed to analog ground with ceramic 0.1μF capacitors.

The +5V (pin 35) and −5V (pin 37) supplies should be bypassed to analog ground with tantalum 10μF caps in parallel with ceramic 0.2μF caps.

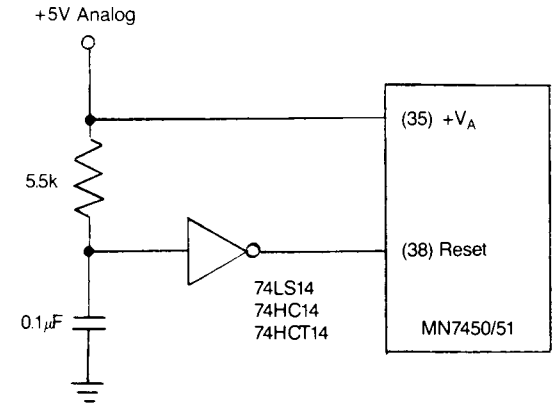
The Analog Grounds (pins 30, 36) and Digital Ground (pin 9) should be connected together and to a ground plane.

The Reference Output (pin 32) should be bypassed to analog ground with a tantalum 10μF cap in parallel with a ceramic 0.1μF cap. The reference output is an internally generated +4.5V that should not be used to drive any additional circuitry. If it absolutely needs to be used, it must be buffered.



Power Supply and Reference Decoupling

POWER-UP/CALIBRATION — Although the internal components are protected against overvoltage conditions, it is recommended that the ±15V supplies be applied simultaneously to or shortly after the ±5V supplies. Once the device is powered up, a reset calibration must be performed. The required initial reset is initiated by strobing the Reset (pin 38) high for a minimum of 100nsec. When Reset returns low, a full calibration cycle begins. This calibration cycle lasts 1,441,020 master clock cycles (equivalent to 360.255msec with a 4MHz external clock). During this time Conversion Status (pin 39) will be high, and return low when calibration is complete.



The reset calibration can be performed either under microprocessor control or by hardware using a reset circuit triggered at device power-up, as shown. The reset calibration may be used at any time or at any operating temperature throughout the lifetime of the device to ensure optimum performance.

During calibration the A/D's differential linearity self-adjusts to minimize errors due to internal component ratio drift mismatch.

ANALOG INPUT RANGES — There are two DAS models to choose from, each with unipolar and bipolar input ranges. With the PGA in a gain of 1, the MN7450 has a unipolar range of 0 to +5V and a bipolar range of -5V to +5V. The MN7451 has a unipolar range of 0 to +10V and a bipolar range of −10V to +10V. The unipolar ranges are digitally represented in Straight Binary coding. The bipolar ranges are digitally represented in Offset Binary coding. Selection of a unipolar or bipolar input transfer function is made digitally using Bipolar/Unipolar (pin 34).

MASTER CLOCK — The user has an option to use the internally generated master clock by tying Clock In (pin 31) low or to externally supply a master clock to the Clock In pin. The internal clock frequency (with Clock In low) will be a minimum of 2MHz. The external user supplied clock can be of TTL or CMOS levels and from a frequency minimum of 100kHz to a maximum of 4MHz. All device timing characteristics scale directly to the master clock frequency.

DIGITAL OUTPUT BITS — The DAS presents parallel data out in an 8-bit x 2 byte format upon execution of read operations. A read operation is performed by bringing 3-State/Read (pin 33) low. The first read following a completed conversion will bring the digital output lines out of the 3-state condition and present the 8 MSB's (MSB on pin 8 through Bit 8 on pin 1). The second read following a conversion is executed by bringing 3-State/Read back high and then low again. The 8 LSB's appear at the output (Bit 9 on pin 8 through LSB on pin 1). On subsequent reads before another conversion is complete, the MSB/LSB byte will toggle.

INITIATING CONVERSIONS — A falling edge on Start Convert (pin 40) sets the DAS into the hold mode and initiates a conversion cycle. The Start Convert input must remain low for a minimum of one master clock cycle plus 50nsec (300nsec w/4MHz clock). It must return high before the minimum conversion time of 69 master clock cycles plus 235nsec (17.235μsec w/4 MHz clock) to allow for sufficient acquisition time for the next sample.

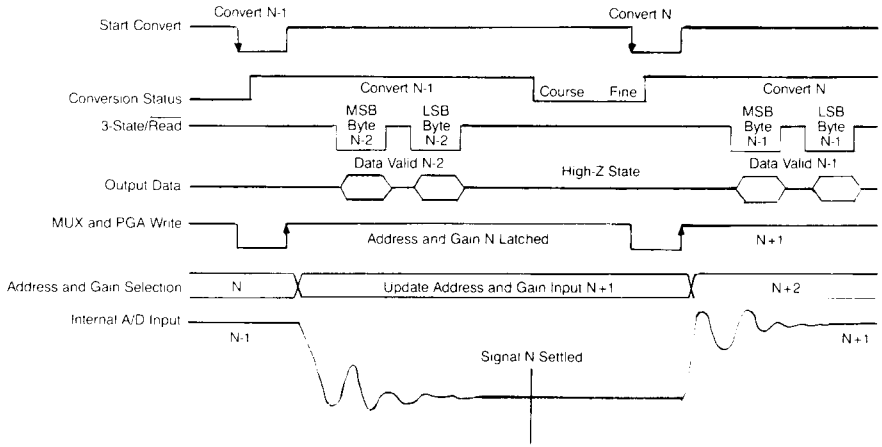
The Conversion Status output indicates that a conversion cycle is complete and data is valid when it falls low. It will return high on the first subsequent read operation or at the start of a new conversion cycle.

SIGNAL ACQUISITION — Upon completion of a conversion cycle, the sampling A/D automatically enters the track mode to acquire and follow the analog input before another conversion cycle is begun.

To operate at maximum throughput, the desired signal to be converted must already have been switched and settled through the MUX, PGA and buffer when the sampling A/D enters the track mode. This is acheived by selecting the new input signal channel and gain immediately after the sampling A/D enters the hold mode and begins to convert the old input signal channel. This pipelining technique allows the new input signal sufficient time to settle at the buffer output, which is internally disconnected to the sampling A/D input, until the old conversion is complete. The new signal then has only to be acquired by the sampling A/D, which has an acquisition time of six master clock cycles plus 2.25μsec (3.75μsec w/ 4MHz clock).

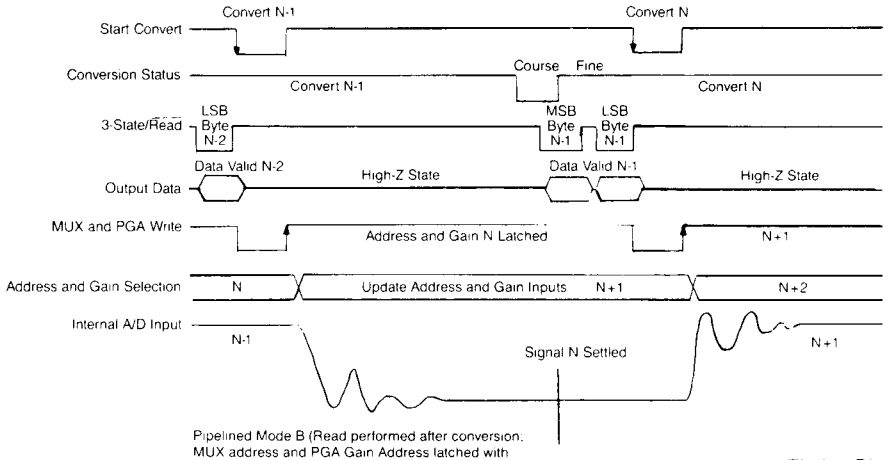
The throughput of the DAS when operated in this configuration is 47.65kHz. This pipelined configuration can be implemented by using the Start Convert signal to control both MUX Write and PGA Write. The channel and gain selections made during the conversion cycle are updated and latched as the previous channel conversion initiates.

There is a nonlinear reduction in throughput if insufficient time is allotted for switching and settling of a new channel before the acquisition cycle begins (at the fall of conversion status). This is due to the sampling A/D's method of acquisition, which is to coarse charge the hold capacitor for six master clock cycles (1.5μsec w/4MHz clock) immediately after the previous conversion is completed, and then fine charge the hold cap (and track the acquired signal) for a minimum of 2.25μsec until another Start Convert pulse is received. The required time for a new channel to be switched and settled at the buffer output is a worst case maximum of 6μsec. If the signal switched through the MUX, PGA and buffer is not settled completely before coarse charge begins, the bulk (or potentially all) of the signal acquisition must be performed in the slower fine charge mode. The absolute maximum worst case acquisition time, which occurs for a full scale step switched after completion of a previous conversion, is 40μsec. This corresponds to a worst case maximum throughput of approximately 17.5kHz (w/ 4MHz clock) for the non-pipelined configuration.



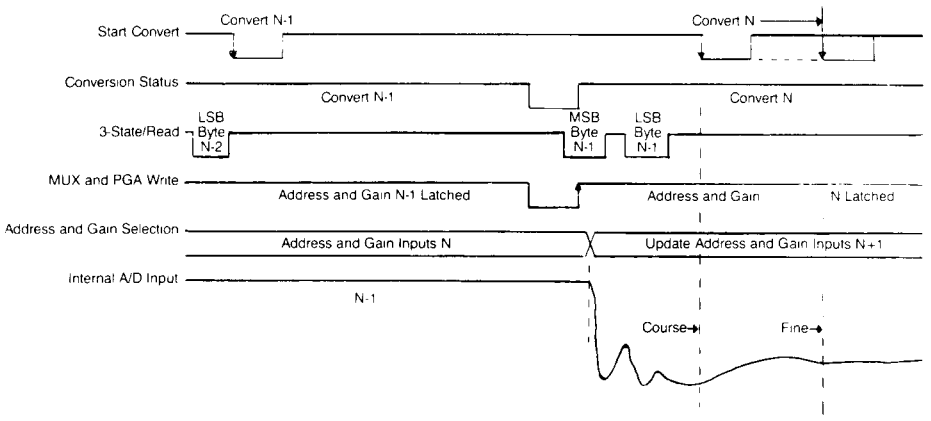
Pipelined Mode A (Read performed during conversion. MUX address and PGA Gain Address latched with Start Convert)

Timing Diagram Mode A



Pipelined Mode B (Read performed after conversion; MUX address and PGA Gain Address latched with Start Convert)

Timing Diagram Mode B



Non-Pipelined Mode C (Read performed after conversion; MUX address and PGA Gain Address latched with Conversion Complete)

Timing Diagram Mode C

MN7450