

# OKI Semiconductor

## MSM5116405A

4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

### DESCRIPTION

The MSM5116405A is a 4,194,304-word × 4-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM5116405A achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM5116405A is available in a 26/24-pin plastic SOJ or 26/24-pin plastic TSOP.

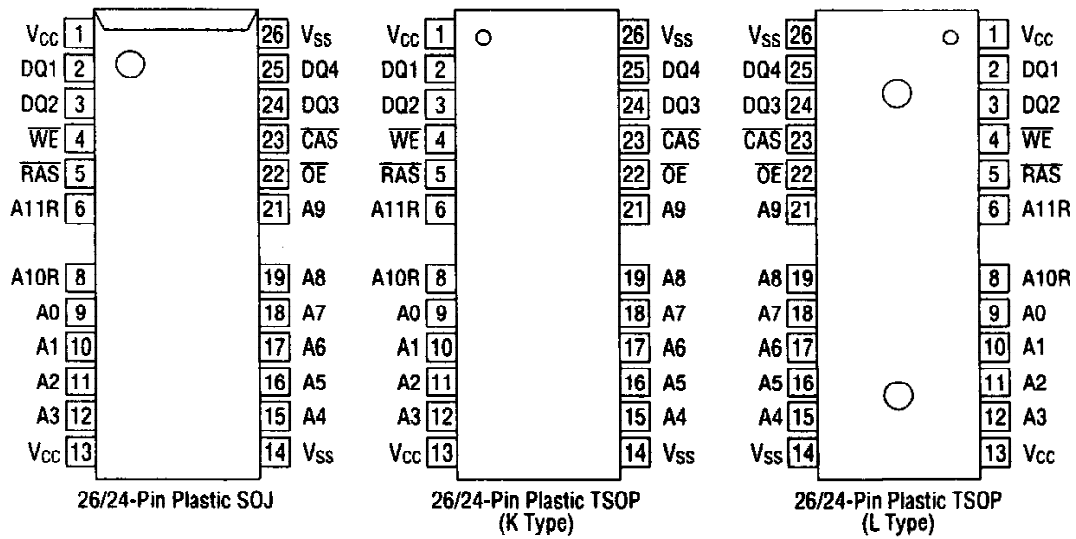
### FEATURES

- 4,194,304-word × 4-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 4096 cycles/64 ms
- Fast page mode with EDO, read modify write capability
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
- Multi-bit test mode capability
- Package options:
  - 26/24-Pin 300 mil plastic SOJ (SOJ26/24-P-300) (Product : MSM5116405A-xxSJ)
  - 26/24-Pin 300 mil plastic TSOP (TSOP26/24-P-300-K) (Product : MSM5116405A-xxTS-K)
  - (TSOP26/24-P-300-L) (Product : MSM5116405A-xxTS-L)xx indicates speed rank.

### PRODUCT FAMILY

| Family         | Access Time (Max.) |                 |                  |                  | Cycle Time<br>(Min.) | Power Dissipation |                |
|----------------|--------------------|-----------------|------------------|------------------|----------------------|-------------------|----------------|
|                | t <sub>RAC</sub>   | t <sub>AA</sub> | t <sub>CAC</sub> | t <sub>OEA</sub> |                      | Operating (Max.)  | Standby (Max.) |
| MSM5116405A-60 | 60 ns              | 30 ns           | 15 ns            | 15 ns            | 110 ns               | 550 mW            | 5.5 mW         |
| MSM5116405A-70 | 70 ns              | 35 ns           | 20 ns            | 20 ns            | 130 ns               | 495 mW            |                |
| MSM5116405A-80 | 80 ns              | 40 ns           | 20 ns            | 20 ns            | 150 ns               | 440 mW            |                |

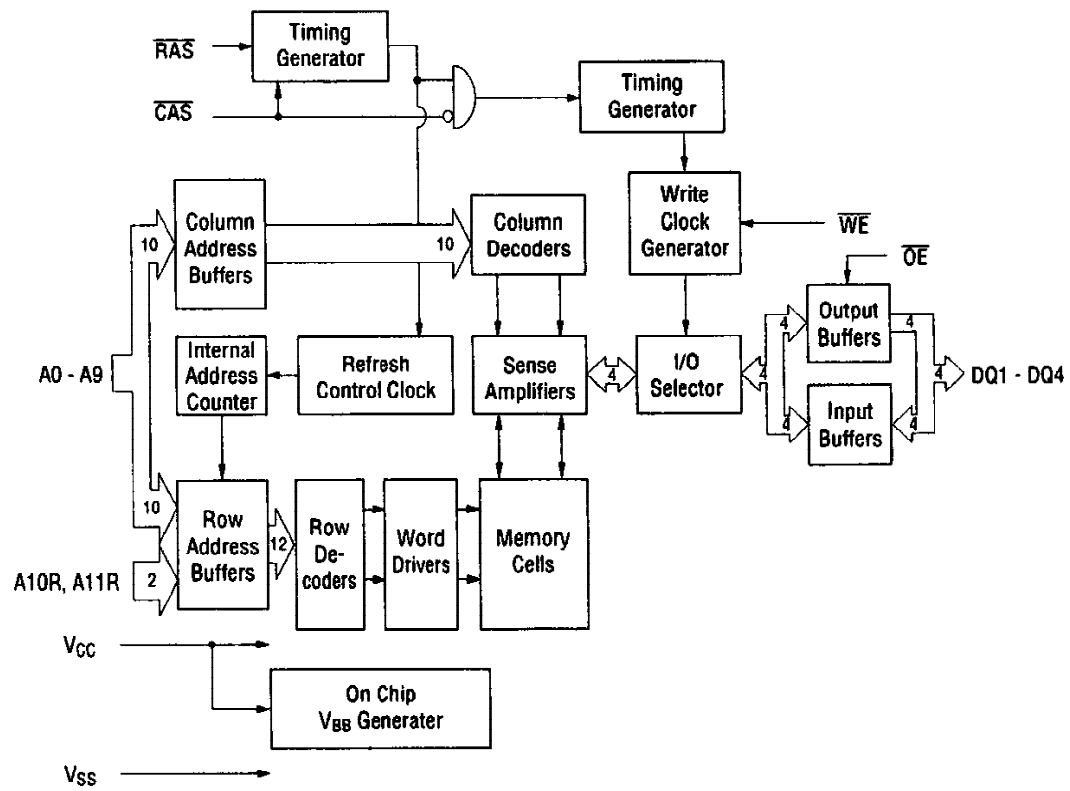
## PIN CONFIGURATION (TOP VIEW)



| Pin Name               | Function               |
|------------------------|------------------------|
| A0 - A9,<br>A10R, A11R | Address Input          |
| RAS                    | Row Address Strobe     |
| CAS                    | Column Address Strobe  |
| DQ1 - DQ4              | Data Input/Data Output |
| OE                     | Output Enable          |
| WE                     | Write Enable           |
| V <sub>CC</sub>        | Power Supply (5 V)     |
| V <sub>SS</sub>        | Ground (0 V)           |

Note : The same power supply voltage must be provided to every V<sub>CC</sub> pin, and the same GND voltage level must be provided to every V<sub>SS</sub> pin.

# BLOCK DIAGRAM



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

| Parameter                               | Symbol    | Rating      | Unit |
|-----------------------------------------|-----------|-------------|------|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_T$     | -1.0 to 7.0 | V    |
| Short Circuit Output Current            | $I_{OS}$  | 50          | mA   |
| Power Dissipation                       | $P_D^*$   | 1           | W    |
| Operating Temperature                   | $T_{opr}$ | 0 to 70     | °C   |
| Storage Temperature                     | $T_{stg}$ | -55 to 150  | °C   |

\*:  $T_a = 25^\circ\text{C}$ **Recommended Operating Conditions** $(T_a = 0^\circ\text{C to } 70^\circ\text{C})$ 

| Parameter            | Symbol   | Min. | Typ. | Max. | Unit |
|----------------------|----------|------|------|------|------|
| Power Supply Voltage | $V_{CC}$ | 4.5  | 5.0  | 5.5  | V    |
|                      | $V_{SS}$ | 0    | 0    | 0    | V    |
| Input High Voltage   | $V_{IH}$ | 2.4  | —    | 6.5  | V    |
| Input Low Voltage    | $V_{IL}$ | -1.0 | —    | 0.8  | V    |

**Capacitance** $(V_{CC} = 5\text{ V} \pm 10\%, T_a = 25^\circ\text{C}, f = 1\text{ MHz})$ 

| Parameter                                                                                     | Symbol    | Typ. | Max. | Unit |
|-----------------------------------------------------------------------------------------------|-----------|------|------|------|
| Input Capacitance<br>(A0 - A9, A10R, A11R)                                                    | $C_{IN1}$ | —    | 6    | pF   |
| Input Capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$ ) | $C_{IN2}$ | —    | 7    | pF   |
| Output Capacitance (DQ1 - DQ4)                                                                | $C_{I/O}$ | —    | 10   | pF   |

## DC Characteristics

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C)

| Parameter                                                                                            | Symbol           | Condition                                                                                                 | MSM5116405<br>A-60 |                 | MSM5116405<br>A-70 |                 | MSM5116405<br>A-80 |                 | Unit | Note |
|------------------------------------------------------------------------------------------------------|------------------|-----------------------------------------------------------------------------------------------------------|--------------------|-----------------|--------------------|-----------------|--------------------|-----------------|------|------|
|                                                                                                      |                  |                                                                                                           | Min.               | Max.            | Min.               | Max.            | Min.               | Max.            |      |      |
| Output High Voltage                                                                                  | V <sub>OH</sub>  | I <sub>OH</sub> = -5.0 mA                                                                                 | 2.4                | V <sub>CC</sub> | 2.4                | V <sub>CC</sub> | 2.4                | V <sub>CC</sub> | V    |      |
| Output Low Voltage                                                                                   | V <sub>OL</sub>  | I <sub>OL</sub> = 4.2 mA                                                                                  | 0                  | 0.4             | 0                  | 0.4             | 0                  | 0.4             | V    |      |
| Input Leakage Current                                                                                | I <sub>LI</sub>  | 0 V ≤ V <sub>I</sub> ≤ 6.5 V;<br>All other pins not<br>under test = 0 V                                   | -10                | 10              | -10                | 10              | -10                | 10              | μA   |      |
| Output Leakage Current                                                                               | I <sub>LO</sub>  | DQ disable<br>0 V ≤ V <sub>O</sub> ≤ 5.5 V                                                                | -10                | 10              | -10                | 10              | -10                | 10              | μA   |      |
| Average Power<br>Supply Current<br>(Operating)                                                       | I <sub>CC1</sub> | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling,<br>t <sub>RC</sub> = Min.                      | —                  | 100             | —                  | 90              | —                  | 80              | mA   | 1, 2 |
| Power Supply<br>Current (Standby)                                                                    | I <sub>CC2</sub> | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ = V <sub>IH</sub>                                       | —                  | 2               | —                  | 2               | —                  | 2               | mA   | 1    |
|                                                                                                      |                  | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$<br>≥ V <sub>CC</sub> - 0.2 V                            | —                  | 1               | —                  | 1               | —                  | 1               |      |      |
| Average Power<br>Supply Current<br>( $\overline{\text{RAS}}$ -only Refresh)                          | I <sub>CC3</sub> | $\overline{\text{RAS}}$ cycling,<br>$\overline{\text{CAS}}$ = V <sub>IH</sub> ,<br>t <sub>RC</sub> = Min. | —                  | 100             | —                  | 90              | —                  | 80              | mA   | 1, 2 |
| Power Supply<br>Current (Standby)                                                                    | I <sub>CC5</sub> | $\overline{\text{RAS}}$ = V <sub>IH</sub> ,<br>$\overline{\text{CAS}}$ = V <sub>IL</sub> ,<br>DQ = enable | —                  | 5               | —                  | 5               | —                  | 5               | mA   | 1    |
| Average Power<br>Supply Current<br>( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh) | I <sub>CC6</sub> | $\overline{\text{RAS}}$ cycling,<br>$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$                | —                  | 100             | —                  | 90              | —                  | 80              | mA   | 1, 2 |
| Average Power<br>Supply Current<br>(Fast Page Mode)                                                  | I <sub>CC7</sub> | $\overline{\text{RAS}}$ = V <sub>IL</sub> ,<br>$\overline{\text{CAS}}$ cycling,<br>t <sub>PC</sub> = Min. | —                  | 120             | —                  | 110             | —                  | 100             | mA   | 1, 3 |

- Notes :
1. I<sub>CC</sub> Max. is specified as I<sub>CC</sub> for output open condition.
  2. Address can be changed once or less while  $\overline{\text{RAS}}$  = V<sub>IL</sub>.
  3. Address can be changed once or less while  $\overline{\text{CAS}}$  = V<sub>IH</sub>.

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3, 12, 13

| Parameter                                                                  | Symbol            | MSM5116405<br>A-60 |         | MSM5116405<br>A-70 |         | MSM5116405<br>A-80 |         | Unit | Note    |
|----------------------------------------------------------------------------|-------------------|--------------------|---------|--------------------|---------|--------------------|---------|------|---------|
|                                                                            |                   | Min.               | Max.    | Min.               | Max.    | Min.               | Max.    |      |         |
| Random Read or Write Cycle Time                                            | t <sub>RC</sub>   | 110                | —       | 130                | —       | 150                | —       | ns   |         |
| Read Modify Write Cycle Time                                               | t <sub>RWC</sub>  | 155                | —       | 185                | —       | 205                | —       | ns   |         |
| Fast Page Mode Cycle Time                                                  | t <sub>HPC</sub>  | 25                 | —       | 30                 | —       | 35                 | —       | ns   |         |
| Fast Page Mode Read Modify Write Cycle Time                                | t <sub>PRWC</sub> | 85                 | —       | 100                | —       | 105                | —       | ns   |         |
| Access Time from $\overline{\text{RAS}}$                                   | t <sub>RAC</sub>  | —                  | 60      | —                  | 70      | —                  | 80      | ns   | 4, 5, 6 |
| Access Time from $\overline{\text{CAS}}$                                   | t <sub>CAC</sub>  | —                  | 15      | —                  | 20      | —                  | 20      | ns   | 4, 5    |
| Access Time from Column Address                                            | t <sub>AA</sub>   | —                  | 30      | —                  | 35      | —                  | 40      | ns   | 4, 6    |
| Access Time from $\overline{\text{CAS}}$ Precharge                         | t <sub>CPA</sub>  | —                  | 35      | —                  | 40      | —                  | 45      | ns   | 4       |
| Access Time from $\overline{\text{OE}}$                                    | t <sub>OEA</sub>  | —                  | 15      | —                  | 20      | —                  | 20      | ns   | 4       |
| Output Low Impedance Time from $\overline{\text{CAS}}$                     | t <sub>CLZ</sub>  | 0                  | —       | 0                  | —       | 0                  | —       | ns   | 4       |
| Data Output Hold After $\overline{\text{CAS}}$ Low                         | t <sub>DOH</sub>  | 3                  | 15      | 3                  | 15      | 3                  | 15      | ns   |         |
| $\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time          | t <sub>CEZ</sub>  | 3                  | 15      | 3                  | 20      | 3                  | 20      | ns   | 7, 8    |
| $\overline{\text{RAS}}$ to Data Output Buffer Turn-off Delay Time          | t <sub>REZ</sub>  | 3                  | 15      | 3                  | 20      | 3                  | 20      | ns   | 7, 8    |
| $\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time           | t <sub>OEZ</sub>  | 3                  | 15      | 3                  | 20      | 3                  | 20      | ns   | 7       |
| $\overline{\text{WE}}$ to Data Output Buffer Turn-off Delay Time           | t <sub>WEZ</sub>  | 3                  | 15      | 3                  | 20      | 3                  | 20      | ns   | 7       |
| Transition Time                                                            | t <sub>T</sub>    | 2                  | 50      | 2                  | 50      | 2                  | 50      | ns   | 3       |
| Refresh Period                                                             | t <sub>REF</sub>  | —                  | 64      | —                  | 64      | —                  | 64      | ms   |         |
| $\overline{\text{RAS}}$ Precharge Time                                     | t <sub>RP</sub>   | 40                 | —       | 50                 | —       | 60                 | —       | ns   |         |
| $\overline{\text{RAS}}$ Pulse Width                                        | t <sub>RAS</sub>  | 60                 | 10,000  | 70                 | 10,000  | 80                 | 10,000  | ns   |         |
| $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode with EDO)              | t <sub>RASP</sub> | 60                 | 100,000 | 70                 | 100,000 | 80                 | 100,000 | ns   |         |
| $\overline{\text{RAS}}$ Hold Time                                          | t <sub>RSH</sub>  | 15                 | —       | 20                 | —       | 20                 | —       | ns   |         |
| $\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$     | t <sub>ROH</sub>  | 10                 | —       | 10                 | —       | 10                 | —       | ns   |         |
| $\overline{\text{CAS}}$ Precharge Time (Fast Page Mode with EDO)           | t <sub>CP</sub>   | 10                 | —       | 10                 | —       | 10                 | —       | ns   |         |
| $\overline{\text{CAS}}$ Pulse Width                                        | t <sub>CAS</sub>  | 10                 | 10,000  | 10                 | 10,000  | 15                 | 10,000  | ns   |         |
| $\overline{\text{CAS}}$ Hold Time                                          | t <sub>CSH</sub>  | 40                 | —       | 45                 | —       | 50                 | —       | ns   |         |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time          | t <sub>CRP</sub>  | 10                 | —       | 10                 | —       | 10                 | —       | ns   |         |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time          | t <sub>RHCP</sub> | 35                 | —       | 40                 | —       | 45                 | —       | ns   |         |
| $\overline{\text{OE}}$ Hold Time from $\overline{\text{CAS}}$ (DQ Disable) | t <sub>CHO</sub>  | 5                  | —       | 10                 | —       | 10                 | —       | ns   |         |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time              | t <sub>RCD</sub>  | 20                 | 45      | 20                 | 50      | 20                 | 60      | ns   | 5       |
| $\overline{\text{RAS}}$ to Column Address Delay Time                       | t <sub>RAD</sub>  | 15                 | 30      | 15                 | 35      | 15                 | 40      | ns   | 6       |
| $\overline{\text{RAS}}$ to Second $\overline{\text{CAS}}$ Delay Time       | t <sub>RSCD</sub> | 60                 | —       | 70                 | —       | 80                 | —       | ns   |         |
| Row Address Set-up Time                                                    | t <sub>ASR</sub>  | 0                  | —       | 0                  | —       | 0                  | —       | ns   |         |
| Row Address Hold Time                                                      | t <sub>RAH</sub>  | 10                 | —       | 10                 | —       | 10                 | —       | ns   |         |
| Column Address Set-up Time                                                 | t <sub>ASC</sub>  | 0                  | —       | 0                  | —       | 0                  | —       | ns   |         |
| Column Address Hold Time                                                   | t <sub>CAH</sub>  | 10                 | —       | 15                 | —       | 15                 | —       | ns   |         |
| Column Address Hold Time from $\overline{\text{RAS}}$                      | t <sub>AR</sub>   | 40                 | —       | 45                 | —       | 50                 | —       | ns   |         |
| Column Address to $\overline{\text{RAS}}$ Lead Time                        | t <sub>RAL</sub>  | 30                 | —       | 35                 | —       | 40                 | —       | ns   |         |

AC Characteristics (2/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3, 12, 13

| Parameter                                                                                                                   | Symbol            | MSM5116405<br>A-60 |      | MSM5116405<br>A-70 |      | MSM5116405<br>A-80 |      | Unit | Note |
|-----------------------------------------------------------------------------------------------------------------------------|-------------------|--------------------|------|--------------------|------|--------------------|------|------|------|
|                                                                                                                             |                   | Min.               | Max. | Min.               | Max. | Min.               | Max. |      |      |
| Read Command Set-up Time                                                                                                    | t <sub>RCS</sub>  | —                  | —    | 0                  | —    | 0                  | 0    | ns   |      |
| Read Command Hold Time                                                                                                      | t <sub>RCH</sub>  | —                  | —    | 0                  | —    | 0                  | 0    | ns   | 9    |
| Read Command Hold Time referenced to $\overline{\text{RAS}}$                                                                | t <sub>RRH</sub>  | —                  | —    | 0                  | —    | 0                  | 0    | ns   | 9    |
| Write Command Set-up Time                                                                                                   | t <sub>WCS</sub>  | —                  | —    | 0                  | —    | 0                  | 0    | ns   | 10   |
| Write Command Hold Time                                                                                                     | t <sub>WCH</sub>  | —                  | —    | 15                 | —    | 15                 | 10   | ns   |      |
| Write Command Hold Time from $\overline{\text{RAS}}$                                                                        | t <sub>WCR</sub>  | —                  | —    | 45                 | —    | 50                 | 40   | ns   |      |
| Write Command Pulse Width                                                                                                   | t <sub>WP</sub>   | —                  | —    | 10                 | —    | 10                 | 10   | ns   |      |
| $\overline{\text{WE}}$ Pulse Width (DQ Disable)                                                                             | t <sub>WPE</sub>  | —                  | —    | 10                 | —    | 10                 | 5    | ns   |      |
| $\overline{\text{OE}}$ Command Hold Time                                                                                    | t <sub>OEH</sub>  | —                  | —    | 20                 | —    | 20                 | 15   | ns   |      |
| $\overline{\text{OE}}$ Precharge Time                                                                                       | t <sub>OEP</sub>  | —                  | —    | 10                 | —    | 10                 | 10   | ns   |      |
| $\overline{\text{OE}}$ Command Hold Time                                                                                    | t <sub>OCH</sub>  | —                  | —    | 10                 | —    | 10                 | 10   | ns   |      |
| Write Command to $\overline{\text{RAS}}$ Lead Time                                                                          | t <sub>RWL</sub>  | —                  | —    | 20                 | —    | 20                 | 15   | ns   |      |
| Write Command to $\overline{\text{CAS}}$ Lead Time                                                                          | t <sub>CWL</sub>  | —                  | —    | 20                 | —    | 20                 | 15   | ns   |      |
| Data-in Set-up Time                                                                                                         | t <sub>DS</sub>   | —                  | —    | 0                  | —    | 0                  | 0    | ns   | 11   |
| Data-in Hold Time                                                                                                           | t <sub>DH</sub>   | —                  | —    | 15                 | —    | 15                 | 15   | ns   | 11   |
| Data-in Hold Time from $\overline{\text{RAS}}$                                                                              | t <sub>DHR</sub>  | —                  | —    | 45                 | —    | 50                 | 40   | ns   |      |
| $\overline{\text{OE}}$ to Data-in Delay Time                                                                                | t <sub>OED</sub>  | —                  | —    | 20                 | —    | 20                 | 15   | ns   |      |
| $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time                                                                | t <sub>CWD</sub>  | —                  | —    | 50                 | —    | 50                 | 40   | ns   | 10   |
| Column Address to $\overline{\text{WE}}$ Delay Time                                                                         | t <sub>AWD</sub>  | —                  | —    | 65                 | —    | 70                 | 55   | ns   | 10   |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time                                                                | t <sub>RWD</sub>  | —                  | —    | 100                | —    | 110                | 85   | ns   | 10   |
| $\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time                                                         | t <sub>CPWD</sub> | —                  | —    | 70                 | —    | 75                 | 60   | ns   | 10   |
| $\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge                                            | t <sub>RPC</sub>  | —                  | —    | 10                 | —    | 10                 | 10   | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )   | t <sub>CSR</sub>  | —                  | —    | 10                 | —    | 10                 | 10   | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )     | t <sub>CHR</sub>  | —                  | —    | 20                 | —    | 20                 | 20   | ns   |      |
| $\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)                                                               | t <sub>CPT</sub>  | —                  | —    | 40                 | —    | 40                 | 40   | ns   |      |
| $\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ ) | t <sub>WRP</sub>  | —                  | —    | 10                 | —    | 10                 | 10   | ns   |      |
| $\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )    | t <sub>WRH</sub>  | —                  | —    | 10                 | —    | 10                 | 10   | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)                                                   | t <sub>WTS</sub>  | —                  | —    | 10                 | —    | 10                 | 10   | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)                                                     | t <sub>WTH</sub>  | —                  | —    | 20                 | —    | 20                 | 20   | ns   |      |

- Notes:
1. A start-up delay of 200  $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 5$  ns.
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, access time is controlled by  $t_{AA}$ .
  7.  $t_{CEZ}$  (Max.),  $t_{REZ}$  (Max.),  $t_{WEZ}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{CEZ}$  and  $t_{REZ}$  must be satisfied for open circuit condition.
  9.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  10.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  11. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in an early write cycle, and to  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle or a read modify write cycle.
  12. The test mode is initiated by performing a  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test mode CA0 and CA1 are not used and each DQ pin now accesses 4-bit locations. Since all 4 DQ pins are used, a total of 16 data bits can be written in parallel into the memory array. In a read cycle, if 4 data bits are equal, the DQ pin will indicate a high level. If the 4 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a  $\overline{\text{RAS}}$ -only refresh cycle or a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle.
  13. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

### See ADDENDUM L for AC Timing Waveforms