Configuration EPROMs for FLEX 8000 Devices

August 1993, ver. 2 Data Sheet

Features

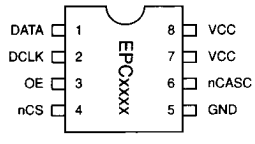
- Family of serial EPROMs designed to configure FLEX 8000 devices
- Available in compact, one-time programmable (OTP) 8-pin plastic dual in-line (PDIP) and 20-pin plastic J-lead chip carrier (PLCC) packages (see Figure 1); 32-pin thin quad flat pack (TQFP) packages under development
- Simple 4-wire interface to FLEX 8000 devices for ease of use
- Low current during configuration (15 mA) and near-zero standby current (100 µA)
- Software design support with Altera's MAX+PLUS II development system for IBM PC, Sun SPARCstation, and HP 9000 Series 700 platforms
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers, including Data I/O

Functional Description

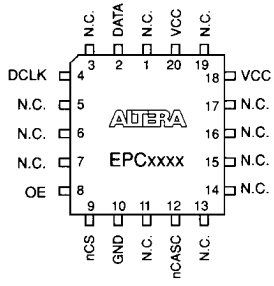
In SRAM-based devices, configuration data must be reloaded each time the system initializes, or whenever new configuration data is desired. Altera's serial-memory Configuration EPROMs store configuration data for the SRAM-based Altera FLEX 8000 devices.

Figure 1. Configuration EPROM Package Pin-Out Diagrams

Package outlines not drawn to scale.



8-Pin DIP



20-Pin J-Lead

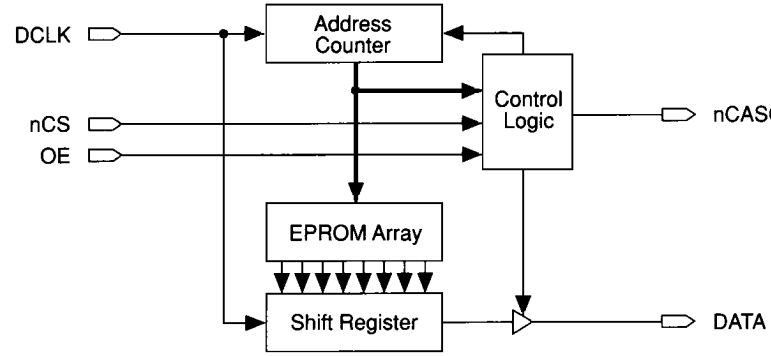
Table 1 shows the size of each Altera Configuration EPROM and indicates which FLEX 8000 device is typically configured by each.

Table 1. Typical Application for Altera Configuration EPROMs

Device	Device Size	Typical FLEX 8000 Device Configured
EPC1064	65,536 × 1 bit	EPF8282, EPF8282V, EPF8452
EPC1213	212,992 × 1 bit	EPF8820, EPF81188

Figure 2 shows a block diagram of the Configuration EPROM. Configuration data is stored in the EPROM array and clocked out serially by the DCLK input. The Output Enable (OE), Chip-Select (nCS), and Clock (DCLK) pins supply the control signals for the address counter and the output tri-state. The device presents the configuration data as a serial bit stream on the DATA pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The nCASC pin provides handshaking between multiple Configuration EPROMs, so that a set of devices can be linked together to serially configure a large FLEX 8000 device. Refer to the *FLEX 8000 Programmable Logic Device Family Data Sheet* and *Application Note 33 (Configuring FLEX 8000 Devices)* in this data book for more information on FLEX architecture and configuration.

Figure 2. Configuration EPROM Functional Block Diagram



The control signals for Configuration EPROMs (DCLK, nCS, OE) interface directly to the FLEX 8000 device control signals. A FLEX 8000 device can control the entire configuration process by retrieving the configuration data from the Configuration EPROM without an external intelligent controller. Configuration usually occurs automatically at system power-up.

The OE and nCS pins work together to control the tri-state buffer on the DATA output pin, and to enable the address counter in the Configuration EPROM. When OE is driven low, the device resets the address counter and tri-states the DATA pin. When the OE pin is driven high again, the device is

controlled by the nCS pin. If nCS is held high after the OE reset pulse, the counter is disabled, and the DATA output pin is tri-stated. When nCS is driven low, the counter is enabled and the DATA output pin is enabled. The nCS pin can then be held either high or low to control the output and counter. When OE is driven low again, regardless of the state of nCS, the address counter is reset and the DATA output pin is tri-stated. Upon power-up, the address counter is automatically reset. Table 2 describes the pin functions of Altera Configuration EPROMs.

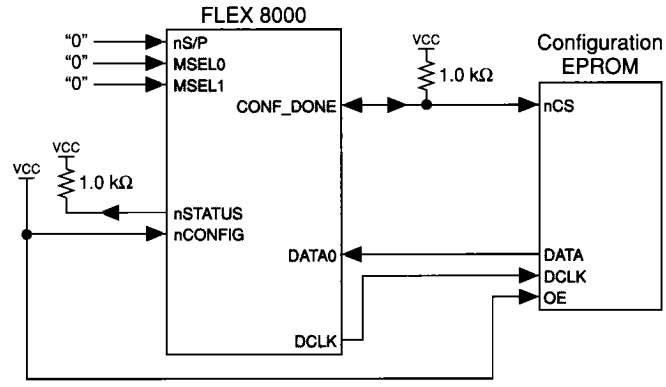
Table 2. Configuration EPROM Pin Functions

Pin Name	8-Pin PDIP Pin Number	20-Pin PLCC Pin Number	Pin Type	Description
DATA	1	2	Output	Serial data output.
DCLK	2	4	Input	Clock input. Rising edges on DCLK increment the internal address counter and cause the next bit of data to be presented on DATA. The counter is incremented only if the OE input is held high and the nCS input is held low.
OE	3	8	Input	Output Enable (active high) and Reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS	4	9	Input	Chip-Select output (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC	6	12	Output	Cascade-Select output (active low). This output goes low when the address counter has reached its maximum value. nCASC is usually connected to the nCS input of the next Configuration EPROM in a daisy-chain, so the next DCLK clocks data out of the next Configuration EPROM.
GND	5	10	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	Power	Power pin

Single-Device Configuration

The active serial (AS) configuration scheme uses a serial Configuration EPROM (e.g., EPC1213) as a data source for a FLEX 8000 device. The Configuration EPROM presents its data to the FLEX 8000 device in a serial bit-stream. Figure 3 shows a typical circuit in which the FLEX 8000 device controls the configuration process and uses a serial Configuration EPROM as the data source. For additional information, refer to *Application Note 33 (Configuring FLEX 8000 Devices).*

Figure 3. Active Serial Configuration



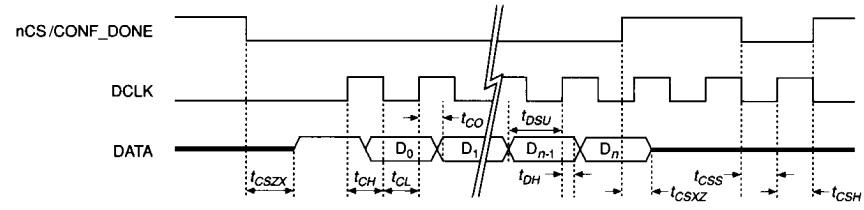
The nCONFIG pin on the FLEX 8000 device in Figure 3 is connected to V_{CC}, so the device automatically configures itself at system power-up. The system can monitor the nSTATUS pin to ensure that configuration occurs correctly. Immediately after power-up, the FLEX 8000 device pulls the nSTATUS pin low and releases it within 100 ms. Once released, the open-drain nSTATUS pin is pulled up to V_{CC} by an external 1.0-kΩ pull-up resistor. If an error occurs during configuration, the FLEX 8000 device pulls the nSTATUS pin low, indicating that configuration was unsuccessful.

The DCLK signal, which is driven by the FLEX 8000 device, clocks sequential data bits from the Configuration EPROM. While the SRAM data is being loaded, the FLEX 8000 device holds the open-drain CONF_DONE pin at GND, indicating that data is loading. A 24-bit program-length counter within the FLEX 8000 device stores the program length, i.e., the total number of configuration bits. Once the terminal count value for the configuration data (i.e., the last configuration data bit) has been reached, the FLEX 8000 device releases the CONF_DONE pin, which is subsequently pulled up to V_{CC} by an external 1.0-kΩ pull-up resistor. The resulting high input on the nCS pin causes the Configuration EPROM to tri-state its DATA output, electrically removing the Configuration EPROM from the circuit.

After it releases the CONF_DONE pin, the FLEX 8000 device uses it as an input for monitoring the configuration process. When the FLEX 8000 device senses a high logic level on CONF_DONE, it completes the initialization process and enters user mode. Figure 4 shows the timing associated with the AS configuration process and the order of transitions on the control signals.

Worst-case values for the timing parameters shown in Figure 4 are given in the "Timing Parameters" table later in this data sheet.

Figure 4. Single-Device Configuration Timing Waveforms

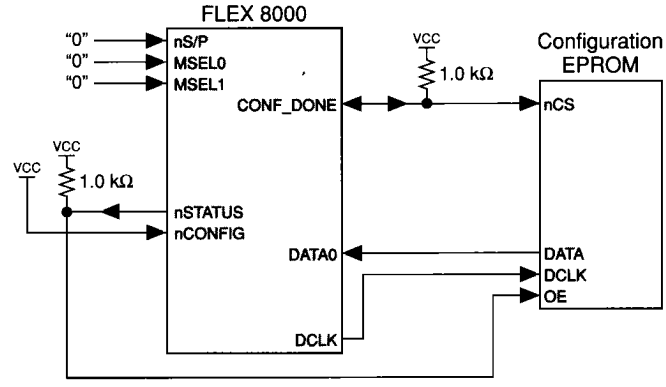


In the circuit shown in Figure 3, the nCONFIG pin on the FLEX 8000 device is tied to the Output Enable (OE) input of the Configuration EPROM; both are tied to V_{CC}. A high logic level on the nCONFIG input automatically starts the configuration. The output of the serial Configuration EPROM is enabled by a high input on its OE pin. If an error occurs during circuit configuration, the FLEX 8000 device pulls and holds the nSTATUS pin low, indicating a configuration error. External circuitry is used to monitor the nSTATUS pin and take appropriate action if configuration fails. This circuitry must assert a high-low-high pulse on the nCONFIG pin to reconfigure the device after the error. The same circuitry can also be used to begin reconfiguring the FLEX 8000 device at any time after system power-up.

The FLEX 8000 device's built-in *Auto-Restart Configuration on Frame Error* option bit allows the device to automatically reconfigure itself if it encounters an error during configuration. If this option bit is turned on, a configuration error causes the FLEX 8000 device to pull the nSTATUS pin low for 10 internal Clock cycles and then release it. This 1- to 3-µs pulse on the nSTATUS pin provides an external indication that reconfiguration is about to begin. It also can be used to reset the Altera Configuration EPROM.

Figure 5 shows a circuit that uses the *Auto-Restart Configuration on Frame Error* option. The nSTATUS pin is connected to the OE input on the Altera Configuration EPROM so that the error-reset pulse on nSTATUS resets the internal address counter on the Configuration EPROM and prepares it to reconfigure the FLEX 8000 device. The nCONFIG input is also available to initiate a reconfiguration cycle externally. Since the nSTATUS pin is pulled low and then released whenever configuration begins, it resets the Configuration EPROM before reconfiguration. During device operation, if V_{CC} drops below the power-on reset (POR) threshold for the FLEX 8000 device, nSTATUS is pulsed and the Configuration EPROM is reset in the same way to provide automatic reconfiguration. Timing for the circuit in Figure 5 is identical to the timing shown in Figure 4 for the AS configuration scheme (the error-reset pulse on nSTATUS is not shown).

Figure 5. Active Serial Device Configuration with Automatic Reconfiguration on Error



MAX+PLUS II Support

The MAX+PLUS II development system provides programming support for Altera Configuration EPROMs. MAX+PLUS II software automatically generates a Programmer Object File (**.pof**) for every FLEX 8000 device in a project. By default, each FLEX 8000 device in a multi-device project has a dedicated serial Configuration EPROM. MAX+PLUS II selects the appropriate Configuration EPROM to most efficiently store the data for each FLEX 8000 device.

The POF includes a preamble, cyclic redundancy check (CRC), and synchronization data that allow it to be used in a serial bitstream. The POF is programmed into the Configuration EPROM with MAX+PLUS II and a Configuration EPROM programming adapter. A number of other programming hardware manufacturers, including Data I/O, support programming of Configuration EPROMs. See the *Altera Programming Hardware* and *Programming Hardware Manufacturers* data sheets in this data book.

Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			20	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			100	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	4.75	5.25	V
V_I	Input voltage	*Note (1)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

DC Operating Conditions *Notes (2), (3)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–10	10	µA

Supply Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100		µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 8 MHz		10		mA

Capacitance *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Timing Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
t_{OEZX}	OE high to DATA output enabled			50	ns
t_{CSZX}	nCS low to DATA output enabled			50	ns
t_{CSXZ}	nCS high to DATA output disabled			50	ns
t_{CSS}	nCS low setup time to first DCLK rising edge		100		ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		ns
t_{DSU}	Data setup time before rising edge on DCLK		50		ns
t_{DH}	Data hold time after rising edge on DCLK		0		ns
t_{CO}	DCLK to DATA out delay, *Note (5)*			75	ns
t_{CK}	Clock period		160		ns
f_{CK}	Clock frequency			6	MHz
t_{CL}	DCLK low time		80		ns
t_{CH}	DCLK high time		80		ns
t_{XZ}	OE low or nCS high to DATA output disabled			50	ns
t_{OEW}	OE pulse width to guarantee counter reset		100		ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			60	ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			50	ns
t_{CEOUT}	nCS high to nCASC high delay			100	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
(4) Capacitance is sample-tested only.
(5) Eight Clock cycles are required after the t_{CSS} setup time has been met to clock out the first eight bits. These bits are all high and are used to synchronize the configuration process. The ninth Clock cycle presents the first configuration data bit.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPC1213, EPC1064
Industrial Temp.	(–40° C to 85° C)	Consult factory
Military Temp.	(–55° C to 125° C)	Consult factory

Package Outlines

See the *Package Outlines Data Sheet* in this data book for dimensions of the Configuration EPROM 8-pin PDIP and 20-pin PLCC packages. For package outlines of the 32-pin TQFP Configuration EPROM, contact Altera Applications at (800) 800-EPLD.