# SiT5186 ADVANCED

AEC-Q100, 1 to 60 MHz, ±0.5 to ±2.5 ppm, Elite Platform™ Super-TCXO

## Description

The SiT5186 is a ±0.5 to ±2.5 ppm MEMS Super-TCXO that is engineered for best dynamic performance. It is ideal for high reliability GNSS-based precision positioning and timing applications.

Leveraging SiTime's unique DualMEMS™ temperature sensing and TurboCompensation™ technologies, the SiT5186 delivers the best dynamic performance for timing stability in the presence of environmental stressors due to air flow, temperature perturbation, vibration, shock, and electromagnetic interference. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT5186 offers three device configurations that can be ordered using Ordering Codes for:

1) TCXO with non-pullable output frequency,
2) VCTCXO allowing voltage control of output frequency, and
3) DCTCXO, enabling digital control of output frequency using an I²C interface, pullable to 5 ppt (parts per trillion) resolution.

The SiT5186 can be factory programmed for any combination of frequency, stability, voltage, and pull range. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

Refer to Manufacturing Guideline for proper reflow profile and PCB cleaning recommendations to ensure best performance.

## Features

- Automotive AEC-Q100 qualified
- AEC-Q100 Grade 2 temp. range (-40°C to +105°C) Grade 3 and 4 also available
- Any frequency from 1 MHz to 60 MHz in 1 Hz steps
- Factory programmable options for low lead times
- Best dynamic stability under airflow, thermal shock
  - ±0.5 ppm stability across temperature
  - ±15 ppb/°C typical frequency slope (ΔF/ΔT)
- No activity dips or micro jumps
- Resistant to shock, vibration and board bending
- On-chip regulators eliminate the need for external LDOs
- Digital frequency pulling (DCTCXO) via I²C
  - Digital control of output frequency and pull range
  - Up to ±3200 ppm pull range
  - Frequency pull resolution down to 5 ppt
- 2.5V, 2.8V, 3.0V and 3.3V supply voltage
- LVCMOS or clipped sinewave output
- RoHS and REACH compliant
- Pb-free, Halogen-free, Antimony-free

## Applications

- Precision GNSS systems

TempFlat MEMS™

## Block Diagram

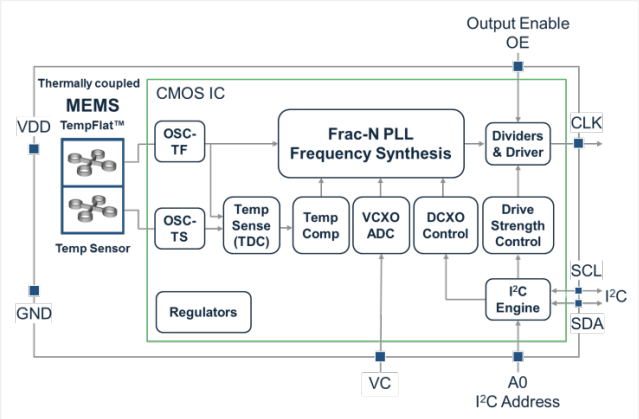



**Figure 1. SiT5186 Block Diagram**

## 5.0 x 3.2 mm² Package Pinout

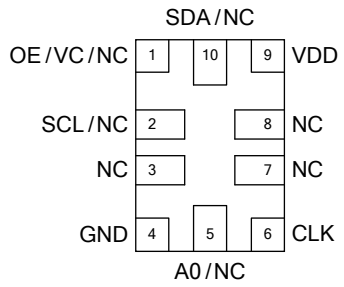
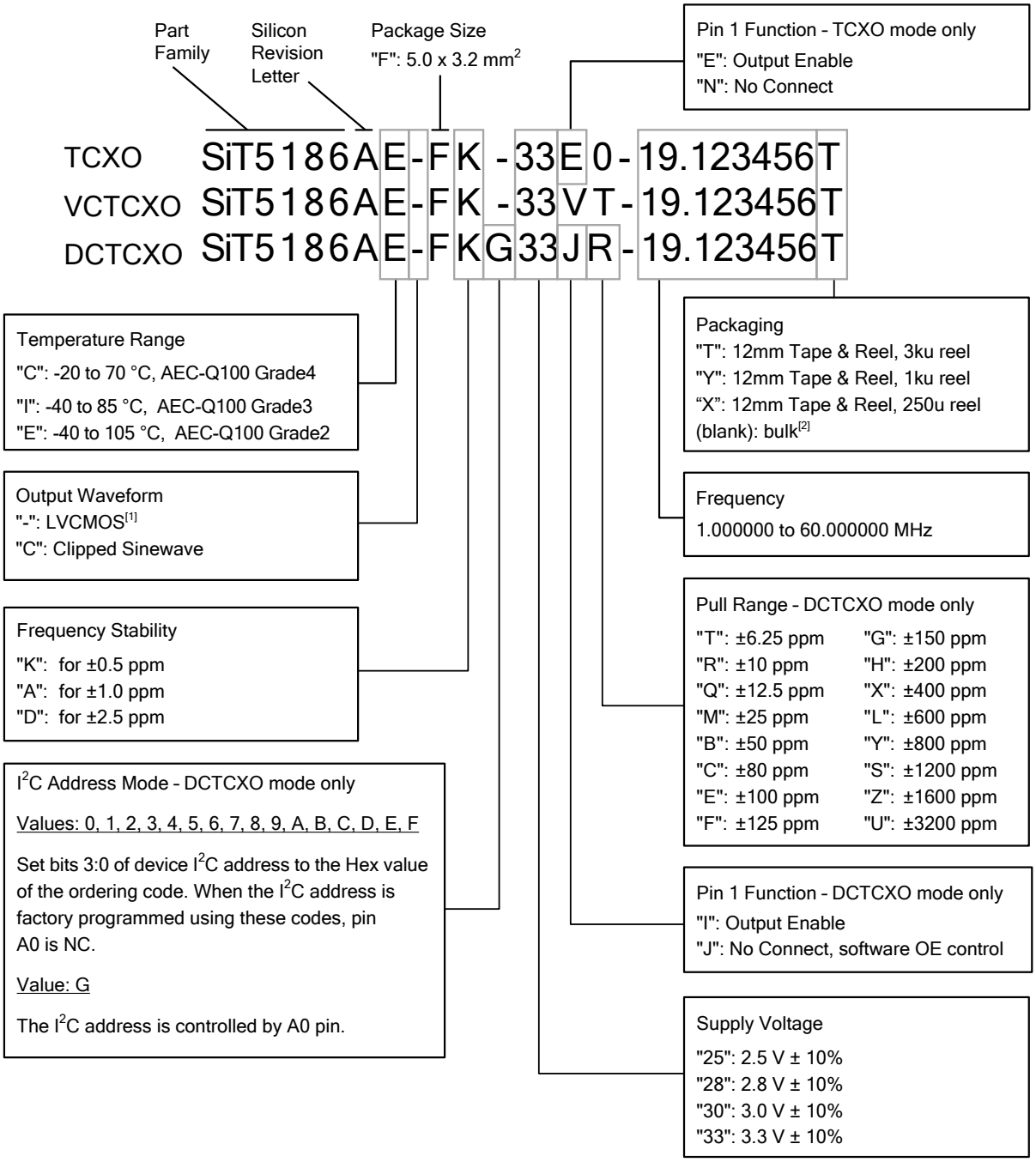



**Figure 2. Pin Assignments (Top view)**
(Refer to Table 13 for Pin Descriptions)

## Ordering Information




**Notes:**

1. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI.
2. Bulk is available for sampling only

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## Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3V Vdd.

**Table 1. Output Characteristics**

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Coverage** | | | | | | |
| **Nominal Output Frequency Range** | F_nom | 1 | – | 60 | MHz | |
| **Temperature Range** | | | | | | |
| **Operating Temperature Range** | T_use | -20 | – | +70 | °C | AEC-Q100 Grade4, ambient temperature |
| | | -40 | – | +85 | °C | AEC-Q100 Grade3, ambient temperature |
| | | -40 | – | +105 | °C | AEC-Q100 Grade2, ambient temperature |
| **Frequency Stability** | | | | | | |
| **Initial Tolerance** | F_init | – | ±1 | – | ppm | Initial frequency at 25°C inclusive of solder-down shift at 48 hours after 2 reflows |
| **Supply Voltage Sensitivity** | F_Vdd | – | ±7.10 | – | ppb | ±0.5 ppm F_stab, Vdd ±5% |
| | | – | ±11.83 | – | ppb | ±1.0ppm F_stab, Vdd ±5% |
| | | – | ±28.40 | – | ppb | ±2.5 ppm F_stab, Vdd ±5% |
| **Output Load Sensitivity** | F_load | – | ±0.81 | – | ppb | ±0.5 ppm F_stab. LVCMOS output, 15 pF ±10%. Clipped sinewave output, 10kΩ \|\| 10 pF ±10% |
| | | – | ±1.35 | – | ppb | ±1.0 ppm F_stab. LVCMOS output, 15 pF ±10%. Clipped sinewave output, 10kΩ \|\| 10 pF ±10% |
| | | – | ±3.24 | – | ppb | ±2.5 ppm F_stab. LVCMOS output, 15 pF ±10%. Clipped sinewave output, 10kΩ \|\| 10 pF ±10% |
| **Frequency Stability over Temperature** | F_stab | -0.5 | – | +0.5 | ppm | Referenced to (max frequency + min frequency)/2 over the rated temperature range. Vc=Vdd/2 for VCTCXO |
| | | -1.0 | – | +1.0 | ppm | |
| | | -2.5 | – | +2.5 | ppm | |
| **Frequency vs. Temperature Slope** | ΔF/ΔT | – | ±15 | – | ppb/°C | ±0.5 ppm F_stab, 0.5°C/min ramp rate, -40 to 105 ºC |
| | | – | ±25 | – | ppb/°C | ±1.0 ppm F_stab, 0.5°C/min ramp rate, -40 to 105 ºC |
| | | – | ±60 | – | ppb/°C | ±2.5 ppm F_stab, 0.5°C/min ramp rate, -40 to 105 ºC |
| **Dynamic Frequency Change during Temperature Ramp** | F_dynamic | – | ±0.13 | – | ppb/s | ±0.5 ppm F_stab, 0.5°C/min ramp rate, -40 to 105 ºC |
| | | – | ±0.21 | – | ppb/s | ±1.0 ppm F_stab, 0.5°C/min ramp rate, -40 to 105 ºC |
| | | – | ±0.50 | – | ppb/s | ±2.5 ppm F_stab, 0.5°C/min ramp rate, -40 to 105 ºC |
| **One-Year Aging** | F_1y | – | ±1 | – | ppm | At 25°C, after 2-days of continued operation. Aging is measured with respect to day 3. |
| **20-Year Aging** | F_20y | – | ±2 | – | ppm | At 25°C, after 2-days of continued operation. Aging is measured with respect to day 3. |
| **LVCMOS Output Characteristics** | | | | | | |
| **Duty Cycle** | DC | 45 | – | 55 | % | |
| **Rise/Fall Time** | Tr, Tf | – | 1.2 | – | ns | 10% - 90% Vdd |
| **Output Voltage High** | VOH | 90% | – | – | Vdd | IOH = +3mA |
| **Output Voltage Low** | VOL | – | – | 10% | Vdd | IOL = -3mA |
| **Output Impedance** | Z_out_c | – | 20 | – | Ohms | Impedance looking into output buffer |
| **Clipped Sinewave Output Characteristics** | | | | | | |
| **Output Voltage Swing** | V_out | 0.8 | – | 1.2 | V | Clipped sinewave output, 10kΩ \|\| 10 pF ±10% |
| **Rise/Fall Time** | Tr, Tf | – | 3.5 | – | ns | 20% - 80% Vdd, F = 19.2 MHz |
| **Start-up Characteristics** | | | | | | |
| **Start-up Time** | T_start | – | 2.5 | 3.5 | ms | Time to first pulse, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs from 0V to Vdd |
| **Output Enable Time** | T_oe | – | – | 680 | ns | F_nom=10 MHz. See Timing Diagrams section below. |
| **First Pulse Accuracy** | T_stability | – | 5 | – | ms | Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs |

### Table 2. DC Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Supply Voltage** | | | | | | |
| **Supply Voltage** | Vdd | 2.25 | 2.5 | 2.75 | V | Contact SiTime for 2.25V to 3.63V continuous supply voltage support. |
| | | 2.52 | 2.8 | 3.08 | V | |
| | | 2.7 | 3.0 | 3.3 | V | |
| | | 2.97 | 3.3 | 3.63 | V | |
| **Current Consumption** | | | | | | |
| **Current Consumption** | Idd | – | 44 | 53 | mA | F_nom = 19.2 MHz, No Load, TCXO and DCTCXO modes |
| | | – | 48 | 57 | mA | F_nom = 19.2 MHz, No Load, VCTCXO mode |
| **OE Disable Current** | I_od | – | 43 | 51 | mA | OE = GND, output weakly pulled down. TCXO, DCTCXO |
| | | – | 47 | 55 | mA | OE = GND, output weakly pulled down. VCTCXO mode |

### Table 3. Input Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Input Characteristics – OE Pin** | | | | | | |
| **Input Impedance** | Z_in | 75 | – | – | kΩ | Internal pull up to Vdd |
| **Input High Voltage** | VIH | 70% | – | – | Vdd | |
| **Input Low Voltage** | VIL | – | – | 30% | Vdd | |
| **Frequency Tuning Range – Voltage Control or I²C mode** | | | | | | |
| **Pull Range** | PR | ±6.25 | – | – | ppm | VCTCXO mode; contact SiTime for ±12.5 and ±25 ppm. |
| | | ±6.25<br>±10<br>±12.5<br>±25<br>±50<br>±80<br>±100<br>±125<br>±150<br>±200<br>±400<br>±600<br>±800<br>±1200<br>±1600<br>±3200 | – | – | ppm | DCTCXO mode |
| **Absolute Pull Range**[3] | APR | ±2.75 | – | – | ppm | ±0.5 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm |
| | | ±2.25 | – | – | ppm | ±1.0 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm |
| | | ±0.75 | – | – | ppm | ±2.5 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm |
| **Upper Control Voltage** | VC_U | 90% | – | – | Vdd | VCTCXO mode |
| **Lower Control Voltage** | VC_L | – | – | 10% | Vdd | VCTCXO mode |
| **Control Voltage Input Impedance** | VC_z | 8 | – | – | MΩ | VCTCXO mode |
| **Control Voltage Input Bandwidth** | VC_bw | – | 10 | – | kHz | VCTCXO mode; contact SiTime for other bandwidth options |
| **Frequency Control Polarity** | F_pol | | Positive | | | VCTCXO mode |
| **Pull Range Linearity** | PR_lin | – | 0.5 | 1.0 | % | VCTCXO mode |
| **I²C Interface Characteristics, 200 Ohm, 550 pF (Max I²C Bus Load)** | | | | | | |
| **Bus Frequency** | F_I2C | – | 100 | – | kHz | -40 to 105 °C |
| | | – | 400 | – | kHz | -40 to 105 °C |
| | | – | 1000 | – | kHz | -40 to 85 °C |
| **Input Voltage Low** | VIL_I2C | – | – | 30% | Vdd | DCTCXO mode |
| **Input Voltage High** | VIH_I2C | 70% | – | – | Vdd | DCTCXO mode |
| **Output Voltage Low** | VOL_I2C | – | – | 0.4 | V | DCTCXO mode |
| **Input Leakage current** | $I_L$ | 0.5 | – | 24 | µA | 0.1 $V_{DD}$< VOUT < 0.9 $V_{DD}$. Includes typical leakage current from 200 kΩ pull resister to VDD. DCTCXO mode |
| **Input Capacitance** | $C_{IN}$ | – | – | 5 | pF | DCTCXO mode |

**Note:**

3. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature. Refer to Table 17 for APR with respect to other pull range options.

### Table 4. Jitter & Phase Noise – LVCMOS, -40 to 85 °C

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Jitter** | | | | | | |
| **RMS Phase Jitter (random)** | T_phj | – | 0.31 | – | ps | F_nom = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz |
| **RMS Period Jitter** | T_jitt_per | – | 0.8 | – | ps | F_nom = 10 MHz, population 10k |
| **Peak Cycle-to-Cycle Jitter** | T_jitt_cc | – | 6 | – | ps | F_nom = 10 MHz, population 1k, measured as absolute value |
| **Phase Noise** | | | | | | |
| **1 Hz offset** | | – | -80 | – | dBc/Hz | F_nom = 10 MHz<br>TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range |
| **10 Hz offset** | | – | -108 | – | dBc/Hz | |
| **100 Hz offset** | | – | -127 | – | dBc/Hz | |
| **1 kHz offset** | | – | -148 | – | dBc/Hz | |
| **10 kHz offset** | | – | -154 | – | dBc/Hz | |
| **100 kHz offset** | | – | -154 | – | dBc/Hz | |
| **1 MHz offset** | | – | -167 | – | dBc/Hz | |
| **5 MHz offset** | | – | -168 | – | dBc/Hz | |
| **Spurious** | T_spur | – | -112 | – | dBc | F_nom = 10 MHz, 1 kHz to 5 MHz offsets |

### Table 5. Jitter & Phase Noise – Clipped Sinewave, -40 to 85 °C

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Jitter** | | | | | | |
| **RMS Phase Jitter (random)** | T_phj | – | 0.31 | – | ps | F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz |
| **Phase Noise** | | | | | | |
| **1 Hz offset** | | – | -74 | – | dBc/Hz | F_nom = 19.2 MHz<br>TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range |
| **10 Hz offset** | | – | -102 | – | dBc/Hz | |
| **100 Hz offset** | | – | -121 | – | dBc/Hz | |
| **1 kHz offset** | | – | -142 | – | dBc/Hz | |
| **10 kHz offset** | | – | -148 | – | dBc/Hz | |
| **100 kHz offset** | | – | -149 | – | dBc/Hz | |
| **1 MHz offset** | | – | -162 | – | dBc/Hz | |
| **5 MHz offset** | | – | -164 | – | dBc/Hz | |
| **Spurious** | T_spur | – | -109 | – | dBc | F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets |

### Table 6. Jitter & Phase Noise – LVCMOS, -40 to 105 °C

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Jitter** | | | | | | |
| **RMS Phase Jitter (random)** | T_phj | – | 0.31 | – | ps | F_nom = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz |
| **RMS Period Jitter** | T_jitt_per | – | 0.8 | – | ps | F_nom = 10 MHz, population 10k |
| **Peak Cycle-to-Cycle Jitter** | T_jitt_cc | – | 6 | – | ps | F_nom = 10 MHz, population 1k, measured as absolute value |
| **Phase Noise** | | | | | | |
| **1 Hz offset** | | – | -80 | – | dBc/Hz | F_nom = 10 MHz<br>TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range. |
| **10 Hz offset** | | – | -108 | – | dBc/Hz | |
| **100 Hz offset** | | – | -127 | – | dBc/Hz | |
| **1 kHz offset** | | – | -148 | – | dBc/Hz | |
| **10 kHz offset** | | – | -154 | – | dBc/Hz | |
| **100 kHz offset** | | – | -154 | – | dBc/Hz | |
| **1 MHz offset** | | – | -167 | – | dBc/Hz | |
| **5 MHz offset** | | – | -168 | – | dBc/Hz | |
| **Spurious** | T_spur | – | -112 | – | dBc | F_nom = 10 MHz, 1 kHz to 5 MHz offsets, Vdd=2.5V |
| | | – | -112 | – | dBc | F_nom = 10 MHz, 1 kHz to 5 MHz offsets, Vdd=2.8V, 3.0V, 3.3V |

### Table 7. Jitter & Phase Noise – Clipped Sinewave, -40 to 105 °C

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Jitter** | | | | | | |
| **RMS Phase Jitter (random)** | T_phj | – | 0.31 | – | ps | F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz |
| **Phase Noise** | | | | | | |
| **1 Hz offset** | | – | -74 | – | dBc/Hz | F_nom = 19.2 MHz<br>TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range |
| **10 Hz offset** | | – | -102 | – | dBc/Hz | |
| **100 Hz offset** | | – | -121 | – | dBc/Hz | |
| **1 kHz offset** | | – | -142 | – | dBc/Hz | |
| **10 kHz offset** | | – | -148 | – | dBc/Hz | |
| **100 kHz offset** | | – | -149 | – | dBc/Hz | |
| **1 MHz offset** | | – | -162 | – | dBc/Hz | |
| **5 MHz offset** | | – | -164 | – | dBc/Hz | |
| **Spurious** | T_spur | – | -109 | – | dBc | F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets |

### Table 8. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Test Conditions | Value | Unit |
|---|---|---|---|
| **Storage Temperature** | | -65 to 125 | °C |
| **Continuous Power Supply Voltage Range (Vdd)** | | -0.5 to 4 | V |
| **Human Body Model (HBM) ESD Protection** | JESD22-A114 | 2000 | V |
| **Soldering Temperature (follow standard Pb-free soldering guidelines)** | | 260 | °C |
| **Junction Temperature[4]** | | 130 | °C |

**Note:**
4. Exceeding this temperature for an extended period of time may damage the device.

### Table 9. Thermal Considerations[5]

| Package | θJA (°C/W) | θJC, Bottom (°C/W) |
|---|---|---|
| **Ceramic 5.0 x 3.2 mm²** | 54 | 15 |

**Note:**
5. Measured in still air.

### Table 10. Maximum Operating Junction Temperature[6]

| Max Operating Temperature (ambient) | Maximum Operating Junction Temperature |
|---|---|
| **70°C** | **80°C** |
| **85°C** | **95°C** |
| **105°C** | **115°C** |

**Note:**
6. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

### Table 11. Environmental Compliance

| Parameter | Test Conditions | Value | Unit |
|---|---|---|---|
| **Mechanical Shock Resistance** | **MIL-STD-883F, Method 2002** | **30000** | *g* |
| **Mechanical Vibration Resistance** | **MIL-STD-883F, Method 2007** | **70** | *g* |
| **Temperature Cycle** | **JESD22, Method A104** | – | – |
| **Solderability** | **MIL-STD-883F, Method 2003** | – | – |
| **Moisture Sensitivity Level** | **MSL1 @260°C** | – | – |

## Device Configurations and Pin-outs

### Table 12. Device Configurations

| Configuration | Pin 1 | Pin 5 | I²C Programmable Parameters |
|---|---|---|---|
| TCXO | OE/NC | NC | – |
| VCTCXO | VC | NC | – |
| DCTCXO | OE/NC | A0/NC | Frequency Pull Range, Frequency Pull Value, Output Enable control. |

### Pin-out Top Views

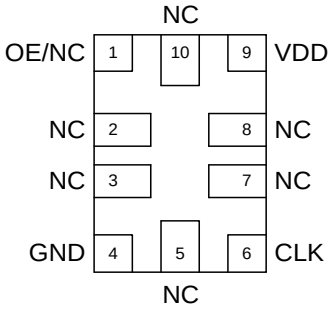



**Figure 3. TCXO**

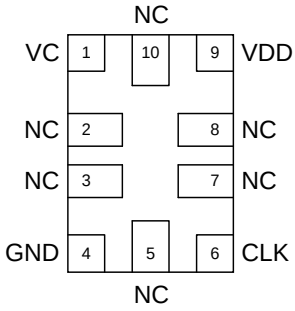



**Figure 4. VCTCXO**

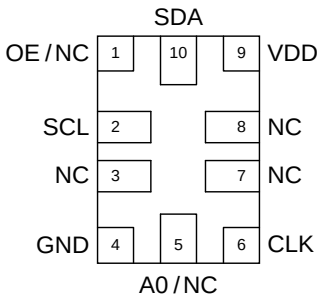



**Figure 5. DCTCXO**

### Table 13. Pin Description

| Pin | Symbol | I/O | Internal Pull-up/Pull Down Resistor | Function |
|---|---|---|---|---|
| 1 | OE/NC/VC | OE – Input | 100 kΩ Pull-Up | H[7]: specified frequency output<br>L: output is high impedance. Only output driver is disabled. |
| | | NC[8] – No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| | | VC – Input | – | Control Voltage in VCTCXO Mode |
| 2 | SCL / NC[8] | SCL – Input | 200 kΩ Pull-Up | I²C serial clock input. |
| | | No Connect | | H or L or Open: No effect on output frequency or other device functions |
| 3 | NC[8] | No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| 4 | GND | Power | – | Connect to ground |
| 5 | A0 / NC[8] | A0 – Input | 100 kΩ Pull-Up | Device I²C address when the address selection mode is via the A0 pin. This pin is NC when the I²C device address is specified in the ordering code.<br>A0 Logic Level — I²C Address<br>0 — 1100010<br>1 — 1101010 |
| | | NC – No Connect | – | H or L or Open: No effect on output frequency or other device functions. |
| 6 | CLK | Output | – | LVCMOS, or clipped sinewave oscillator output |
| 7 | NC[8] | No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| 8 | NC[8] | No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| 9 | VDD | Power | – | Connect to VDD[8] |
| 10 | SDA / NC[8] | SDA – Input/Output | 200 kΩ Pull Up | I²C Serial Data. |
| | | NC – No Connect | – | H or L or Open: No effect on output frequency or other device functions. |

**Notes:**

7. In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
8. A 0.1 µF capacitor in parallel with a 10 µF capacitor are required between Vdd and GND. The 0.1 µF capacitor is recommended to place close to the device, and place the 10 µF capacitor less than 2 inches away.
9. All NC pins can be left floating and do not need to be soldered down.

## Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs

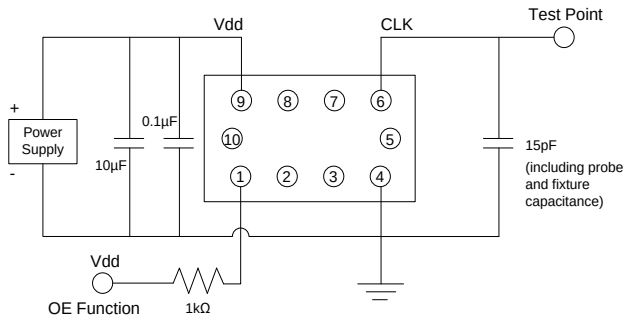



**Figure 6. LVCMOS Test Circuit (OE Function)**

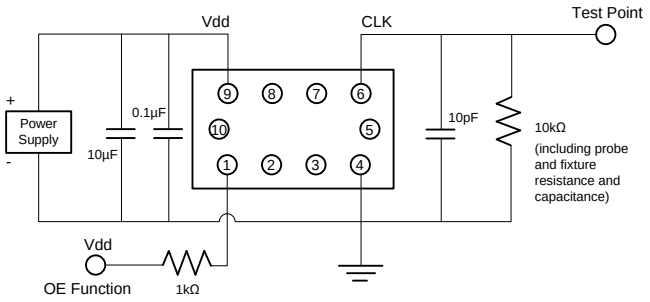



**Figure 7. Clipped Sinewave Test Circuit (OE Function) for AC and DC Measurements**

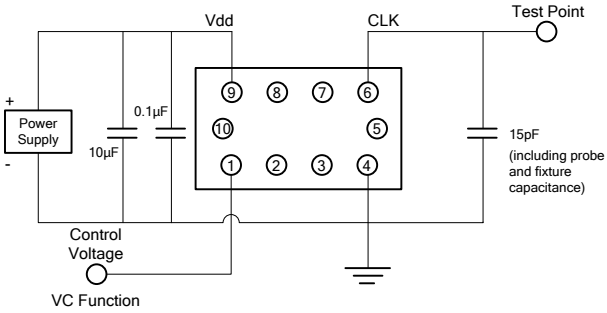



**Figure 8. LVCMOS Test Circuit (VC Function)**

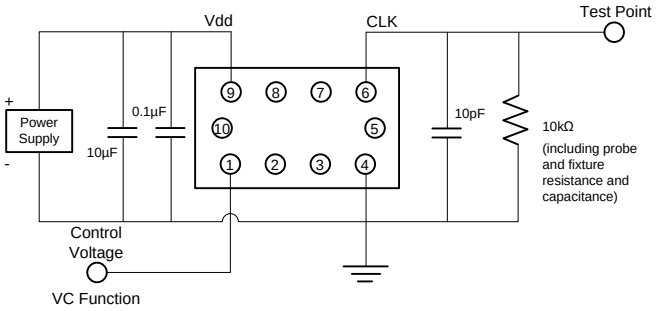



**Figure 9. Clipped Sinewave Test Circuit (VC Function) for AC and DC Measurements**

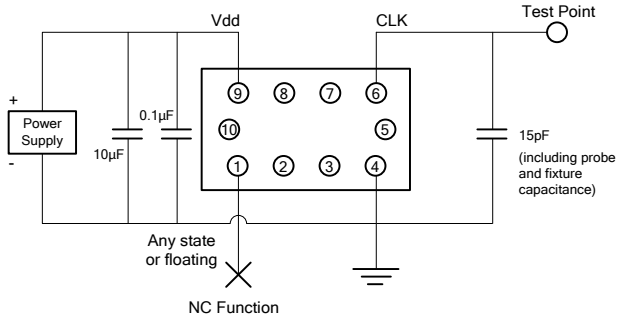



**Figure 10. LVCMOS Test Circuit (NC Function)**

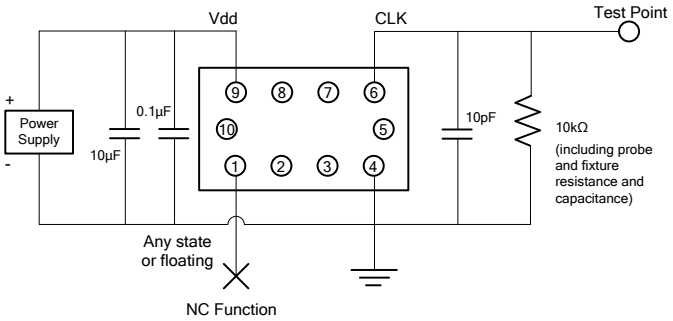



**Figure 11. Clipped Sinewave Test Circuit (NC Function) for AC and DC Measurements**

## Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs (continued)

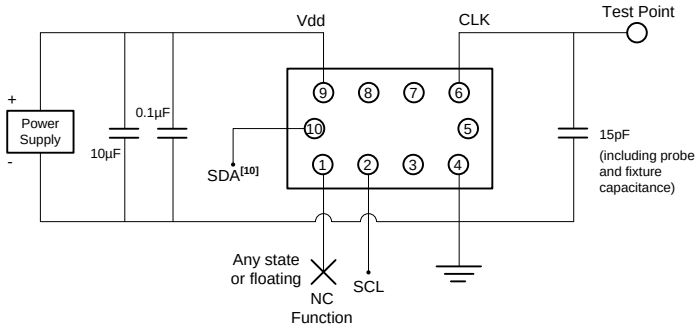



**Figure 12. LVCMOS Test Circuit (I²C Control), DCTCXO mode**

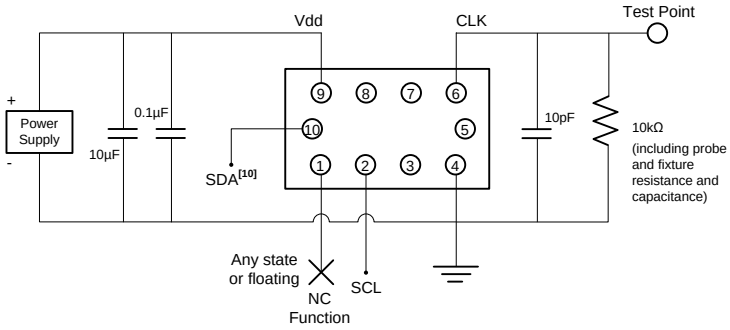



**Figure 13. Clipped Sinewave Test Circuit (I²C Control), DCTCXO mode for AC and DC Measurements**

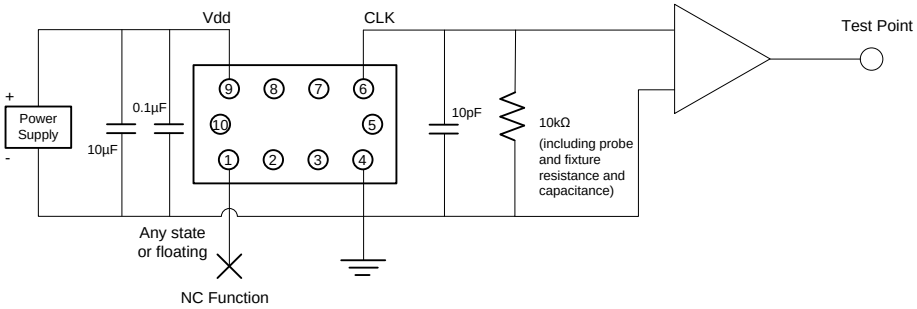



**Figure 14. Clipped Sinewave Test Circuit for Phase Noise Measurements, Applies to All Configurations (NC Function shown for example only)**

**Note:**

10. SDA is open-drain and may require pull-up resistor if not present in I²C test setup.

## Waveforms

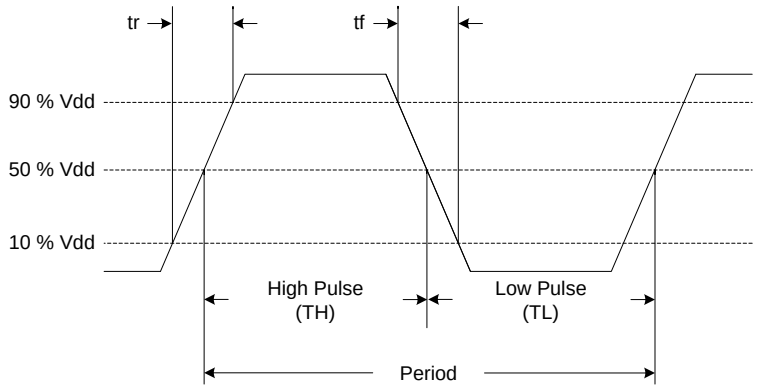



**Figure 15. LVCMOS Waveform Diagram[11]**

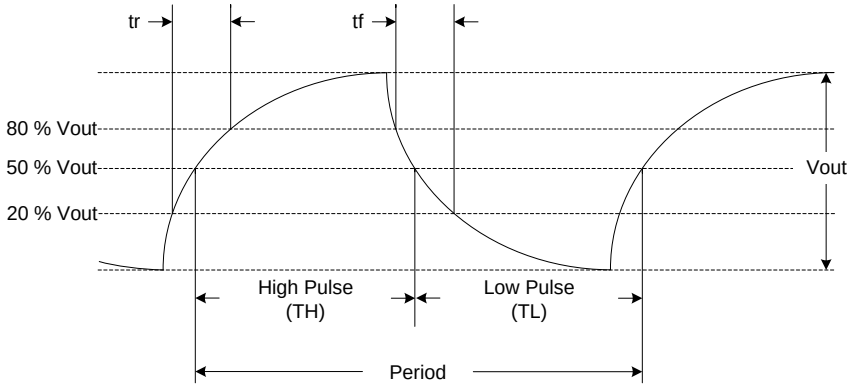
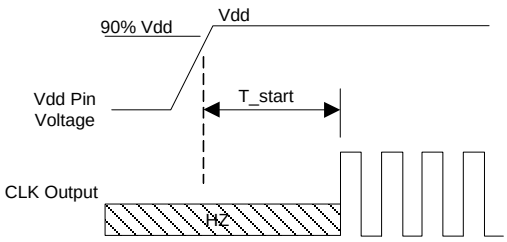



**Figure 16. Clipped Sinewave Waveform Diagram[11]**

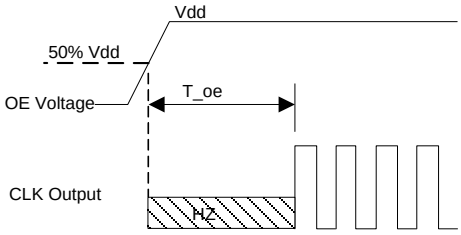
**Note:**
11. Duty Cycle is computed as Duty Cycle = TH/Period.

## Timing Diagrams




T_start: Time to start from power-off

**Figure 17. Startup Timing**




T_oe: Time to re-enable the clock output

**Figure 18. OE Enable Timing (OE Mode Only)**

## Typical Performance Plots

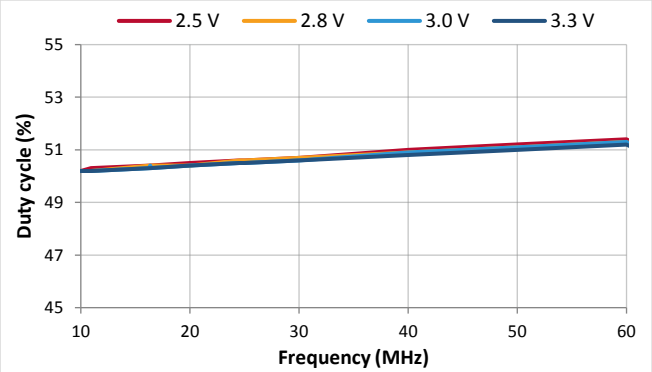



**Figure 19. Duty Cycle (LVCMOS)**

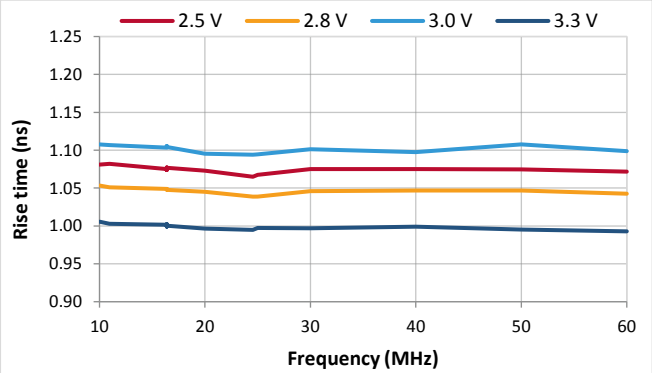



**Figure 20. Rise Time (LVCMOS)**

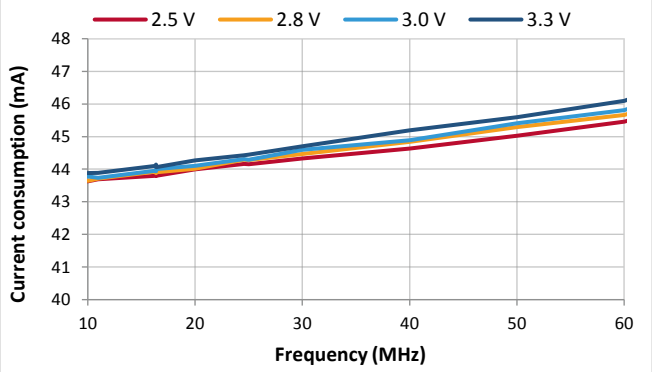



**Figure 21. IDD TCXO (LVCMOS)**

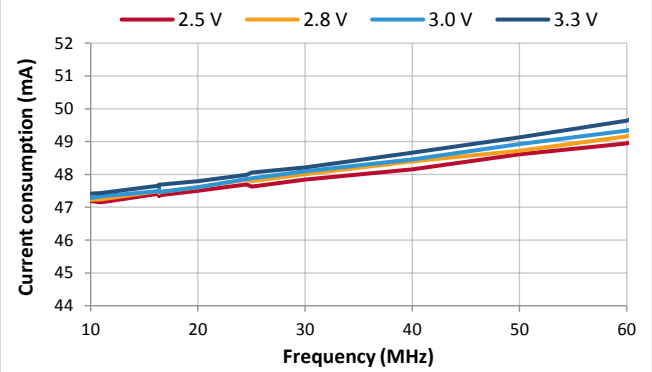



**Figure 22. IDD VCTCXO (LVCMOS)**

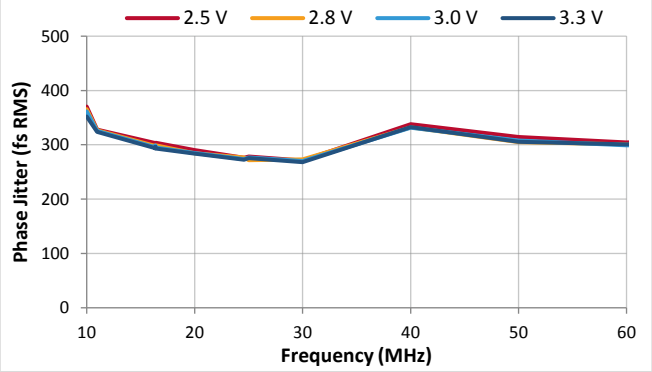



**Figure 23. RMS Phase Jitter, (DC)TCXO (LVCMOS)**

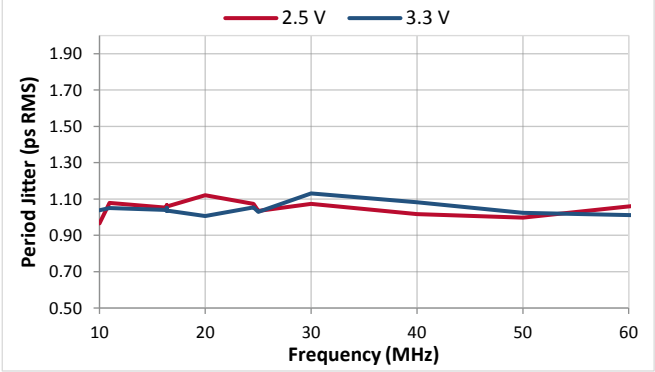



**Figure 24. RMS Period Jitter (LVCMOS)**

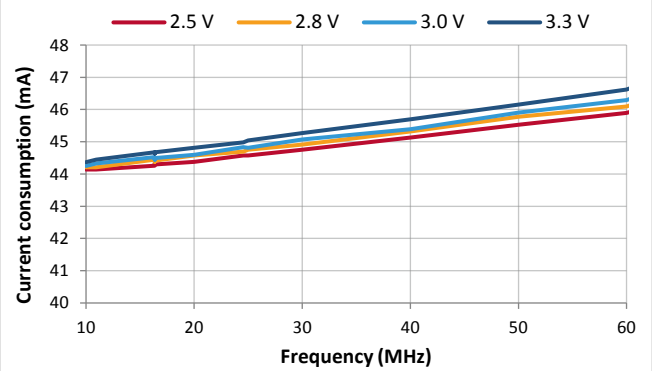



**Figure 25. IDD DCTCXO (LVCMOS)**

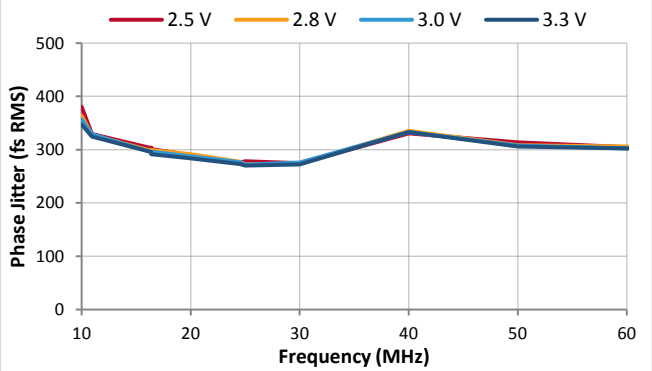



**Figure 26. RMS Phase Jitter, VCTCXO (LVCMOS)**

## Typical Performance Plots (continued)

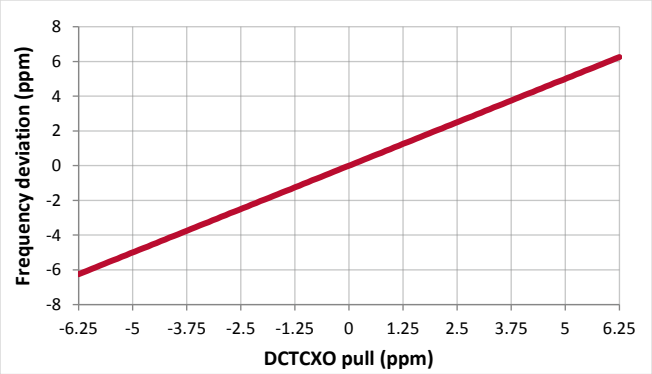



**Figure 27. DCTCXO frequency pull characteristic**

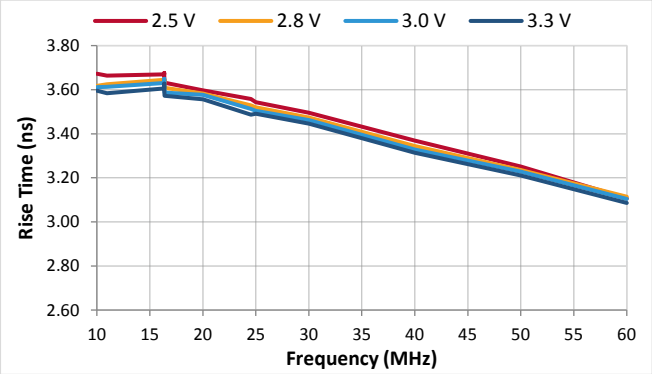



**Figure 28. Rise Time (Clipped Sinewave)**

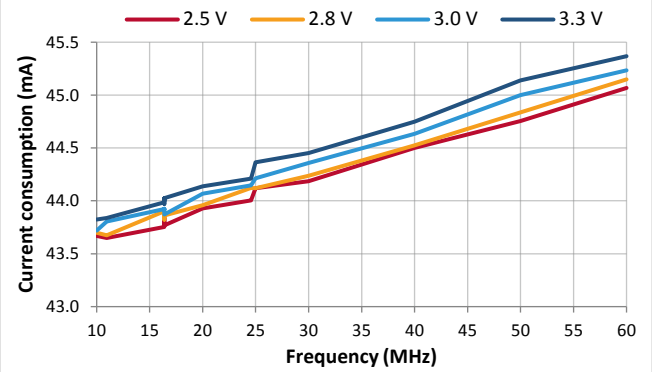



**Figure 29. IDD TCXO (Clipped Sinewave)**

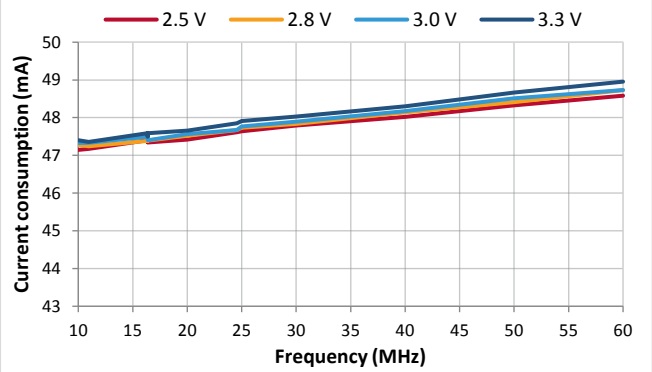



**Figure 30. IDD VCTCXO (Clipped Sinewave)**

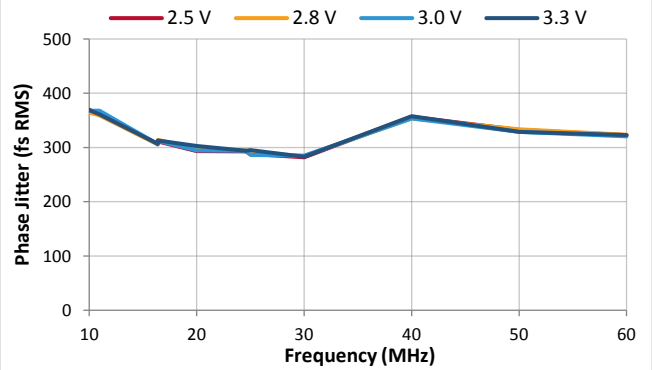



**Figure 31. RMS Phase Jitter, (DC)TCXO (Clipped Sine)**

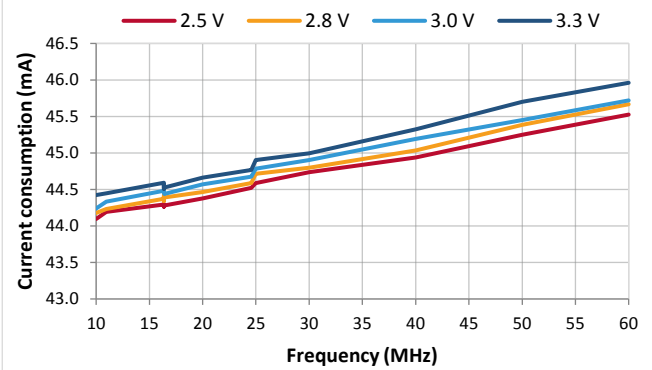



**Figure 32. IDD DCTCXO (Clipped Sinewave)**

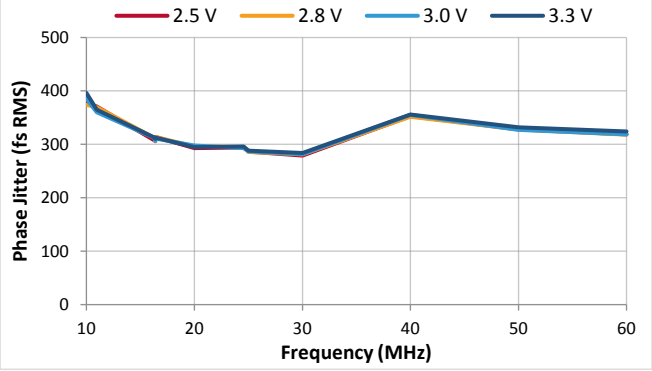



**Figure 33. RMS Phase Jitter, VCTCXO (Clipped Sine)**

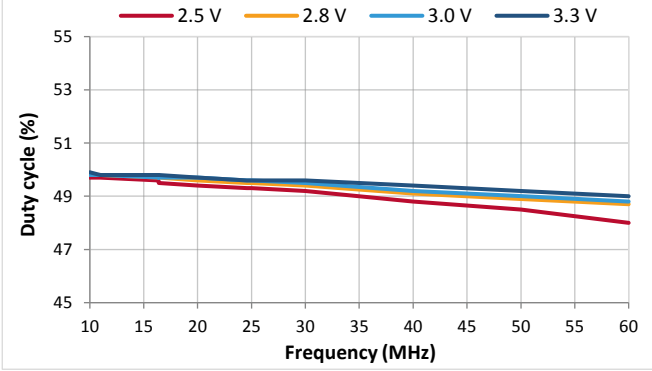



**Figure 34. Duty Cycle (Clipped Sinewave)**

## Architecture Overview

Based on SiTime's innovative Elite Platform™, the SiT5186 delivers exceptional dynamic performance, i.e. resilience to environmental stressors such as shock, vibration, and fast temperature transients. Underpinning the Elite platform are SiTime's unique DualMEMS™ temperature sensing architecture and TurboCompensation™ technologies.

DualMEMS is a noiseless temperature compensation scheme. It consists of two MEMS resonators fabricated on the same die substrate. The TempFlat™ resonator is designed with a flat frequency characteristic over temperature whereas the temperature sensing resonator is by design sensitive to temperature changes. The ratio of frequencies between these two resonators provides an accurate reading of the resonator temperature with 20 µK resolution.

By placing the two MEMS resonators on the same die, this temperature sensing scheme eliminates any thermal lag and gradients between resonator and temperature sensor, thereby overcoming an inherent weakness of legacy quartz TCXOs.

The DualMEMS temperature sensor drives a state-of-the-art CMOS temperature compensation circuit. The TurboCompensation design, with >100 Hz compensation bandwidth, achieves a dynamic frequency stability that is far superior to any quartz TCXO. The digital temperature compensation enables additional optimization of frequency stability and frequency slope over temperature within any chosen temperature range for a given system design.

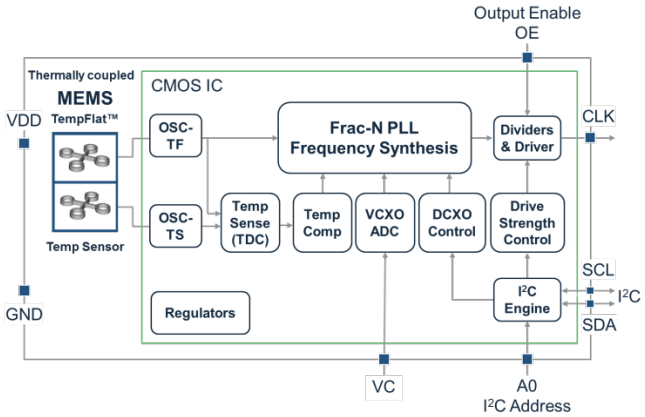



**Figure 35. Elite Architecture**

The Elite platform also incorporates a high resolution, low noise frequency synthesizer along with the industry standard I²C bus. This unique combination enables system designers to digitally control the output frequency in steps as low as 5 ppt and over a wide range up to ±3200 ppm.

For more information regarding the Elite platform and its benefits please visit:

- SiTime's breakthroughs section
- TechPaper: DualMEMS Temperature Sensing Technology
- TechPaper: DualMEMS Resonator TDC

## Functional Overview

The SiT5186 is designed for maximum flexibility with an array of factory programmable options, enabling system designers to configure this precision device for optimal performance in a given application.

### Frequency Stability

The SiT5186 comes in three factory-trimmed stability grades.

**Table 14. Stability Grades vs. Ordering Codes**

| Frequency Stability Over Temperature | Ordering Code |
|---|---|
| ±0.5 ppm | K |
| ±1.0 ppm | A |
| ±2.5 ppm | D |

### Output Frequency and Format

The SiT5186 can be factory programmed for an output frequency without sacrificing lead time or incurring an upfront customization cost typically associated with custom-frequency quartz TCXOs.

The device supports both LVCMOS and clipped sinewave output. Ordering codes for the output format are shown below:

**Table 15. Output Formats vs. Ordering Codes**

| Output Format | Ordering Code |
|---|---|
| LVCMOS | "-" |
| Clipped Sinewave | "C" |

### Output Frequency Tuning

In addition to the non-pullable TCXO, the SiT5186 can also support output frequency tuning through either an analog control voltage (VCTCXO), or I²C interface (DCTCXO). The I²C interface enables 16 factory programmed pull-range options from ±6.25 ppm to ±3200 ppm. The pull range can also be reprogrammed via I²C to any supported pull-range value.

Refer to Device Configuration section for details.

### Pin 1 Configuration (OE, VC, or NC)

Pin 1 of the SiT5186 can be factory programmed to support three modes: Output Enable (OE), Voltage Control (VC), or No Connect (NC).

**Table 16. Pin Configuration Options**

| Pin 1 Configuration | Operating Mode | Output |
|---|---|---|
| OE | TCXO/DCTCXO | Active or High-Z |
| NC | TCXO/DCTCXO | Active |
| VC | VCTCXO | Active |

When pin 1 is configured as OE pin, the device output is guaranteed to operate in one of the following two states:

- Clock output with the frequency specified in the part number when Pin 1 is pulled to logic high
- Hi-Z mode with weak pull down when pin 1 is pulled to logic low.

When pin 1 is configured as NC, the device is guaranteed to output the frequency specified in the part number at all times, regardless of the logic level on pin 1.

In the VCTCXO configuration, the user can fine-tune the output frequency from the nominal frequency specified in the part number by varying the pin 1 voltage. The guaranteed allowable variation of the output frequency is specified as pull range. A VCTCXO part number must contain a valid pull-range ordering code.

## Device Configurations

The SiT5186 supports 3 device configurations – TCXO, VCTCXO, and DCTCXO. The TCXO and VCTCXO options are directly compatible with the quartz TCXO and VCTCXO. The DCTCXO configuration provides performance enhancement by eliminating VCTCXO's sensitivity to control voltage noise with an $I^2C$ digital interface for frequency tuning.

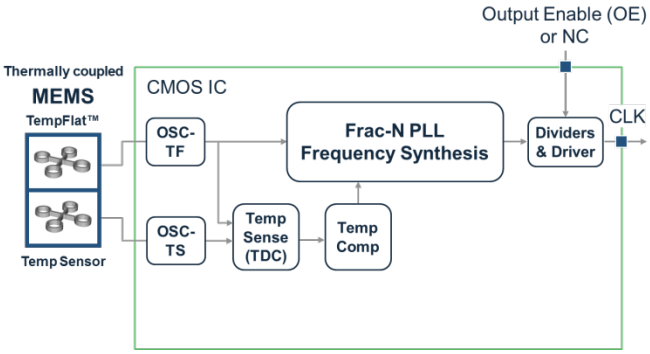



**Figure 36. Block Diagram – TCXO**

### TCXO Configuration

The TCXO configuration generates a fixed frequency output, as shown in Figure 36. The frequency is specified by the user in the frequency field of the device ordering code and then factory programmed. Other factory programmable options include supply voltage, output types (LVCMOS or clipped sinewave), and pin 1 functionality (OE or NC).

Refer to the Ordering Information section at the end of the datasheet for a list of all ordering options.

## VCTCXO Configuration

A VCTCXO, shown in Figure 37, is a frequency control device whose output frequency is an approximately linear function of control voltage applied to the voltage control pin. VCTCXOs have a number of use cases including the VCO portion of a jitter attenuation/jitter cleaner PLL Loop.

The SiT5186 achieves a 10x better pull range linearity of <0.5% via a high-resolution fractional PLL compared with 5% to 10% typical of quartz VCTCXOs that rely on pulling a resonator. By contrast, quartz-based VCTCXOs change output frequency by varying the capacitive load of a crystal resonator using varactor diodes, which results in poor linearity.

Note that the output frequency of the VCTCXO is proportional to the analog control voltage applied to pin 1. Because this control signal is analog and directly controls the output frequency, care must be taken to minimize noise on this pin.

The nominal output frequency is factory programmed per the customer's request to 6 digits of precision and is defined as the output frequency when the control voltage equals Vdd/2. The maximum output frequency variation from this nominal value is set by the pull range, which is also factory programmed to the customer's desired value and specified by the ordering code. The Ordering Information section shows all ordering options and associated ordering codes.

Refer to VCTCXO-Specific Design Considerations for more information on critical VCTCXO parameters including pull range linearity, absolute pull range, control voltage bandwidth, and Kv.

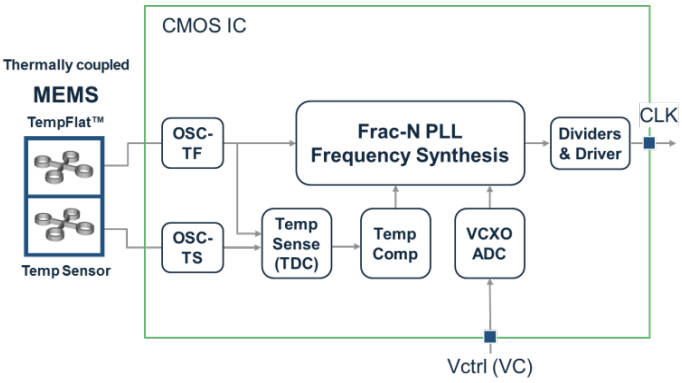



**Figure 37. Block Diagram – VCTCXO**

## DCTCXO Configuration

The SiT5186 offers digital control of the output frequency, as shown in Figure 38. The output frequency is controlled by writing frequency control words over the I²C interface.

There are several advantages of DCTCXOs relative to VCTCXOs:

1) Frequency control resolution as low as 5 ppt. This high resolution minimizes accumulated time error in synchronization applications.
2) Lower system cost – A VCTCXO may need a Digital to Analog Converter (DAC) to drive the control voltage input. In a DCTXCO, the frequency control is achieved digitally by register writes to the control registers via I²C, thereby eliminating the need for a DAC.
3) Better noise immunity – The analog signal used to drive the voltage control pin of a VCTCXO can be sensitive to noise, and the trace over which the signal is routed can be susceptible to noise coupling from the system. The DCTCXO does not suffer from analog noise coupling since the frequency control is performed digitally through I²C.
4) No frequency-pull non-linearity – The frequency pulling is achieved via fractional feedback divider of the PLL, eliminating any pull non-linearity concerns typical of quartz-based VCTCXOs. This improves dynamic performance in closed-loop applications.
5) Programmable wide pull range – The DCTCXO pulling mechanism is via the fractional feedback divider and is therefore not constrained by resonator pullability as in quartz-based solutions. The SiT5186 offers 16 frequency pull-range options from ±6.25ppm to ±3200ppm, providing system designers great flexibility.

Refer to DCTCXO-Specific Design Considerations for more information on critical DCTCXO parameters including pull range, absolute pull range, frequency output, and I²C control registers.

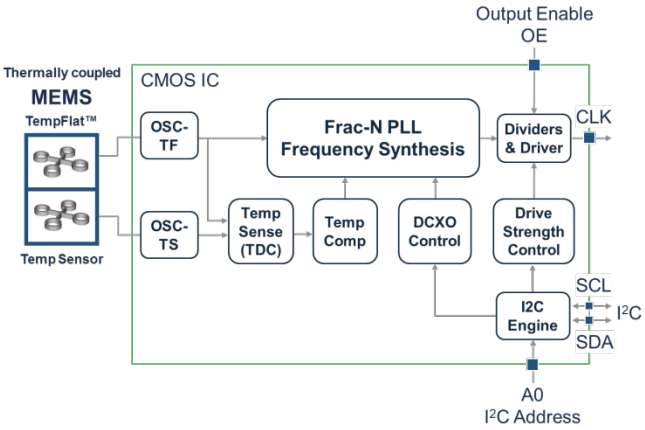



**Figure 38. Block Diagram**

## VCTCXO-Specific Design Considerations

### Linearity

In any VCTCXO, there will be some deviation of the frequency-voltage (FV) characteristic from an ideal straight line. Linearity is the ratio of this maximum deviation to the total pull range, expressed as a percentage. Figure 39 below shows the typical pull linearity of a SiTime VCTCXO. The linearity is excellent (1% maximum) relative to most quartz offerings because the frequency pulling is achieved with a PLL rather than varactor diodes.

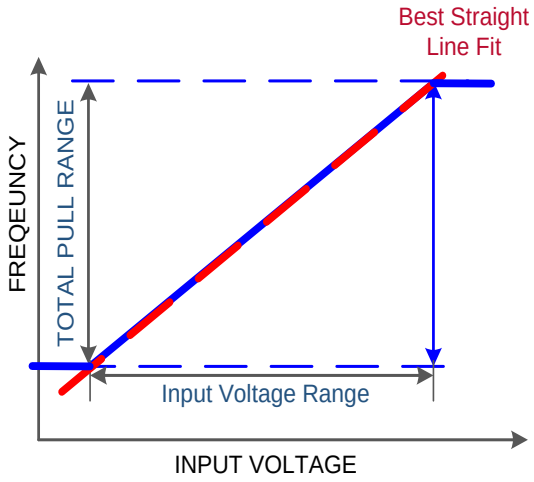



**Figure 39. Typical SiTime VCTCXO Linearity**

### Control Voltage Bandwidth

Control voltage bandwidth, sometimes called "modulation rate" or "modulation bandwidth", indicates how fast a VCO can respond to voltage changes at its input. The ratio of the output frequency variation to the input voltage variation, previously denoted by $K_V$, has a low-pass characteristic in most VCTCXOs. The control voltage bandwidth equals the modulating frequency where the output frequency deviation equals 0.707 (e.g. -3 dB) of its DC value, for DC inputs swept in the same voltage range.

For example, a part with a ±6.25 ppm pull range and a 0-3V control voltage can be regarded as having an average KV of 4.17 ppm/V (12.5 ppm/3V = 4.17 ppm/V). Applying an input of 1.5V DC ± 0.5V (1.0 V to 2.0V) causes an output frequency change of 4.17 ppm (±2.08 ppm). If the control voltage bandwidth is specified as 10 kHz, the peak-to-peak value of the output frequency change will be reduced to 4.33 ppm/√2 or 2.95 ppm, as the frequency of the control voltage change is increased to 10 kHz.

### FV Characteristic Slope $K_V$

The slope of the FV characteristic is a critical design parameter in many low bandwidth PLL applications. The slope is the derivative of the FV characteristic – the deviation of frequency divided by the control voltage change needed to produce that frequency deviation, over a small voltage span, as shown below:

$$K_V = \frac{\Delta f_{out}}{\Delta V_{in}}$$

It is typically expressed in kHz/Volt, MHz/Volt, ppm/Volt, or similar units. This slope is usually called "$K_V$" based on terminology used in PLL designs.

The extreme linear characteristic of the SiTime SiT5186 VCTCXO family means that there is very little $K_V$ variation across the whole input voltage range (typically <1%), significantly reducing the design burden on the PLL designer. Figure 40 below illustrates the typical $K_V$ variation.

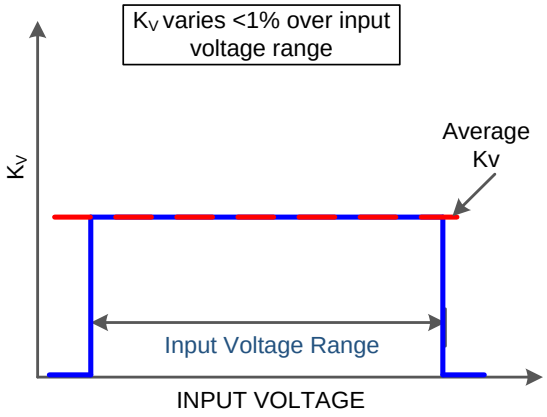



**Figure 40. Typical SiTime $K_V$ Variation**

### Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control voltage over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability, tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$APR = PR - F_{stability} - F_{aging}$$

where $F_{stability}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load.

Figure 41 shows a typical SiTime VCTCXO FV characteristic. The FV characteristic varies with conditions, so that the frequency output at a given input voltage can vary by as much as the specified frequency stability of the VCTCXO. For such VCTCXOs, the frequency stability and APR are independent of each other. This allows very wide range of pull options without compromising frequency stability.

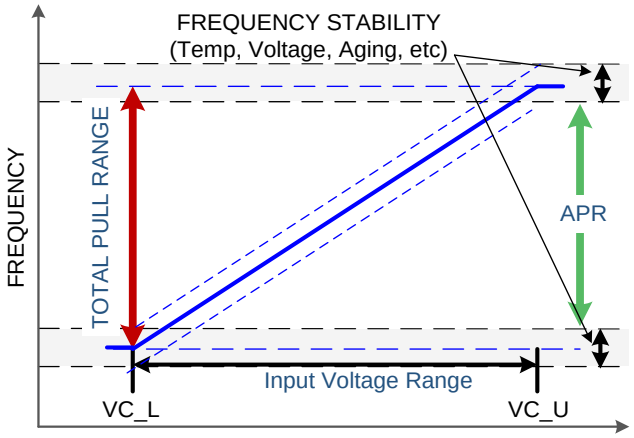



**Figure 41. Typical SiTime VCTCXO FV Characteristic**

The upper and lower control voltages are the specified limits of the input voltage range as shown in Figure 41 above. Applying voltages beyond the upper and lower voltages do not result in noticeable changes of output frequency. In other words, the FV characteristic of the VCTCXO saturates beyond these voltages. Figures 1 and 2 show these voltages as Lower Control Voltage (VC_L) and Upper Control Voltage (VC_U).

Table 17 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

**Table 17. VCTCXO Pull Range, APR Options[12]** Typical unless specified otherwise. Pull range (PR) is ±6.25 ppm.

| Pull Range Ordering Code | Device Option(s) | APR ppm ±0.5 ppm option ±2 ppm 20-year aging | APR ppm ±1.0 ppm option ±2 ppm 20-year aging | APR ppm ±2.5 ppm option ±2 ppm 20-year aging |
|---|---|---|---|---|
| T | VCTCXO | ±2.75 | ±2.25 | ±0.7 |

**Notes:**
12. APR includes initial tolerance, frequency stability vs. temperature, and the corresponding 20-year aging.

# DCTCXO-Specific Design Considerations

## Pull Range and Average Pull Range

Pull range and absolute pull range are described in the previous section. Table 18 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

**Table 18. APR Options[13]**

| Pull Range Ordering Code | Pull Range ppm | APR ppm ±0.5 ppm option ±2 ppm 20-year aging | APR ppm ±1.0 ppm option ±2 ppm 20-year aging | APR ppm ±2. 5 ppm option ±2 ppm 20-year aging |
|---|---|---|---|---|
| T | ±6.25 | ±2.75 | ±2.97 | ±0.75 |
| R | ±10 | ±6.50 | ±6.0 | ±4.5 |
| Q | ±12.5 | ±9.0 | ±8.5 | ±7.0 |
| M | ±25 | ±21.5 | ±21.0 | ±19.5 |
| B | ±50 | ±46.5 | ±46.0 | ±44.5 |
| C | ±80 | ±76.5 | ±76.0 | ±74.5 |
| E | ±100 | ±96.5 | ±96.0 | ±94.5 |
| F | ±125 | ±121.5 | ±121.0 | ±119.5 |
| G | ±150 | ±146.5 | ±146.0 | ±144.5 |
| H | ±200 | ±196.5 | ±196.0 | ±194.5 |
| X | ±400 | ±396.5 | ±396.0 | ±394.5 |
| L | ±600 | ±596.5 | ±596.0 | ±594.5 |
| Y | ±800 | ±796.5 | ±796.0 | ±794.5 |
| S | ±1200 | ±1196.5 | ±1196.0 | ±1194.5 |
| Z | ±1600 | ±1596.5 | ±1596.0 | ±1594.5 |
| U | ±3200 | ±3196.5 | ±3196.0 | ±3194.5 |

**Notes:**
13. APR includes initial tolerance, frequency stability vs. temperature, and the corresponding 20-year aging.

## Output Frequency

The device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up both pull range and output frequency can be controlled via $I^2C$ writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The pull range is specified by the value loaded in the digital pull-range control register. The 16 pull range choices are specified in the control register and range from ±6.25ppm to ±3200ppm.

Table 19 below shows the frequency resolution versus pull range programmed value

**Table 19. Frequency Resolution versus Pull Range**

| Programmed Pull Range | Frequency Resolution |
|---|---|
| ±6.25ppm | $5x10^{-12}$ |
| ±10ppm | $5x10^{-12}$ |
| ±12.5ppm | $5x10^{-12}$ |
| ±25ppm | $5x10^{-12}$ |
| ±50ppm | $5x10^{-12}$ |
| ±80ppm | $5x10^{-12}$ |
| ±100ppm | $5x10^{-12}$ |
| ±120ppm | $5x10^{-12}$ |
| ±150ppm | $5x10^{-12}$ |
| ±200ppm | $5x10^{-12}$ |
| ±400ppm | $1x10^{-11}$ |
| ±600ppm | $1.4x10^{-11}$ |
| ±800ppm | $2.1x10^{-11}$ |
| ±1200ppm | $3.2x10^{-11}$ |
| ±1600ppm | $4.7x10^{-11}$ |
| ±3200ppm | $9.4x10^{-11}$ |

The ppm frequency offset is specified by the 26 bit DCXO frequency control register in two's complement format as described in the $I^2C$ Register Descriptions. The power up default value is 00000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to 0x00[15:0] (Least Significant Word) and 0x01[9:0] (Most Significant Word). The LSW value should be written first followed by the MSW value; the frequency change is initiated after the MSW value is written.

| Bits | 25:24 | 23:20 | 19:16 | 15:12 | 11:8 | 7:4 | 3:0 |
|---|---|---|---|---|---|---|---|
| Value (Hex) | 01 | 1111 | 1111 | 1111 | 1111 | 1111 | 1111 |
| Dec. Value | $2^{25}$ -1 = 33,554,431 | | | | | | |

| Bits | 25:24 | 23:20 | 19:16 | 15:12 | 11:8 | 7:4 | 3:0 |
|---|---|---|---|---|---|---|---|
| Value (Hex) | 00 | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 |
| Dec. Value | 0 | | | | | | |

| Bits | 25:24 | 23:20 | 19:16 | 15:12 | 11:8 | 7:4 | 3:0 |
|---|---|---|---|---|---|---|---|
| Value (Hex) | 10 | 0000 | 0000 | 0000 | 0000 | 0000 | 0000 |
| Dec. Value | -($2^{25}$) = -33,554,432 | | | | | | |

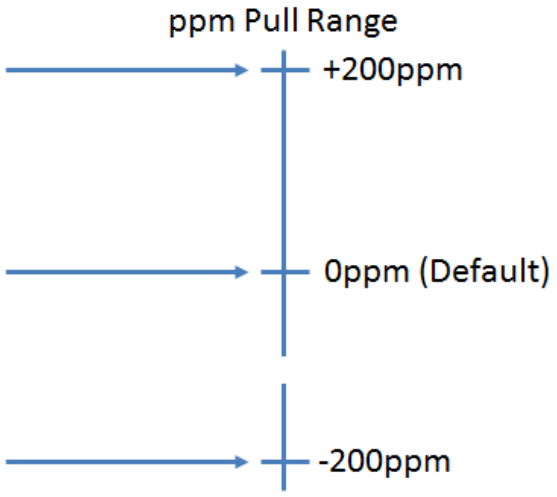



**Figure 42. Pull Range and Frequency Control Word**

Figure 42 shows how the two's complement signed value of the frequency control word sets the output frequency within the ppm pull range set by 0x02:[3:0]. This example shows use of the ±200 ppm pull range. Therefore, to set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, convert to two's complement binary, and then write these values to the frequency control registers.

The following formula generates the control word value:

**Control word value = RND(($2^{25}$-1) × ppm shift from nominal/pull range),** where RND is the rounding function which rounds the number to the nearest whole number. Two examples follow, assuming a ±200 ppm pull range:

**Example 1:**

- Default Output Frequency = 19.2 MHz
- Desired Output Frequency = 19.201728 MHz (+90 ppm)

$2^{25}$-1 corresponds to +200 ppm, and the fractional value required for +90 ppm can be calculated as follows.

- 90 ppm / 200 ppm × ($2^{25}$-1) = 15,099,493.95.

Rounding to the nearest whole number yields 15,099,494 and converting to two's complement gives a binary value of 111001100110011001100110, or E66666 in hex.

**Example 2:**

- Default Output Frequency = 10 MHz
- Desired Output Frequency = 9.998 MHz (-50 ppm)

Following the formula shown above,

- (-50 ppm / 200 ppm) × ($2^{25}$-1) = -8,388,607.75.

Rounding this to the nearest whole number results in -8,388,608.

Converting this to two's complement binary results in 111000000000000000000000000, or 3800000 in hex.

To summarize, the procedure for calculating the frequency control word associated with a given ppm offset is as follows:

1) Calculate the fraction of the half-pull range needed. For example, if the total pull range is set for ±100 ppm and a +20 ppm shift from the nominal frequency is needed, this fraction is 20 ppm/100 ppm = 0.2
2) Multiply this fraction by the full-half scale word value, $2^{25}$-1 = 33,554,431, round to the nearest whole number, and convert the result to two's complement binary. Following the +20ppm example, this value is 0.2 × 33,554,431 = 6,710,886.2 and rounded to 6,710,886.
3) Write the two's complement binary value starting with the Least Significant Word (LSW) 0x00[16:0], followed by the Most Significant Word (MSW), 0x01[9:0]. If the user desires that the output remains enabled while changing the frequency, a 1 must also be written to the OE control bit 0x01[10] if the device has software OE Control Enabled.

It is important to note that the maximum Digital Control update rate is 38 kHz regardless of $I^2C$ bus speed.

## I²C Control Registers

The SiT5186 enables control of frequency pull range, frequency pull value, and Output Enable via I²C writes to the control registers. Table 20 below shows the register map summary, and detailed register descriptions follow.

**Table 20. Register Map Summary**

| Address | Bits | Access | Description |
|---|---|---|---|
| 0x00 | [15:0] | RW | DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW) |
| 0x01 | [15:11] | R | NOT USED |
| | [10] | RW | OE Control. This bit is only active if the output enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect. |
| | [9:0] | RW | DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW) |
| 0x02 | [15:4] | R | NOT USED |
| | [3:0] | RW | DIGITAL PULL RANGE CONTROL |

## Register Descriptions

### Register Address: 0x00. Digital Frequency Control Least Significant Word (LSW)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)[15:0] | | | | | | | | | | | | | | | |

| Bits | Name | Access | Description |
|---|---|---|---|
| 15:0 | DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD | RW | Bits [15:0] are the lower 16 bits of the 26 bit FrequencyControlWord and are the Least Significant Word (LSW). The upper 10 bits are in regsiter 0x01[9:0] and are the Most Significant Word (MSW). The lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word.<br><br>This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section. |

### Register Address: 0x01. OE Control, Digital Frequency Control Most Significant Word (MSW)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Access | R | R | R | R | R | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | NOT USED | | | | | OE | DCXO FREQUENCY CONTROL[9:0] MSW | | | | | | | | | |

| Bits | Name | Access | Description |
|---|---|---|---|
| 15:11 | NOT USED | R | Bits [15:10] are read only and return all 0's when read. Writing to these bits has no effect. |
| 10 | OE Control | RW | Output Enable Software Control. Allows the user to enable and disable the output driver via $I^2C$.<br>0 = Output Disabled (Default)<br>1 = Output Enabled<br>This bit is only active if the Output Enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect. |
| 9:0 | DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW) | RW | Bits [9:0] are the upper 10 bits of the 26 bit FrequencyControlWord and are the Most Significant Word (MSW). The lower 16 bits are in register 0x00[15:0] and are the Least Significant Word (LSW). These lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word.<br>This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section. |

### Register Address: 0x02. DIGITAL PULL RANGE CONTROL [14]

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 6 | 5 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Access | R | R | R | R | R | R | R | R | R | R | R | R | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X |
| Name | NONE | | | | | | | | | | | | DIGITAL PULL RANGE CONTROL | | | |

**Notes:**
14. Default values are factory set but can be over-written after power-up.

| Bits | Name | Access | Description |
|---|---|---|---|
| 15:4 | NONE | R | Bits [15:4] are read only and return all 0's when read. Writing to these bits has no effect. |
| 3:0 | DIGITAL PULL RANGE CONTROL | RW | Sets the digital pull range of the DCXO. The table below shows the available pull range values and associated bit settings. The default value is factory programmed.<br><br>**Bit**<br>**3 2 1 0**<br>0 0 0 0: ±6.25ppm<br>0 0 0 1: ±10ppm<br>0 0 1 0: ±12.5ppm<br>0 0 1 1: ±25ppm<br>0 1 0 0: ±50ppm<br>0 1 0 1: ±80ppm<br>0 1 1 0: ±100ppm<br>0 1 1 1: ±125ppm<br>1 0 0 0: ±150ppm<br>1 0 0 1: ±200ppm<br>1 0 1 0: ±400ppm<br>1 0 1 1: ±600ppm<br>1 1 0 0: ±800ppm<br>1 1 0 1: ±1200ppm<br>1 1 1 0: ±1600ppm<br>1 1 1 1: ±3200ppm |

### Serial Interface Configuration Description

The SiT5186 includes an I²C interface to access registers that control the DCTCXO frequency pull range, and frequency pull value. The SiT5186 I²C slave-only interface supports clock speeds up to 1 MHz. The SiT5186 I²C module is based on the I²C specification, UM1024 (Rev.6 April 4, 2014 of NXP Semiconductor).

### Serial Signal Format

The SDA line must be stable during the high period of the SCL. SDA transitions are allowed only during SCL low level for data communication. Only one transition is allowed during the low SCL state to communicate one bit of data. Figure 43 shows the detailed timing diagram.

An idle I²C bus state occurs when both SCL and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCL is high. A STOP condition is defined by a low to high transition on the SDA while SCL is high. START and STOP conditions are always generated by the master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (the blue-color line shows repeated START in Figure 44).

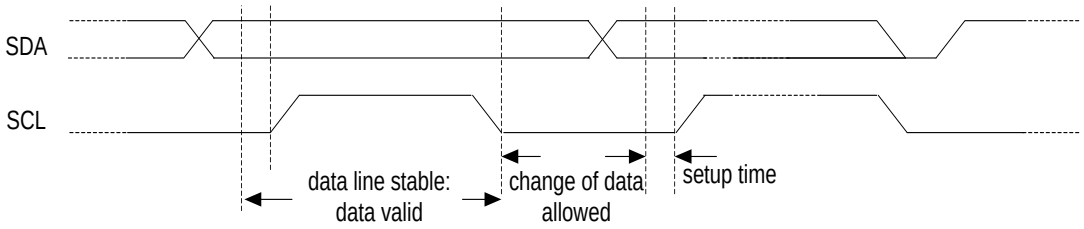



**Figure 43. Data and clock timing relation in I²C bus**

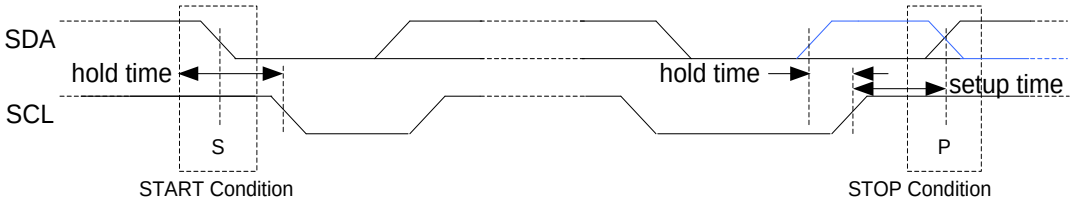



**Figure 44. START and STOP (or repeated START, blue line) condition**

### Parallel Signal Format

Every data byte is 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the MSB (Most Significant Bit) first. The detailed data transfer format is shown in Figure 46 below.

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from the SiT5186 is when the transmitted address does not match the slave address. When the master is reading data from the SiT5186, the SiT5186 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START. If there is a NACK signal at the end of the data, then the SiT5186 tries to send the next data. If the first bit of the next data is “0”, then the SiT5186 holds the SDA line to “0”, thereby blocking the master from generating a STOP/(re)START signal.

### Parallel Data Format

This $I^2C$ slave module supports 7-bit device addressing format. The $8^{th}$ bit is a read/write bit and “0” indicates a read transaction and a “1” indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (00h to FFh). Auto address incrementing is supported which allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. Since the maximum register address value is 255, the address will roll from 255 back to 0 when auto address incrementing is used. Obviously, auto address incrementing should only be used for writing to contiguous addresses. The data format is 16-bit (two bytes) with the most significant byte being transferred first.

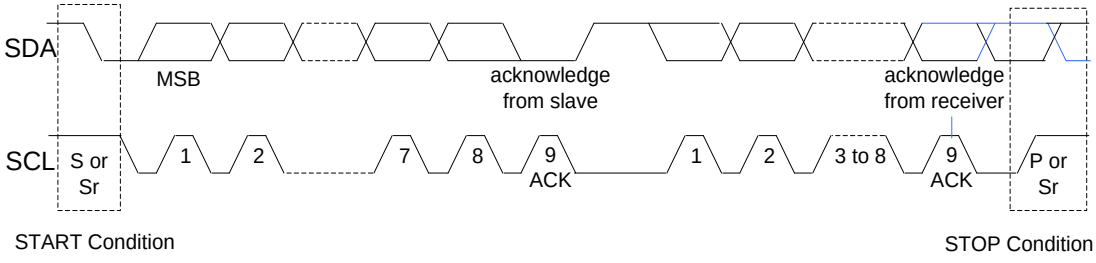



**Figure 45. Parallel signaling format**

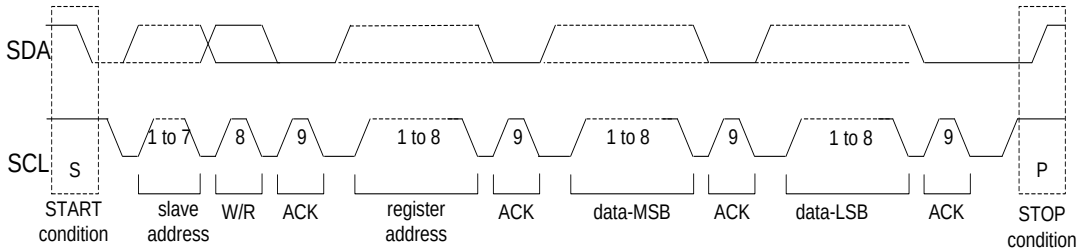



**Figure 46. Parallel data byte format**

Figure 47 below shows the I²C sequence for writing the 4-byte control word using auto address incrementing.

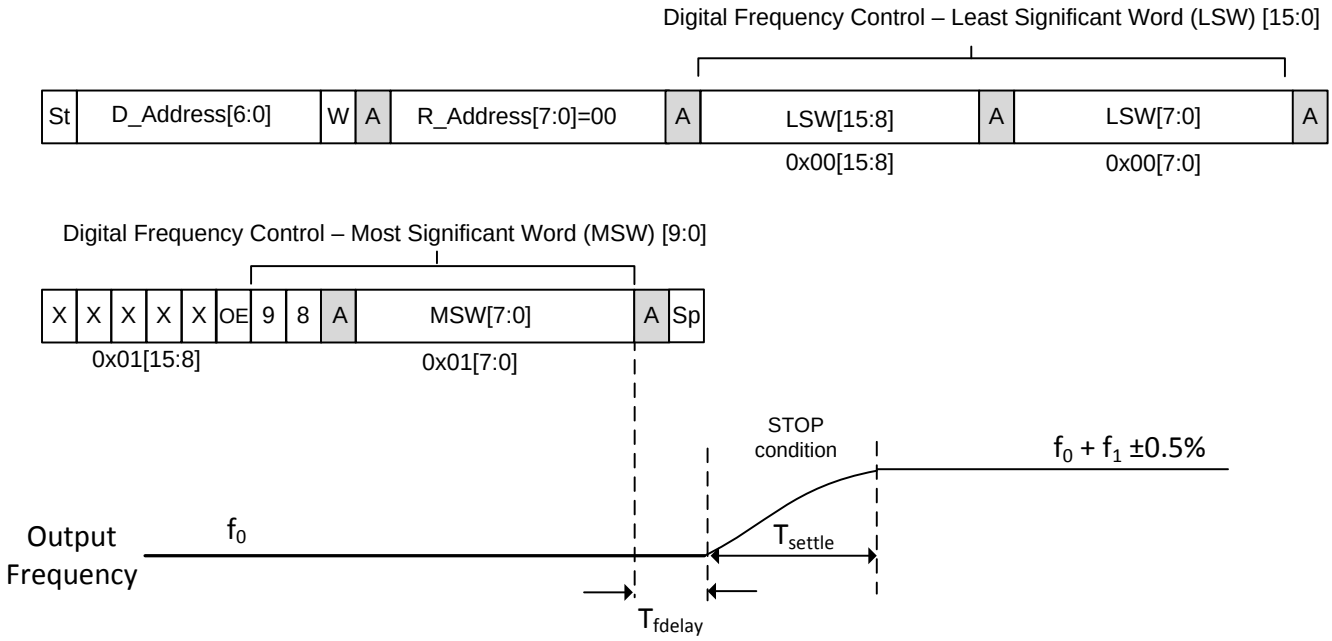



**Figure 47. Writing the Frequency Control Word**

**Table 21. DCTCXO Delay and Settling Time**

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| Frequency Change Delay | $T_{fdelay}$ | – | 22 | – | µsec | |
| Frequency Settling Time | $T_{settle}$ | – | 30 | – | µsec | Time to settle to 1% of final frequency value. |

## I²C Timing Specification

The below timing diagram and table illustrate the timing relationships for both master and slave.

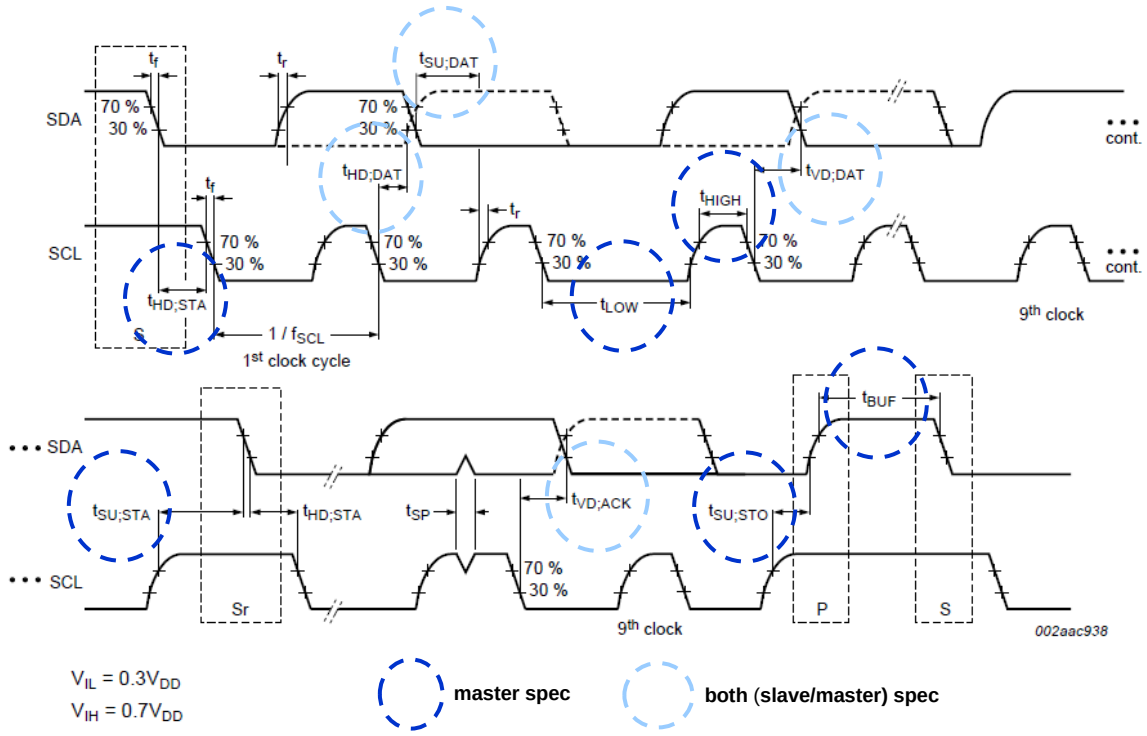



**Figure 48. I²C Timing Diagram**

**Table 22. I²C Timing Requirements**

| Parameter | Speed Mode | Value | Unit |
|---|---|---|---|
| $t_{SETUP}$ | FM+ (1 MHz) | > 50 | nsec |
| | FM (400KHz) | > 100 | nsec |
| | SM (100KHz) | > 250 | nsec |
| $t_{HOLD}$ | FM+ (1 MHz) | > 0 | nsec |
| | FM (400KHz) | > 0 | nsec |
| | SM (100KHz) | > 0 | nsec |
| $t_{VD:AWK}$ | FM+ | > 450 | nsec |
| | FM (400KHz) | > 900 | nsec |
| | SM (100KHz) | > 3450 | nsec |
| $t_{VD:DAT}$ | | NA (s-awk + s-data)/(m-awk/s-data) | |

## I²C Device Address Modes

There are two I²C address modes:

1) Factory Programmed Mode. The lower 4 bits of the 7-bit device address are set by ordering code as shown in Table 23 below. There are 16 factory programmed addresses available. In this mode, pin 5 is NC and the A0 I²C address pin control function is not available.

2) A0 Pin Control. This mode allows the user to select between two I²C Device addresses as shown in Table 24.

**Table 23. Factory Programmed I²C Address Control[15]**

| I²C Address Ordering Code | Device I²C Address |
|---|---|
| 0 | 1100000 |
| 1 | 1100001 |
| 2 | 1100010 |
| 3 | 1100011 |
| 4 | 1100100 |
| 5 | 1100101 |
| 6 | 1100110 |
| 7 | 1100111 |
| 8 | 1101000 |
| 9 | 1101001 |
| A | 1101010 |
| B | 1101011 |
| C | 1101100 |
| D | 1101101 |
| E | 1101110 |
| F | 1101111 |

**Notes:**
15. Table 23 is only valid for the DCTCXO device option which supports I²C Control.

**Table 24. Pin Selectable I²C Address Control[16]**

| A0 Pin 5 | I²C Address |
|---|---|
| 0 | 1100010 |
| 1 | 1101010 |

**Notes:**
16. Table 24 is only valid for the DCTCXO device option which supports I²C control and A0 Device Address Control Pin.

## Schematic Example

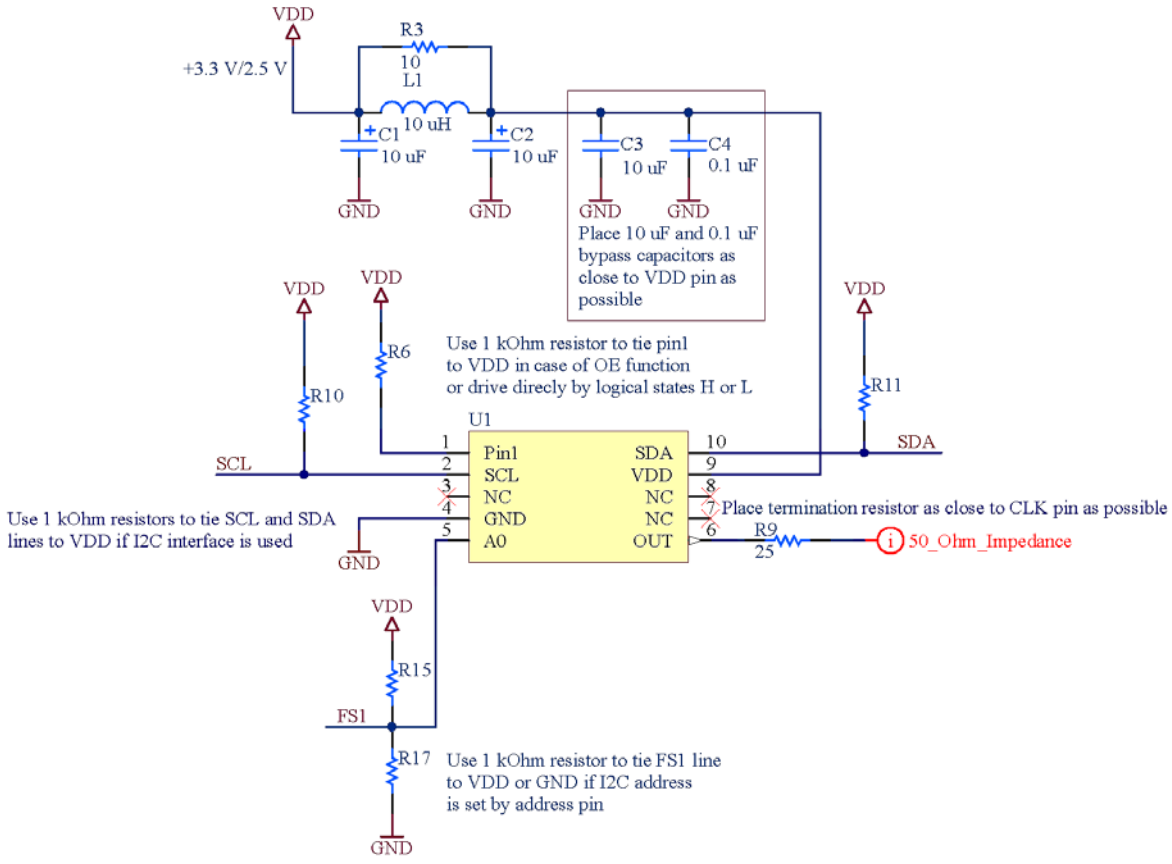
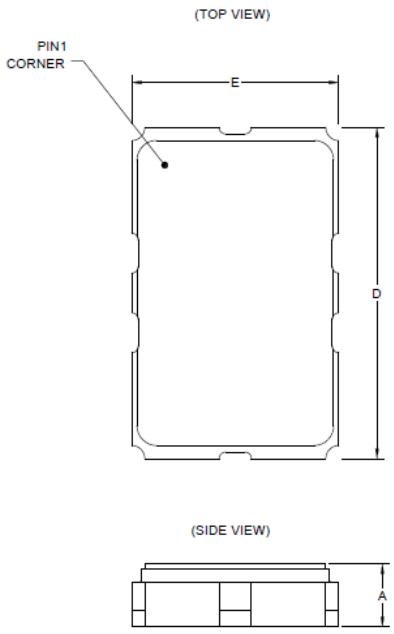



**Figure 49. DCTCXO schematic example.**

## Dimensions and Patterns

**Package Size – Dimensions (Unit: mm)**



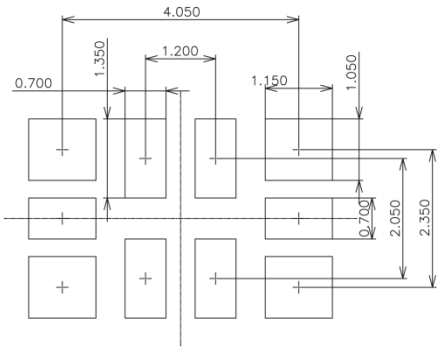

| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.840 | 0.950 | 1.060 |
| BODY SIZE | X | D | 4.850 | 5.000 | 5.150 |
| | Y | E | 3.050 | 3.200 | 3.350 |
| LEAD PITCH | | e | 1.070 | 1.200 | 1.330 |
| | | e1 | 1.220 | 1.350 | 1.480 |
| | | e2 | 0.970 | 1.100 | 1.230 |
| LEAD LENGTH | | L | 0.970 | 1.100 | 1.230 |
| | | L1 | 0.770 | 0.900 | 1.030 |
| LEAD WIDTH | | W | 0.470 | 0.600 | 0.730 |
| | | W1 | 0.670 | 0.800 | 0.930 |
| | | W2 | 0.470 | 0.600 | 0.730 |

NOTES

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.

| TITLE | | DWG. NO. | |
|---|---|---|---|
| 10L CQFN | | POD-CQFN-010-E05032-036 | |
| 3.200x5.000x0.950mm | | REV. | SHEET |
| DATE | 11-OCT-2018 | A02 | 1 OF 1 |

**Recommended Land Pattern (Unit: mm)**




| Solder Print Layout | |
|---|---|
| 10L Ceramic | |
| 5.0x3.2x0.95 | |
| 2017/06/20 | |

## Layout Guidelines

- The SiT5186 uses internal regulators to minimize the impact of power supply noise. For further reduction of noise, it is essential to use two bypass capacitors (0.1 µF and 10 µF). Place the bypass capacitors as close to Vdd pin as possible, typically within 1 to 2 mm. Ensure that the 0.1µF cap is closer to the device Vdd and GND power pins.
- It is also recommended to connect all NC pins to the ground plane and place multiple vias under the GND pin for maximum heat dissipation.
- For additional layout recommendations, refer to the Best Design Layout Practices.

## Manufacturing Guidelines

The SiT5186 Super-TCXOs are precision timing devices. **Proper PCB solder and cleaning processes** must be followed to ensure best performance and long-term reliability.

- **No Ultrasonic or Megasonic Cleaning:** Do not subject the SiT5186 to an ultrasonic or megasonic cleaning environment. Otherwise, permanent damage or long-term reliability issues to the device may result.
- **No external cover.** Unlike legacy quartz TCXOs, the SiT5186 is engineered to operate reliably, without performance degradation, in the presence of ambient disturbers such as airflow and sudden temperature changes. Therefore, the use of an external cover typically required by quartz TCXOs is not needed.
- **Reflow profile:** For mounting these devices to the PCB, IPC/JEDEC J-STD-020 compliant reflow profile must be used. Device performance is not guaranteed if soldered manually or with a non-compliant reflow profile.
- **PCB cleaning:** after the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevated leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, thorough cleaning and drying of the PCB is required as shortly after the reflow process as possible, even when using a “no clean” flux. Care should be taken to remove all residual flux between the SiTime device and the PCB. Note that ultrasonic PCB cleaning should not be used with SiTime oscillators.
- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

### Table 25. Additional Information

| Document | Description | Download Link |
|---|---|---|
| **Evaluation Boards** | SiT6722EB Evaluation Board User Manual | https://www.sitime.com/support/user-guides |
| **Interposer Boards** | SiT6911EB Interposer Boards User Manual | https://www.sitime.com/support/user-guides |
| **Time Master Web-based Configurator** | Web tool to establish proper programming | https://www.sitime.com/time-master-web-based-configurator |
| **Manufacturing Notes** | Tape & Reel dimension, reflow profile and other manufacturing related info | http://www.sitime.com/manufacturing-notes |
| **Performance Reports** | Additional performance data such as phase noise, current consumption and jitter for selected frequencies | http://www.sitime.com/support/performance-measurement-report |
| **Termination Techniques** | Termination design recommendations | http://www.sitime.com/support/application-notes |
| **Layout Techniques** | Layout recommendations | http://www.sitime.com/support/application-notes |

### Table 26. Revision History

| Version | Release Date | Change Summary |
|---|---|---|
| 0.3 | 11/15/2018 | First release, advanced information |

**SiTime Corporation**, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439