

HM511001A Series

1,048,576-Word x 1-Bit CMOS Dynamic RAM

DESCRIPTION

The Hitachi HM511001A series is a CMOS dynamic RAM organized 1,048,576-word x 1-bit. HM511001A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

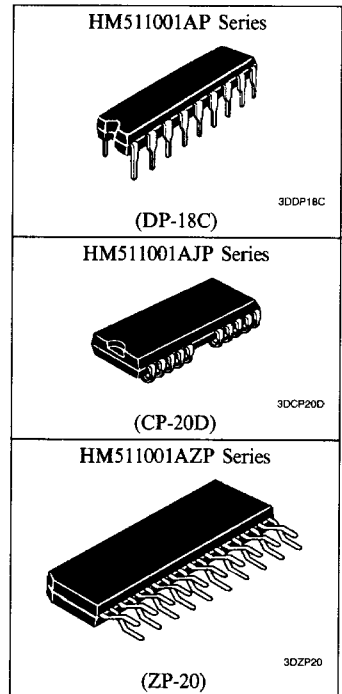
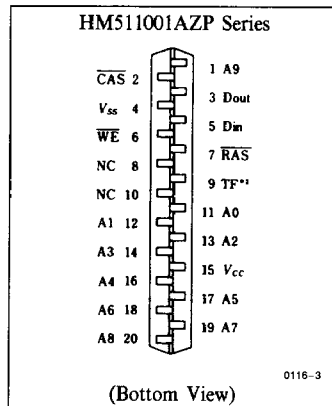
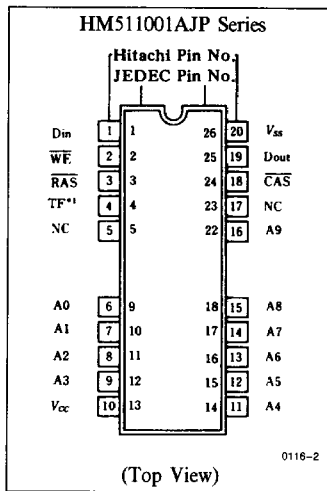
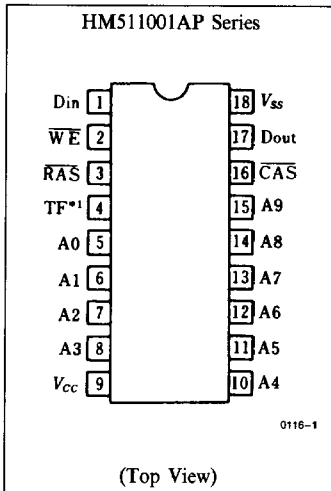
The HM511001A offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM511001A to be packaged in standard, 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

FEATURES

- High Speed
 - Access Time60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power
 - Active495 mW/440 mW/385 mW/330 mW/275 mW
 - Standby11 mW
- Single 5V Supply ($\pm 10\%$)
- Nibble Mode Capability
- 512 Refresh Cycles(8 ms)
- 2 Variations of Refresh
 - RAS Only Refresh
 - CAS Before RAS Refresh

PIN OUT



PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₉	Address Input
A ₀ -A ₈	Refresh Address Input
A ₉	Nibble Address Input
D _{in}	Data Input
D _{out}	Data Output
RAS	Row Address Strobe
CAS	Row Address Input
WE	Read/Write Input
TF*1	Test Function
V _{CC}	Power (+ 5V)
V _{SS}	Ground

Note: *1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

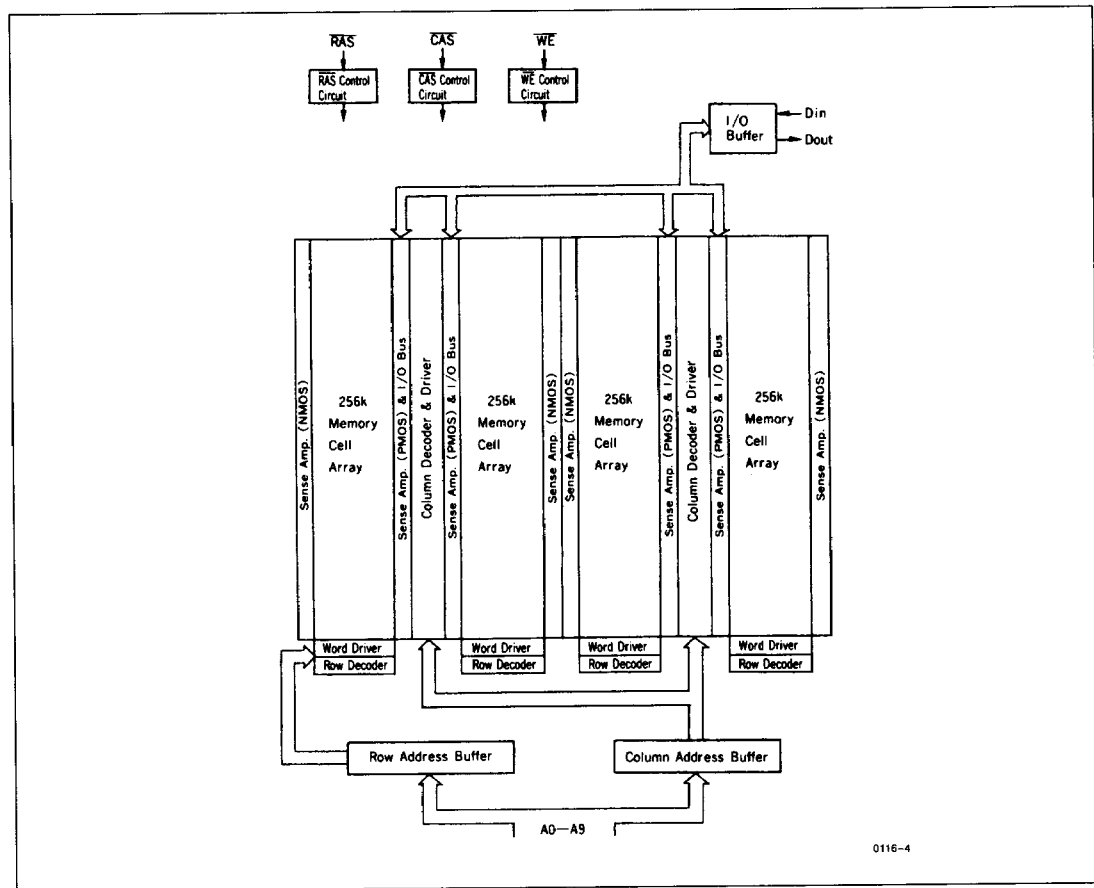


■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511001AP-6	60 ns	300 mil
HM511001AP-7	70 ns	18-pin
HM511001AP-8	80 ns	Plastic DIP
HM511001AP-10	100 ns	(DP-18C)
HM511001AP-12	120 ns	
HM511001AJP-6	60 ns	300 mil
HM511001AJP-7	70 ns	20-pin
HM511001AJP-8	80 ns	Plastic SOJ
HM511001AJP-10	100 ns	(CP-20D)
HM511001AJP-12	120 ns	

Part No.	Access Time	Package
HM511001AZP-6	60 ns	400 mil
HM511001AZP-7	70 ns	20-pin
HM511001AZP-8	80 ns	Plastic DIP
HM511001AZP-10	100 ns	(ZP-20)
HM511001AZP-12	120 ns	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	$^{\circ}C$
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}C$



■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-2.0	—	0.8	V

Note: 1. All voltages referenced to V_{SS} .

• DC Characteristics ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	HM511001A										Unit	Test Condition	Note
		-6		-7		-8		-10		-12				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	—	50	mA	\overline{RAS} , \overline{CAS} Cycling, $t_{RC} = \text{Min}$	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	\overline{RAS} , $\overline{CAS} = V_{IH}$, $\overline{D_{out}} = \text{High-Z}$ TTL Interface	
		—	1	—	1	—	1	—	1	—	1		\overline{RAS} , $\overline{CAS} \geq V_{CC} - 0.2V$, $\overline{D_{out}} = \text{High-Z}$ CMOS Interface	
Refresh Current	I_{CC3}	—	90	—	80	—	70	—	60	—	50	mA	\overline{RAS} Only Refresh, $t_{RC} = \text{Min}$	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, $\overline{D_{out}} = \text{Enable}$	1
Refresh Current	I_{CC6}	—	80	—	70	—	60	—	50	—	40	mA	\overline{CAS} Before \overline{RAS} Refresh, $t_{RC} = \text{Min}$	
Nibble Mode Current	I_{CC8}	—	70	—	70	—	50	—	50	—	40	mA	$\overline{RAS} = V_{IL}$, \overline{CAS} Cycling, $t_{NC} = \text{Min}$	1, 3
Input Leakage	I_{LI}	-10	10	-10	10	-10	10	-10	10	-10	10	μA	$V_{IN} = 0$ to $+7V$	
Output Leakage	I_{LO}	-10	10	-10	10	-10	10	-10	10	-10	10	μA	$V_{in} = 0$ to $+7V$, $\overline{D_{out}} = \text{Disabled}$	
Output Levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	$I_{out} = -5\text{ mA}$	
	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	$I_{out} = 4.2\text{ mA}$	

- Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed less than three times while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

• Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ\text{C}$)

Parameter	Symbol	Typ	Max	Unit	Note	
Input Capacitance	Address, Data Input	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7	pF	1
Output Capacitance	Data Output	C_O	—	7	pF	1, 2

- Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{CAS} = V_{IH}$ to disable $\overline{D_{out}}$.



• AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)^{1, 10}

Test Conditions

Input Rise and Fall Times 5 ns Output Load 2 TTL Gate + C_L (100 pF)
 Input Timing Reference Levels 0.8V, 2.4V (Including Scope and Jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
RAS Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
RAS Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
RAS to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	7
RAS to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	11
RAS Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{\text{CAS}}$ to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	6
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from RAS	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 4
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Delay	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	5



Write Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t _{WCS}	0	—	0	—	0	—	0	—	0	—	ns	8
Write Command Hold Time	t _{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t _{WCP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to RAS Lead Time	t _{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to CAS Lead Time	t _{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in Setup Time	t _{DS}	0	—	0	—	0	—	0	—	0	—	ns	9
Data-in Hold Time	t _{DH}	15	—	15	—	20	—	20	—	25	—	ns	9

Read-Modify-Write Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t _{RWC}	145	—	155	—	190	—	210	—	245	—	ns	
RAS to WE Delay Time	t _{RWD}	60	—	70	—	80	—	90	—	110	—	ns	8
CAS to WE Delay Time	t _{CWD}	20	—	20	—	25	—	25	—	30	—	ns	8
Column Address to WE Delay Time	t _{AWD}	30	—	35	—	40	—	45	—	55	—	ns	8

Refresh Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CAS Setup Time (CAS Before RAS Refresh)	t _{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CAS Before RAS Refresh)	t _{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
RAS Precharge to CAS Hold Time	t _{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Nibble Mode Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Nibble Mode Access Time	t _{NAC}	—	20	—	20	—	25	—	25	—	30	ns	
Nibble Mode Cycle Time	t _{NC}	40	—	40	—	45	—	45	—	50	—	ns	
Nibble Mode CAS Precharge Time	t _{NCP}	10	—	10	—	10	—	10	—	10	—	ns	
Nibble Mode CAS Pulse Width	t _{NCA}	20	—	20	—	25	—	25	—	30	—	ns	
Nibble Mode RAS Hold Time	t _{NRSH}	20	—	20	—	25	—	25	—	30	—	ns	

Nibble Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	65	—	65	—	65	—	65	—	75	—	ns	
Nibble Mode Write Command CAS Lead Time	t_{NCWL}	20	—	20	—	20	—	20	—	25	—	ns	
Nibble Mode \overline{CAS} to \overline{WE} Delay Time	t_{NCWD}	20	—	20	—	20	—	20	—	25	—	ns	

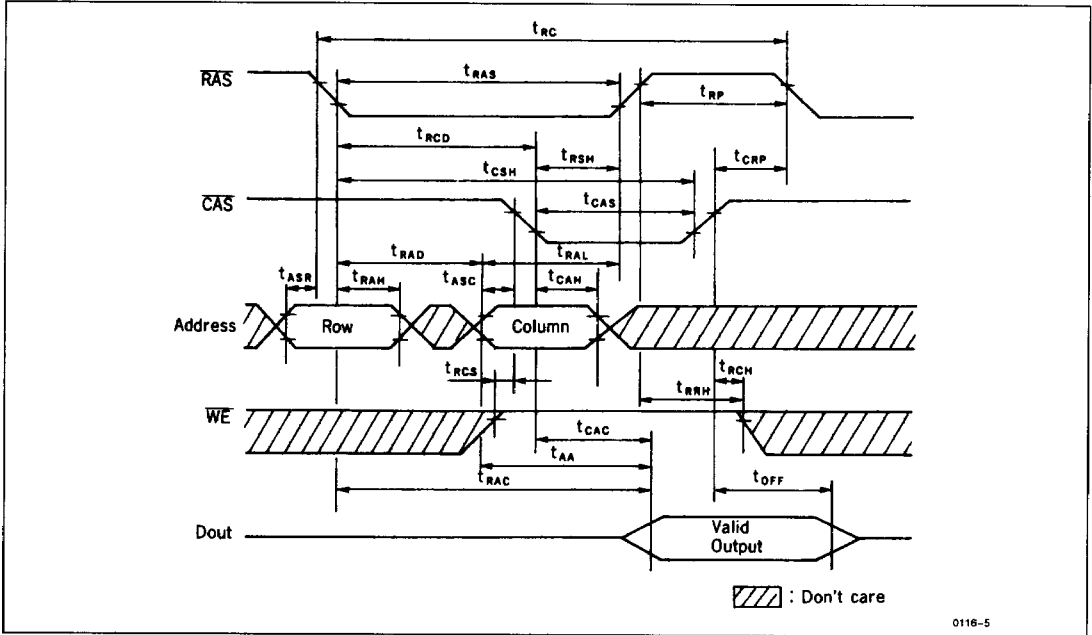
Notes: 1. AC measurements assume $t_T = 5$ ns.

- Assumes that $t_{RCD} \leq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
- Assumes that $t_{RCD} \geq t_{RCD}(\max)$ and $t_{RAD} \leq t_{RAD}(\max)$.
- $t_{OFF}(\max)$ is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Transition times are measured between V_{IH} and V_{IL} .
- Operation with the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RCD}(\max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
- t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\min)$, $t_{CWD} \geq t_{CWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in delayed write or read-modify-write cycles.
- An initial pause of 100 μ s is required after power-up followed by eight initialization cycles (any combination of cycles containing \overline{RAS} clock such as \overline{RAS} only refresh). If internal refresh counter is used, eight or more \overline{CAS} before \overline{RAS} refresh cycles are required.
- If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled exclusively by t_{AA} .

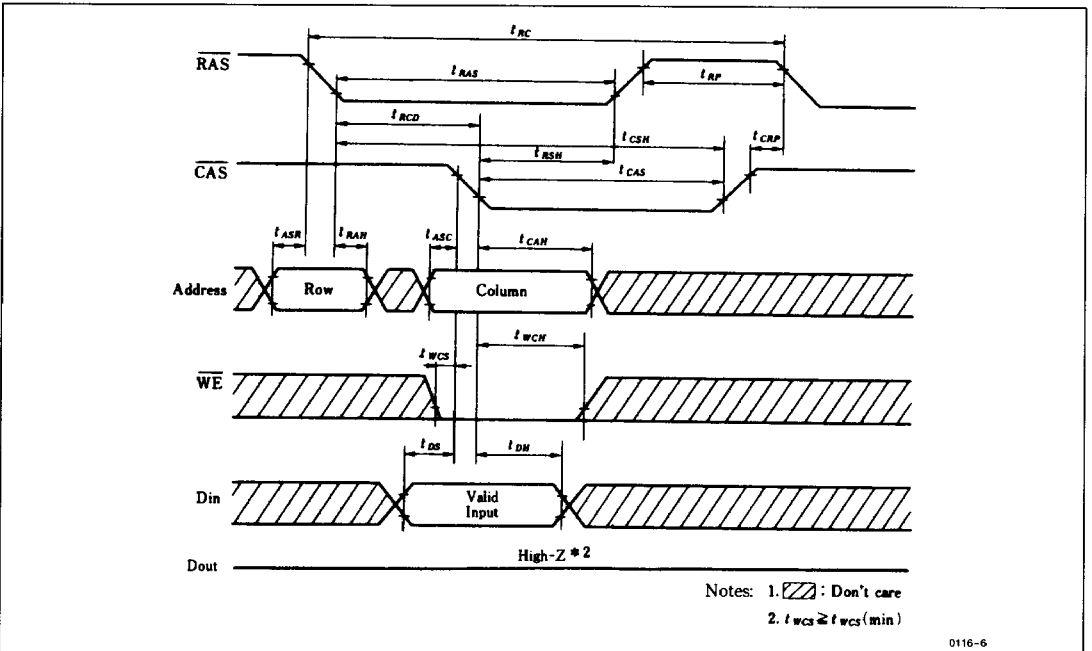


■ TIMING WAVEFORMS

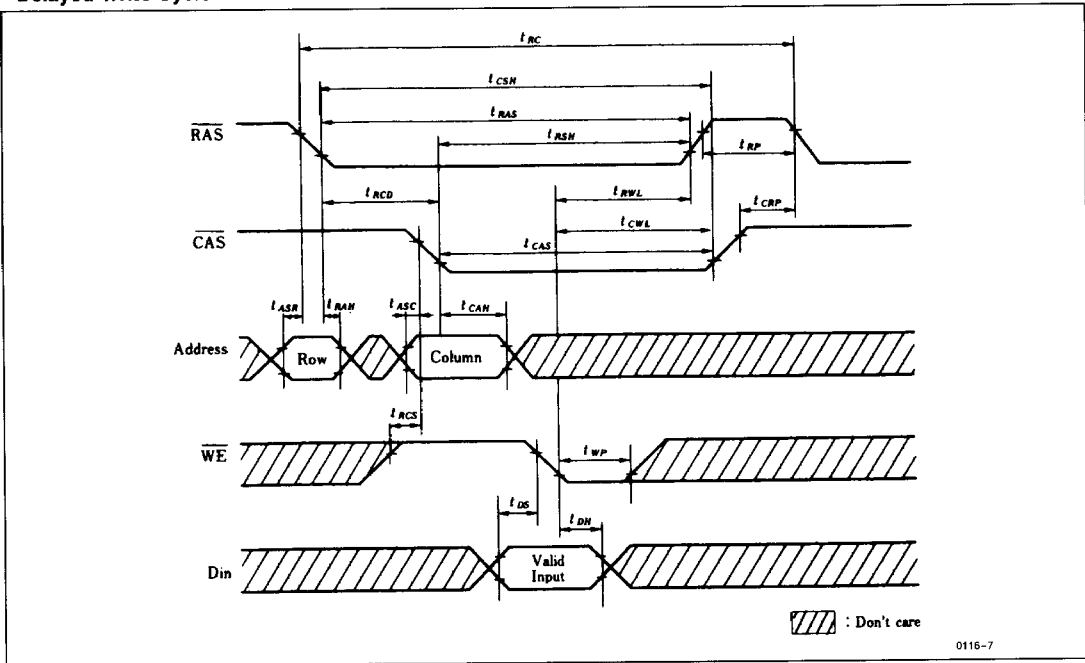
• Read Cycle



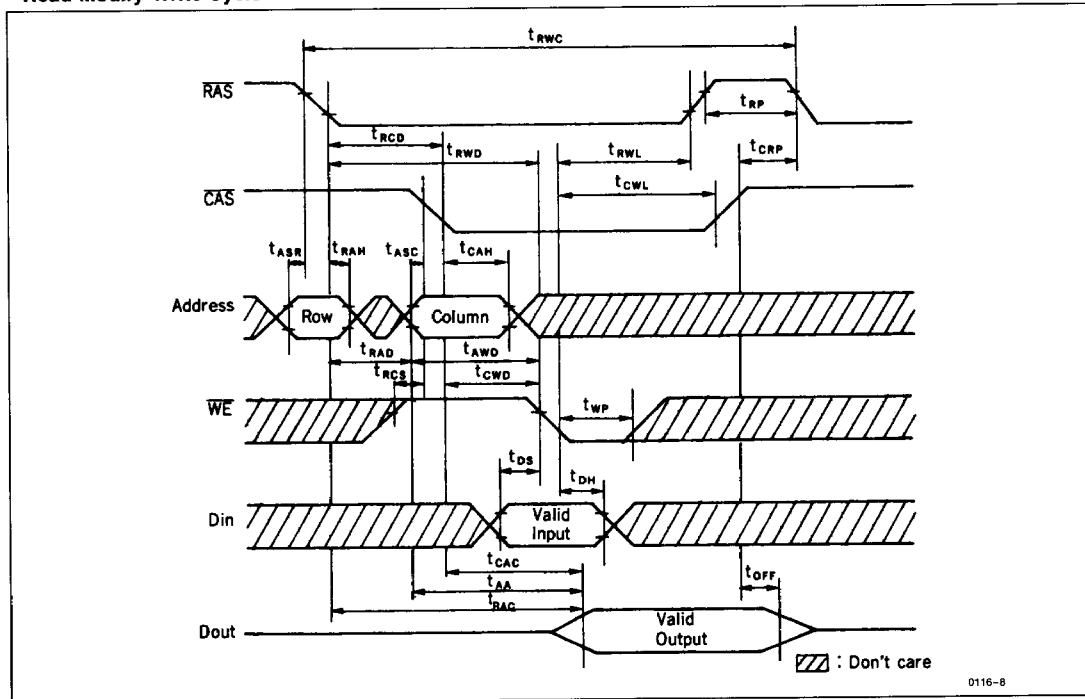
• Early Write Cycle



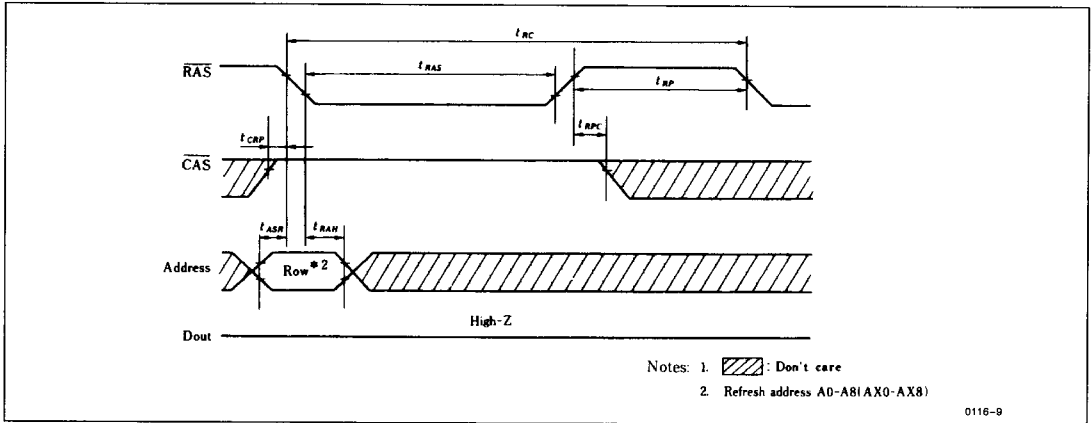
• Delayed Write Cycle



• Read-Modify-Write Cycle

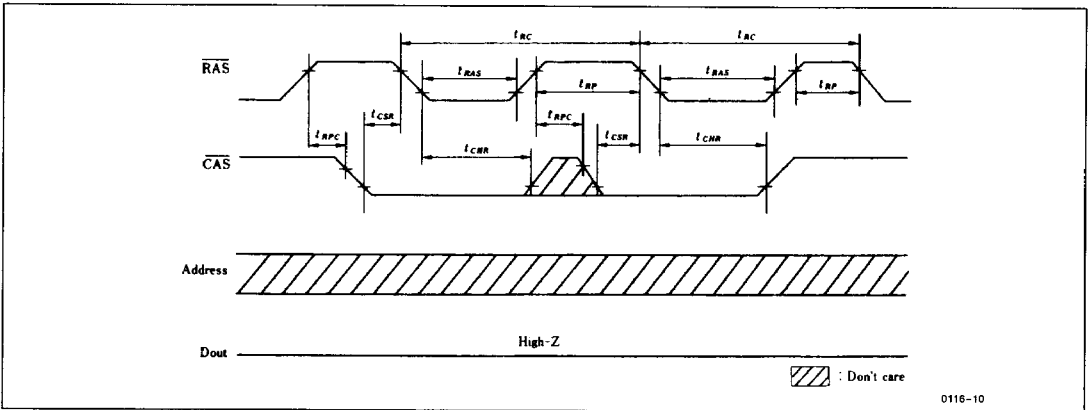


• **RAS Only Refresh Cycle**



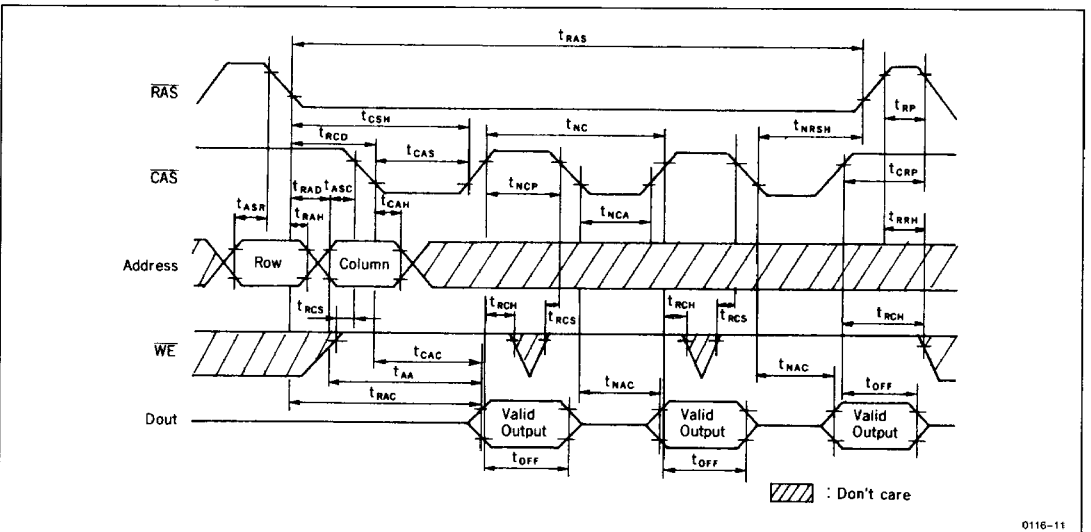
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• **CAS Before RAS Refresh Cycle**



0116-10

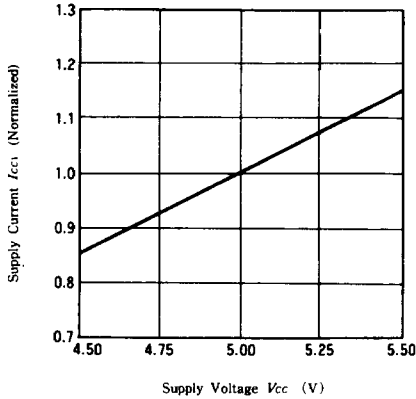
• **Nibble Mode Read Cycle**



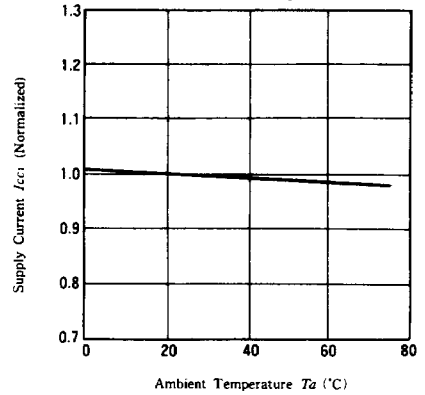
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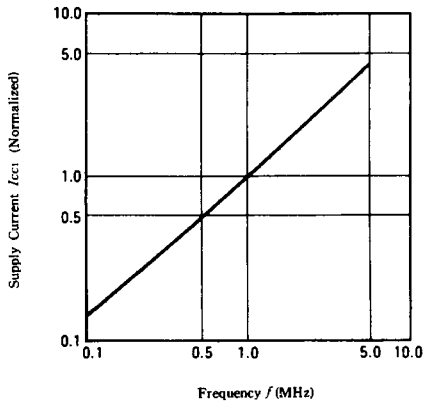
Supply Current (Active) vs. Supply Voltage



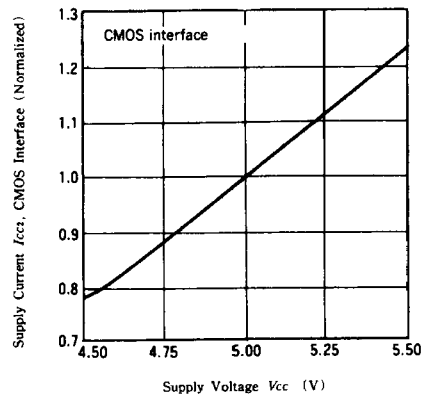
Supply Current (Active) vs. Ambient Temperature



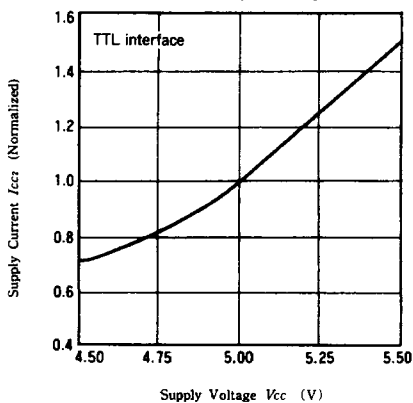
Supply Current (Active) vs. Frequency



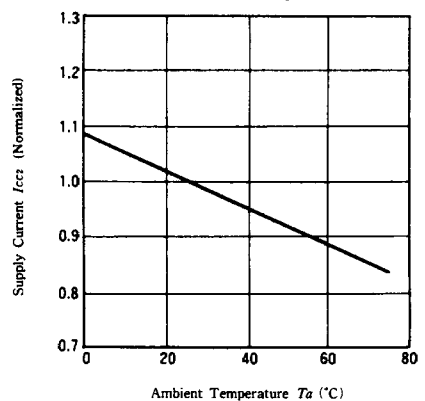
Supply Current (Standby) vs. Supply Voltage



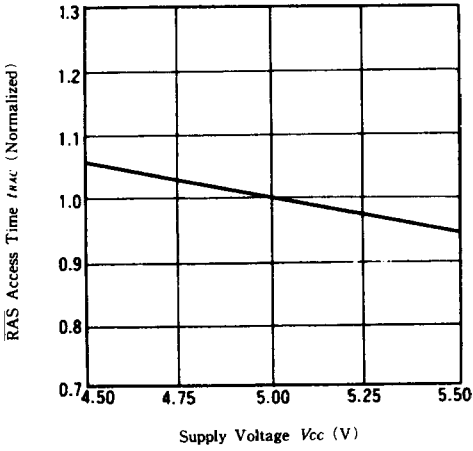
Supply Current (Standby) vs. Supply Voltage



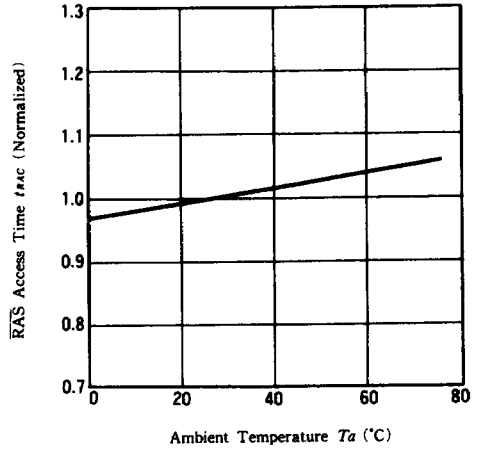
Supply Current (Standby) vs. Ambient Temperature



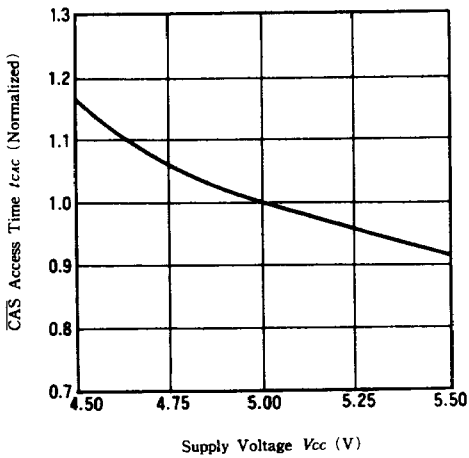
RAS Access Time vs. Supply Voltage



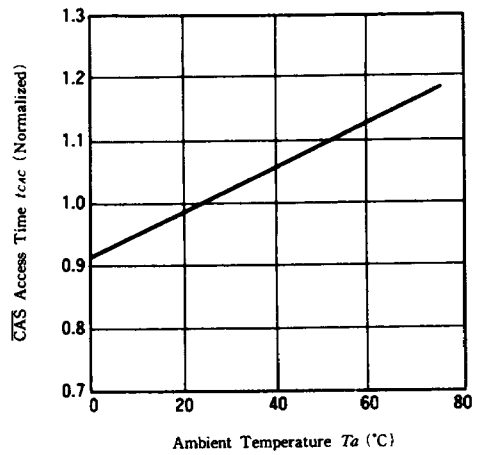
RAS Access Time vs. Ambient Temperature



CAS Access Time vs. Supply Voltage



CAS Access Time vs. Ambient Temperature



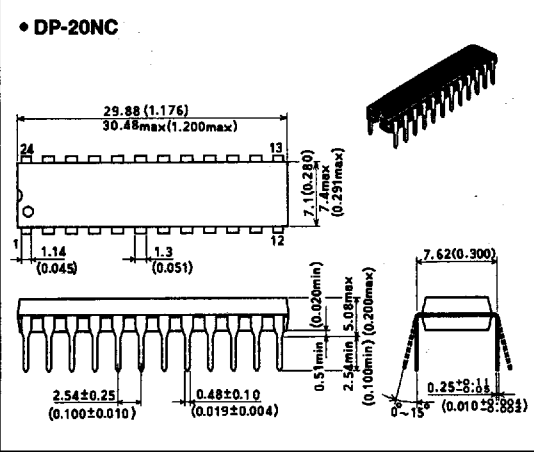
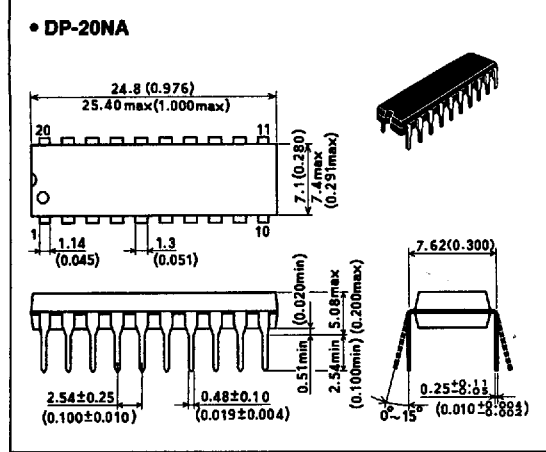
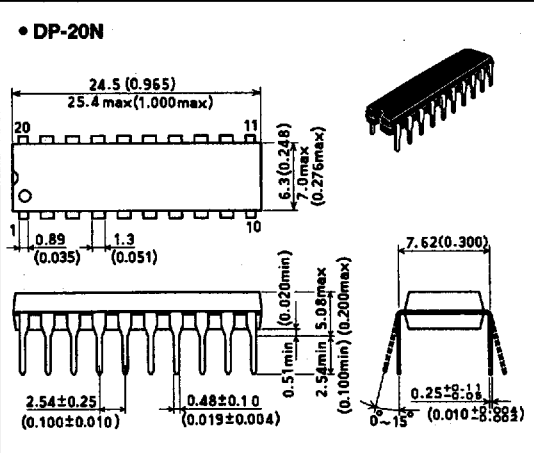
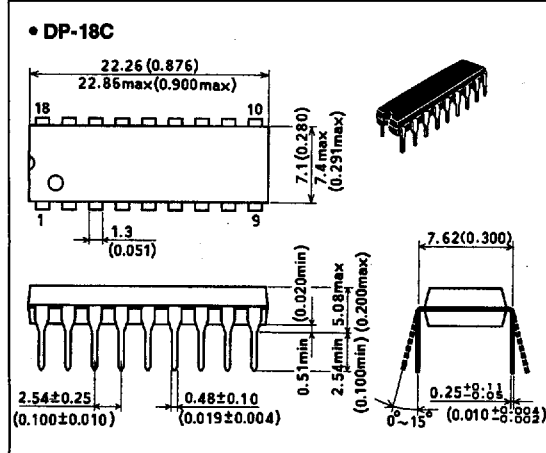
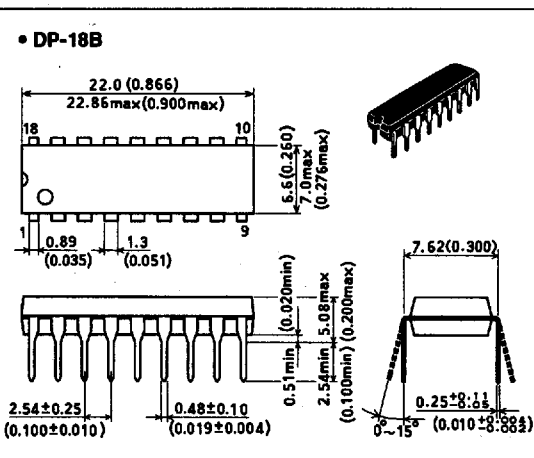
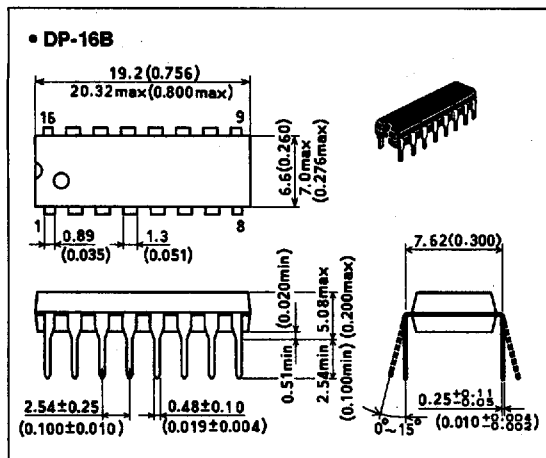
0116-15



T-90-20

Unit: mm (inch) Scale 3/2

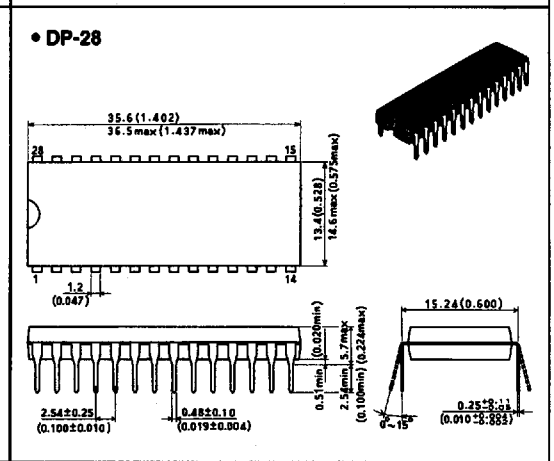
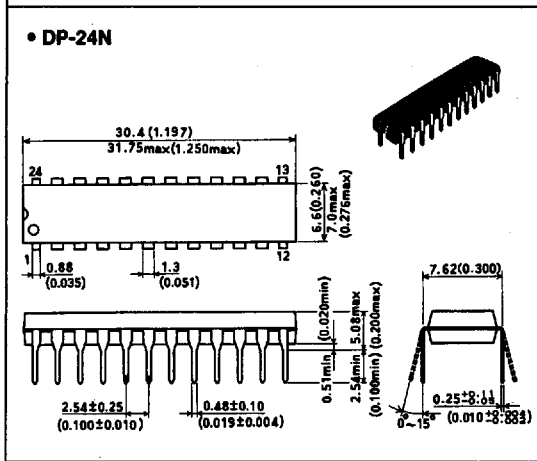
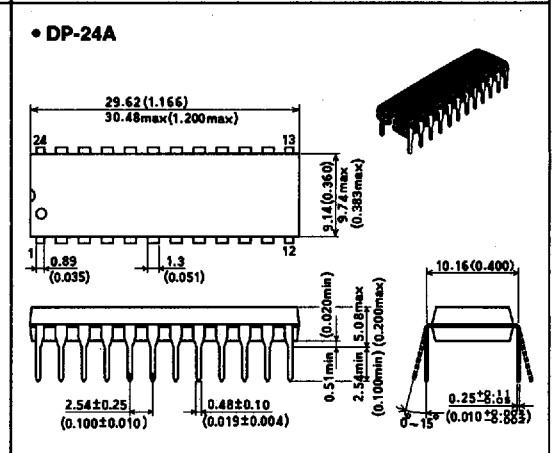
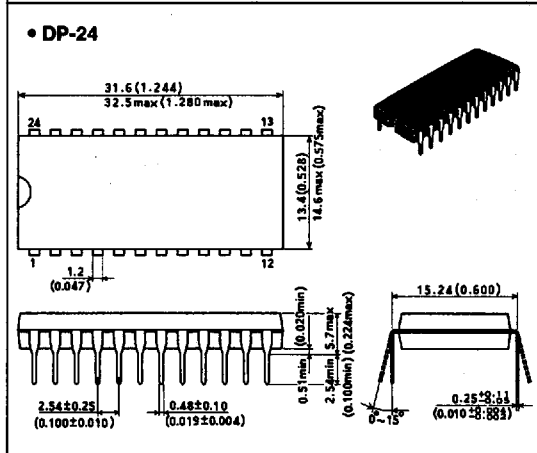
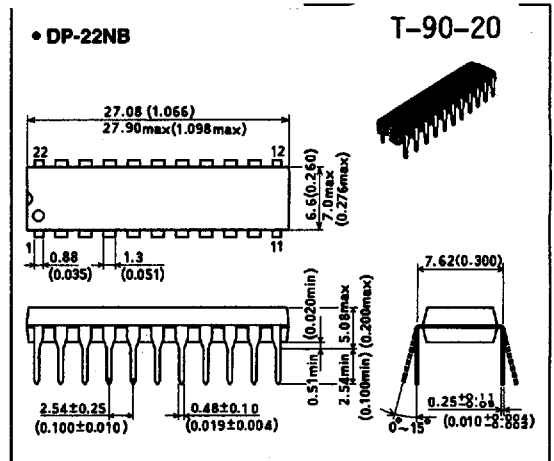
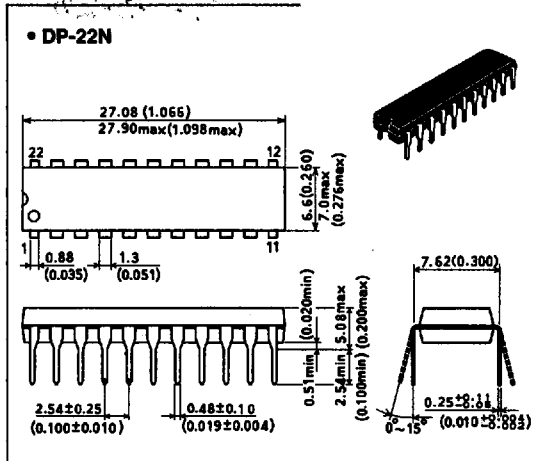
• Dual-in-line Plastic



• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

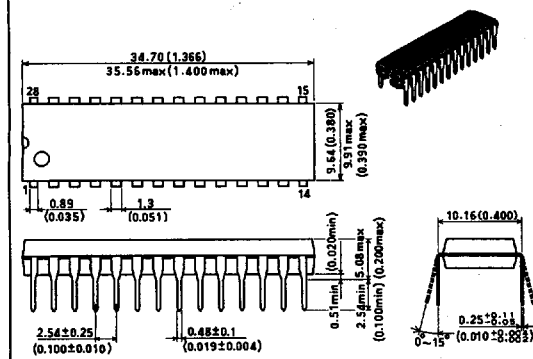


• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

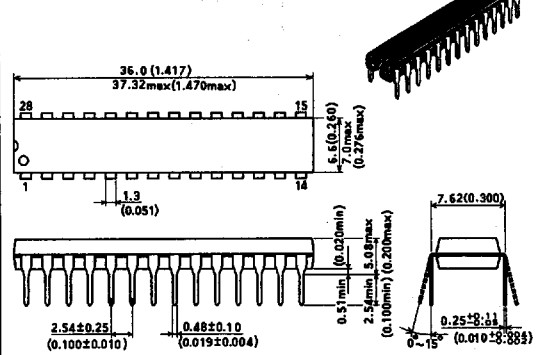
Unit: mm (inch) Scale 3/2

• DP-28C



• DP-28N

T-90-20

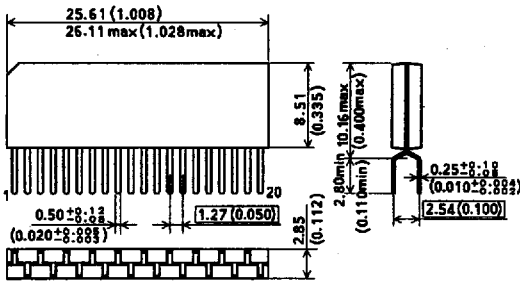
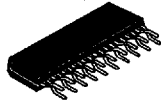


• Zigzag-in-line Plastic

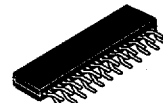
HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

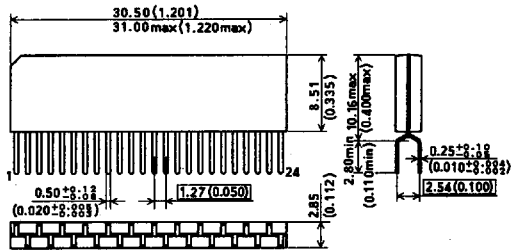
• ZP-20



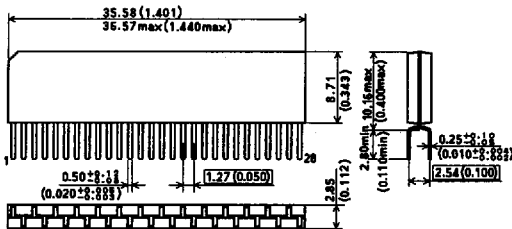
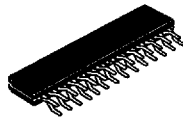
• ZP-24



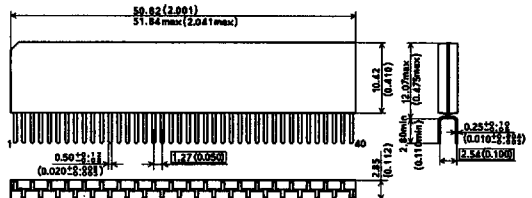
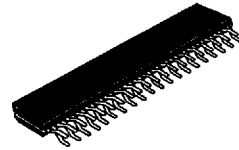
T-90-20



• ZP-28



• ZP-40



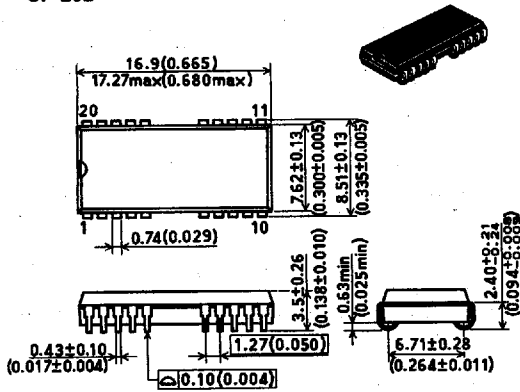
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

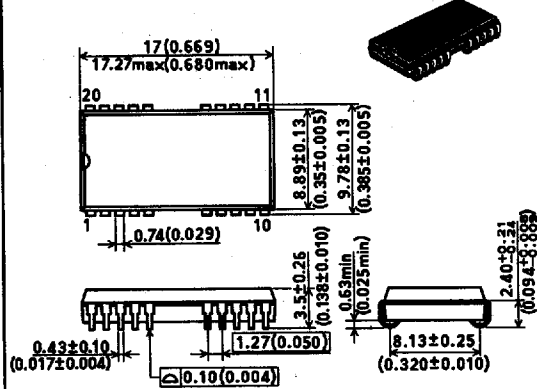
Unit: mm (inch) Scale 3/2

T-90-20

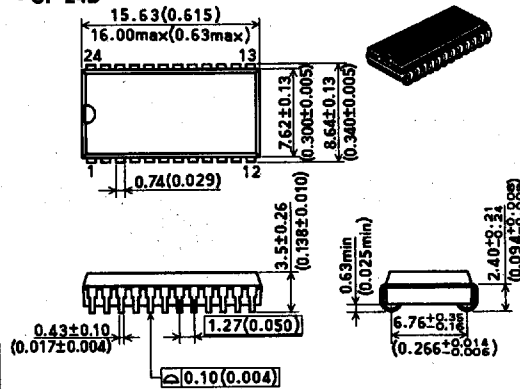
• CP-20D



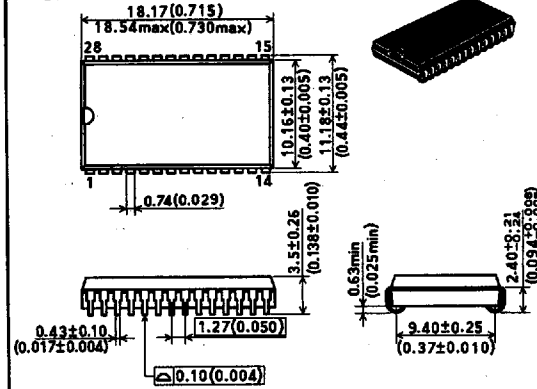
• CP-20DA



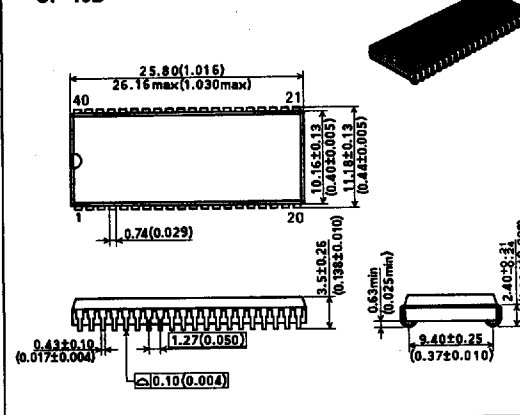
• CP-24D



• CP-28D

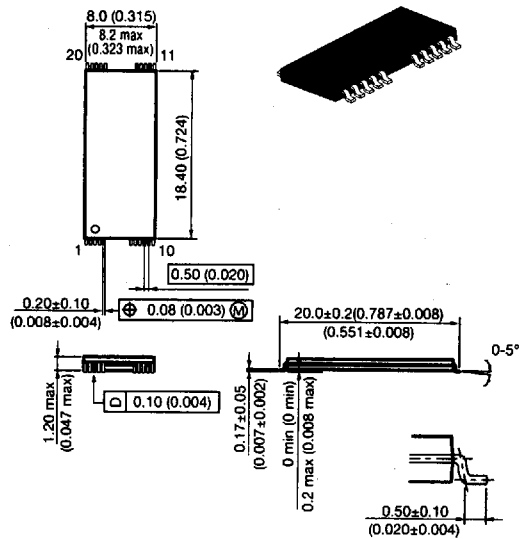


• CP-40D



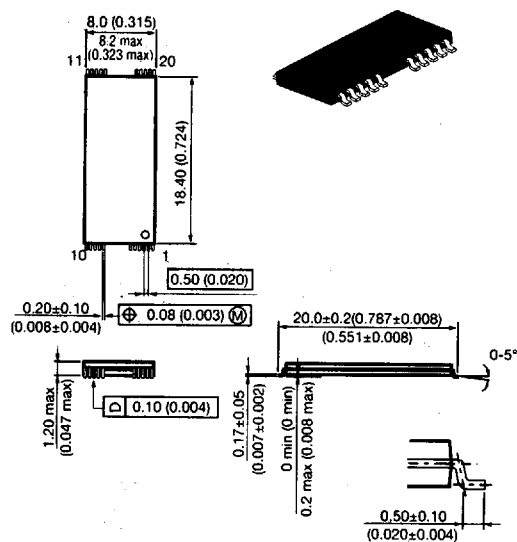
• TSOP (Thin Small Outline Packag^e) HITACHI/ LOGIC/ARRAYS/MEM Unit: mm (inch) Scale 3/2

• TFP-20DA

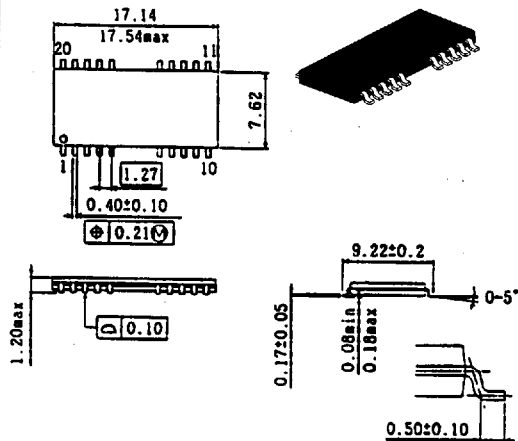


• TFP-20DAR

T-90-20



• TTP-20D



• TTP-20DR

