FAST 74F1761

DRAM And Interrupt Vector Controller

FAST Products

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1761	100MHz	200mA

FEATURES

- **Programmable DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Provides byte selection for 16 and 32 bit buses**
- **Interrupt Priority Encoder included**
- **Interrupt Acknowledge vector generator on-chip**

DESCRIPTION

The Signetics DRAM and Interrupt Vector Controller (DIVC) is a high performance bipolar device designed to reduce board space and improve performance in micro-processor-based systems. The DIVC's functions include a DRAM signal interface with user programmable timing to match the performance of specific DRAMs used in a system. With a maximum clock frequency of 100 MHz, this means a timing resolution of 10 nsec. The DRAM Controller section also includes automatic refresh arbitration, with the duration and frequency of refresh totally programmable by the user. When used with the 74F1762 Memory Address Controller, the DIVC provides a complete system solution for DRAM and Interrupt Control. For Interrupt Control, the DIVC contains an Interrupt Priority Decoder with latched inputs controlled by the Interrupt Latch Enable (ILE) input. In addition, the DIVC contains an Interrupt Acknowledge Controller which passes a program-mable 8-bit vector on the system data bus upon receipt of an interrupt acknowledge. There are 7 interrupt acknowledge vectors, each accessable by placing the priority number of the interrupt acknowledge on the A_1-A_3 signal inputs while acknowledging an interrupt.

ORDERING INFORMATION

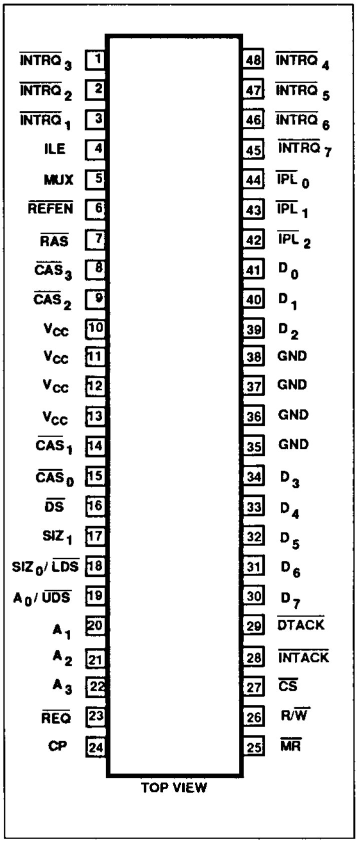
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1761N
44-Pin PLCC	N74F1761A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

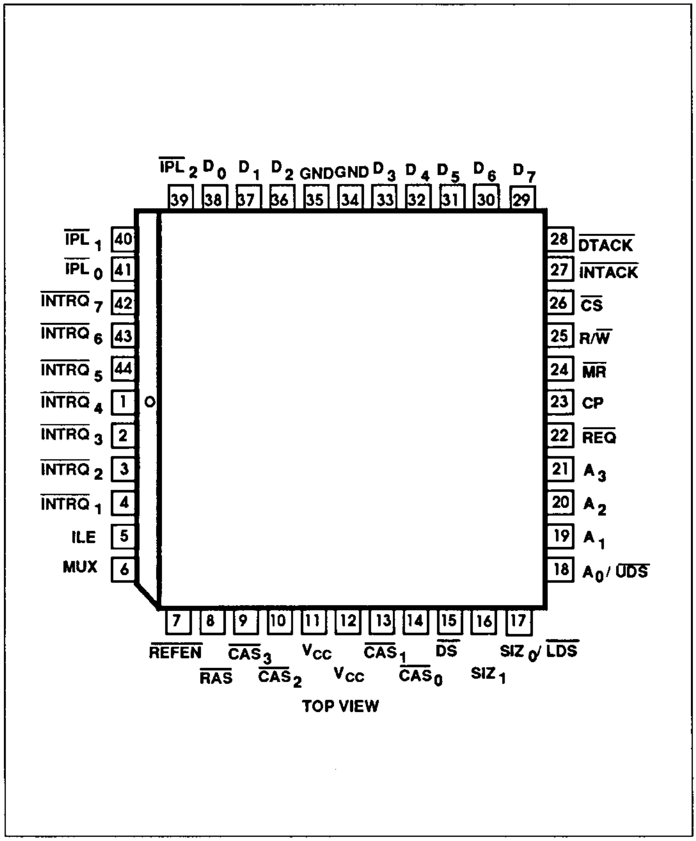
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ}$	DRAM Request input	1.0/1.0	20µA/0.6mA
$SIZ_0/\overline{LDS}$, SIZ_1, $A_0/\overline{UDS}$, A_1	Byte Select inputs	1.0/1.0	20µA/0.6mA
A_2, A_3	Register Select inputs	1.0/1.0	20µA/0.6mA
$\overline{CS}$, $\overline{DS}$	Chip Select, Data Strobe inputs	1.0/1.0	20µA/0.6mA
$R/\overline{W}$	Read/Write input	1.0/1.0	20µA/0.6mA
$\overline{INTACK}$	Interrupt Acknowledge input	1.0/1.0	20µA/0.6mA
ILE	Interrupt Latch Enable intput	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{INTRQ}_{1-7}$	Interrupt Request inputs	1.0/1.0	20µA/0.6mA
$\overline{DTACK}$	Data Transfer Acknowledge output	OC/40	OC/24mA
D_0-D_7	Data Bus outputs	50/40	1.0mA/24mA
IPL_{0-2}	Interrupt Priority outputs	50/40	1.0mA/24mA
$\overline{RAS}$, MUX, $\overline{REFEN}$, $\overline{CAS}_{0-7}$	DRAM Control outputs	N/A	35mA/60mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
FAST Unit Loads do not correspond to DRAM input Loads.
OC=Open Collector

DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



NOTE: Pinout assignments are strictly preliminary and are subject to change

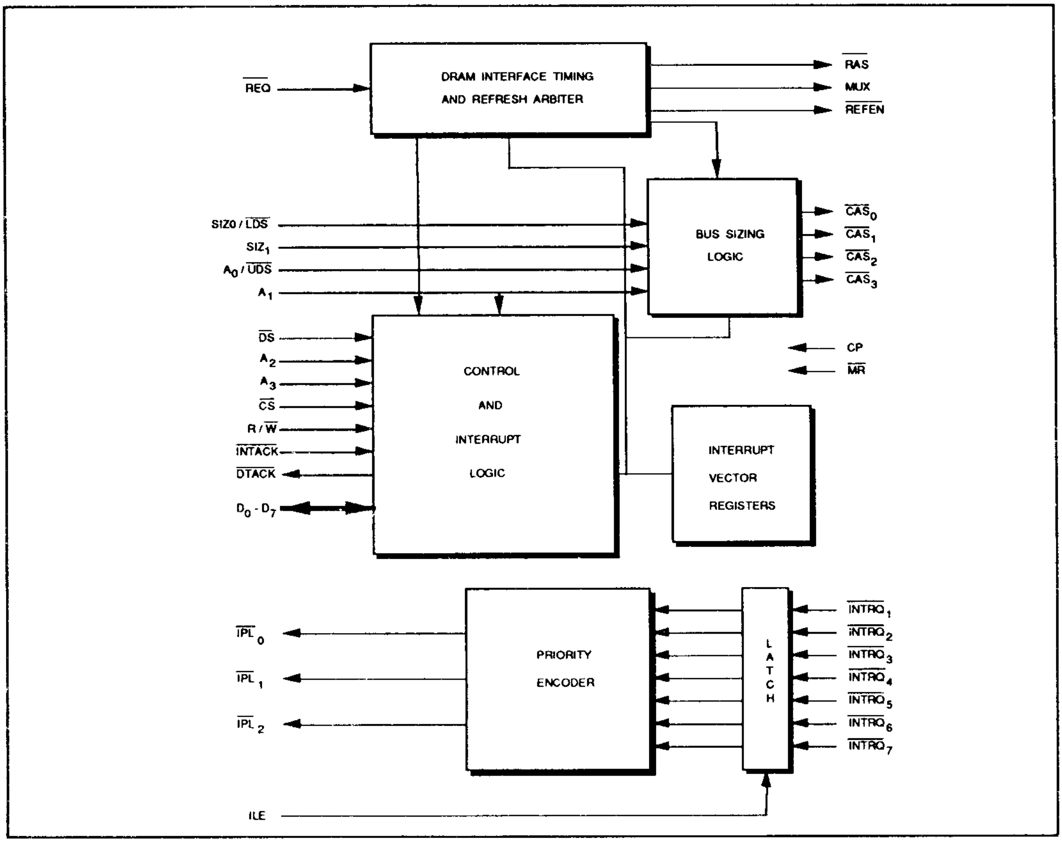
FUNCTIONAL DESCRIPTION

Figure 1 shows the overall architecture of the 74F1761. The DRAM Interface Timing section produces the $\overline{RAS}$, MUX, $\overline{CAS}$, $\overline{DTACK}$ and Refresh Enable ($\overline{REFEN}$) signals in response to the Request ($\overline{REQ}$) input. The timing of these signals is configurable by programming a register set within the F1761 (see **REGISTER DESCRIPTION**). The timing section also includes a refresh arbiter that allows for refreshing the DRAM at a frequency programmable by the user. While a refresh cycle is being executed, the $\overline{REFEN}$ output is asserted, allowing a companion memory address generator (such as the 74F1762 Memory Address Controller) to assert a refresh row address on the DRAM address inputs.

The Bus Sizing Logic section is a configurable decoder that allows for multiple $\overline{CAS}$ outputs depending on the state of the $\overline{DS}$, $SIZ_0/\overline{LDS}$, SIZ_1, $A_0/\overline{UDS}$, and A_1 signal inputs, and the selected bus size scheme (See **Table 4. CAS DECODING SUMMARY**). By programming the Configuration Register, the F1761 can respond to a variety of 8, 16, and 32 Bit Processor signal outputs. In the 8-bit mode, the F1761 will assert one of four $\overline{CAS}$ outputs depending on the state of the A_0 and A_1 inputs during the $\overline{CAS}$ signal assertion time determined by the timing logic. In the 16-bit mode, the F1761 will assert $\overline{CAS}_0$ and/or $\overline{CAS}_1$ depending on the state of the $\overline{UDS}$ and LDS inputs, respectively. In the 32 Bit mode, the A_1, A_0, SIZ_1 and SIZ_0 determine the $\overline{CAS}$ outputs to be asserted according to the 68020 byte-selection scheme.

The Control and Interrupt Logic section determines the response of the F1761 in one of two modes. The internal registers of the device can be accessed by asserting the $\overline{CS}$ and $\overline{DS}$ inputs while placing the address of the register to be accessed on

BLOCK DIAGRAM



the A_1, A_2, and A_3 inputs. The R/$\overline{W}$ input indicates to the F1761 the direction of data transfer when accessing a particular register. In addition, the configuration register contains one bit of register addressing that is initialized to 0. The lower order registers contain the timing information for the DRAM interface, while the upper order registers contain the Interrupt Vectors to be passed during an interrupt acknowledge. All internal registers are read/write, with unused bits being read as zeros and ignored during write cycles. In the Interrupt Acknowledge mode, the $\overline{\text{INTACK}}$ input signals the F1761 that an interrupt acknowledge is occuring. The F1761 responds by placing the contents of one of seven vector registers on the data outputs, according to the value of the A_1, A_2, and A_3 signal inputs. For both Register Access and Interrupt Acknowledge modes, the device will assert $\overline{\text{DTACK}}$ to indicate the completion of the cycle. This $\overline{\text{DTACK}}$ signal is also asserted by the DRAM timing logic in response to a Request from the processor, with its timing programmed by the user.

The F1761 also includes an 8 to 3 bit Interrupt Priority Encoder which can be used to interface with the 68000 family of processors, with the Interrupt inputs ($\overline{\text{INTRQ}}_1$ - $\overline{\text{INTRQ}}_7$) latched on the falling edge of the Interrupt Latch Enable (ILE) input. The ILE input can be connected to the processor clock for glitch-free interrupting.

All of the DRAM interface timing is based upon the Master Clock (CP) input. Numerical values programmed into the Timing Registers indicate the number of clock cycles between events. When a 0 value is programmed into a timing skew, the two events indicated will happen simultaneously. The AC specifications indicate the amount of timing variation due to propogation delays within the device. The Master Reset input ($\overline{\text{MR}}$) initializes all timing registers to their maximum delay (All ones) and clears the Configuration Register.

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
$\overline{DS}$	2	2	Input	Active Low Data Strobe used to enable the Data Bus during register access cycles and the $\overline{CAS}$ outputs during DRAM access cycles.
$SIZ_0/\overline{LDS}$	3	3	Input	In 16-bit Mode, an active Low Lower Data Strobe signal used to enable the $\overline{CAS_1}$ output during a DRAM access cycle. In 32-bit Mode, an active High SIZE 0 signal used with SIZ_1 to indicate to the DIVC the size of the DRAM access transaction.
SIZ_1	4	4	Input	In 32-bit Mode, an active High SIZE 1 signal used with SIZ_0 to indicate to the DIVC the size of the DRAM access transaction.
$A_0/\overline{UDS}$	5	5	Input	In 16-bit Mode, an active Low Upper Data Strobe used to enable the $\overline{CAS_0}$ output during a DRAM access cycle. In 32-bit Mode, used with A1 to indicate to the DIVC the byte boundary of the DRAM access transaction.
A_1	6	6	Input	During DIVC register access, forms the least significant address bit of the register address. During DRAM access and in 32-bit Mode, used with A_0 to indicate to the DIVC the byte boundary of the DRAM access transaction.
A_2, A_3	7,8	7,8	Inputs	During DIVC register access, forms the most significant two address bits of the register address.
$\overline{REQ}$	1	1	Input	Active Low DRAM Access Request indicating to the DIVC that the processor wishes to access the DRAM controlled by the DIVC.
$\overline{CS}$	9	9	Input	Active Low Chip Select used for Register Access with the DIVC.
$R/\overline{W}$	10	10	Input	Read/Write signal used to indicate the direction of register access with the DIVC.
V_{CC}	11-14	11-14		Power Supply +5V ± 10%
$\overline{INTACK}$	15	13	Input	Active Low Interrupt Acknowledge signal used with the A_1, A_2, and A_3 inputs to assert the contents of one of seven internal Interrupt Vector Registers on the data bus (D_0-D_7).
$\overline{DTACK}$	16	14	Output	Active Low Data Transfer Acknowledge indicates to the processor the completion of a DIVC register or DRAM access cycle. For DRAM access, this signal's timing is programmable internally. Open Collector Output.
D_0-D_7	17-24	15-22	Input/ Output	Active High 3-State Data Bus over which data is transferred between the processor and internal registers of the DIVC.
$\overline{IPL_0}$ $\overline{IPL_1}$ $\overline{IPL_2}$	34 33 32	32 31 30	Output Output Output	Active Low Interrupt Priority Level signals indicating to the processor the priority level of the highest latched interrupt request on the $\overline{INTRQ}_{1\text{-}7}$ inputs. A level of all ONES indicates no interrupt rrequest pending
ILE	39	35	Input	Active High Interrupt Latch Enable which causes the internal latches connected to the $\overline{INTRQ}_{1\text{-}7}$ inputs to become transparent. A High-to-Low transition causes the $\overline{INTRQ}_{1\text{-}7}$ signals to be internally latched.
$\overline{INTRQ}_{1\text{-}7}$	31-25	41-38	Input	Active Low Interrupt Request inputs.
CP	40	36	Input	DIVC Clock input.
$\overline{MR}$	41	37	Input	Active Low Master Reset input.
$\overline{CAS}_{0\text{-}3}$	45-42	41-38	Output	Active Low Column Address Strobe inputs.
$\overline{REFEN}$	46	42	Output	Active Low Refresh Enable output. Indicates that the refresh address should be asserted.
MUX	47	43	Output	Active High Multiplexer output. Indicates that the column address should be asserted to the DRAMS.
$\overline{RAS}$	48	44	Output	Active Low Row Address Strobe inputs.
GND	35-38	33-34		Ground Reference.

TABLE 2. DIVC Register Selection Map

RSS[1]	A_3	A_2	A_1	ACRONYM	REGISTER NAME	MODE	AFFECTED BY RESET
X	0	0	0	CR	Configuration Register	R/W	Yes
0	0	0	1	RTR	Refresh Timing Register	R/W	Yes
0	0	1	0	TR2	Timing Register 2	R/W	Yes
0	0	1	1	TR3	Timing Register 3	R/W	Yes
0	1	0	0	TR4	Timing Register 4	R/W	Yes
0	1	0	1	TR5	Timing Register 5	R/W	Yes
0	1	1	0	-----	Reserved	-----	-----
0	1	1	1	-----	Reserved	-----	-----
1	0	0	1	VR1	Vector Register 1	R/W	No
1	0	1	0	VR2	Vector Register 2	R/W	No
1	0	1	1	VR3	Vector Register 3	R/W	No
1	1	0	0	VR4	Vector Register 4	R/W	No
1	1	0	1	VR5	Vector Register 5	R/W	No
1	1	1	0	VR6	Vector Register 6	R/W	No
1	1	1	1	VR7	Vector Register 7	R/W	No

NOTE:
1. RSS=Register Set Select Bit in the Configuration Register

REGISTER DESCRIPTION

Register Map

The DIVC contains a set of registers which can be programmed by a controlling processor to configure the DIVC for different bus sizes, DRAM timing, and Interrupt Vectors. Table 2 shows the Register Map of the DIVC. Note that the higher-order bit of the register address (RSS) is contained in the Configuration Register. Access to the Configuration Register is independent of the value of the RSS bit. By toggling the RSS bit, two sets of registers can be accessed. Those registers accessed with RSS = 0 are the DRAM timing registers for programming events during DRAM access. With RSS = 1, the seven Interrupt Vector registers can be accessed.

Configuration Register (CR)

This register configures the mode of access and register set select for the DIVC. **Bits 7 and 6** are used to specify the size of the bus to be used with the DRAM controlled by the DIVC. In the 8-bit mode, the Column Address Strobe outputs will respond to $\overline{CAS}$ signal assertion from the Timing Block by asserting one of the $\overline{CAS}$ outputs depending on the state of the A_0 and A_1 inputs, in binary fashion (i.e. If A_0=A_1=0 then $\overline{CAS_0}$=0; if A_0=0 and A_1=1 then $\overline{CAS_2}$=0). In 16-bit mode, the DIVC responds to a $\overline{CAS}$ assertion from the Timing Block by asserting $\overline{CAS_0}$ and $\overline{CAS_1}$ depending on the state of the $\overline{UDS}$ and $\overline{LDS}$ inputs, respectively. In 32-bit mode, the SIZ_0, SIZ_1, A_0, and A_1 inputs determine the state of the $\overline{CAS}$ outputs according to the decoding used with the 68020 Microprocessor, with $\overline{CAS_0}$ corresponding to the most significant byte and $\overline{CAS_3}$ corresponding to the least significant byte of the 32-bit bus. **Bit 5** is used as a register set select (RSS) for accessing the other registers in the DIVC. When RSS is low, registers 1 through 5 correspond to the Refresh Timing Register and Timing Registers 2 through 5. With RSS high, registers 1 through 7 correspond to Vector Registers 1 through 7. **Bit 4** is used to disable the refreshing operation of the DRAM Controller section of the DIVC. When set, no refreshes will be performed and internally generated Refresh Requests will be ignored, regardless of the state of the refresh timing parameters. Other bits in the Configuration Register are ignored on write cycles and are read as zeros on read cycles. All implemented bits of this register are reset to zeros when the DIVC is reset.

Refresh Timing Register (RTR)

The value in this register is used with a reloadable counter within the DIVC to generate refresh requests. Each time the counter counts down (using the CP clock divided by sixteen), a refresh request will be generated inside the DIVC. If no DRAM access is taking place, the DIVC immediately performs a refresh cycle, using the REFRESH RASON to RASOFF delay programmed into Timing Register 2, and the RASOFF to REFRESHOFF delay programmed into Timing Register 3. If a DRAM access cycle has already begun, the DIVC will wait until the completion of the DRAM access cycle, after which it will perform the refresh cycle as explained. A value of all zeros will program the DIVC with the shortest possible delay between refresh requests: 16 CP clock cycles. At 100 MHz., this register gives a refresh period resolution of 160 nsec. Resetting the DIVC changes all bits to ones.

Timing Register 2 (TR2)

Bits 0 to 4 of this register program the $\overline{RAS}$ pulse width of a refresh cycle in CP clock cycles. Although a value of zero would normally result in no $\overline{RAS}$ pulse during a refresh cycle, internal propagation delay's cause a small $\overline{RAS}$ pulse to be output. Resetting the DIVC will result in all these bits being set to ones. **Bits 5 to 7** are ignored during write cycles and read as zeros during read cycles.

Timing Register 3 (TR3)

Bits 0 to 3 of this register program the

Table 3. REGISTER BIT FORMATS

Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CR	BUS SIZING		RSS	RD	UNIMPLEMENTED			
	00 = 8 Bit Mode 01 = 16 Bit Mode 10 = 32 Bit Mode 11 = Invalid		See Text	Refresh Disable				

Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RTR	REFRESH TIMING COUNTER VALUE							
	Refresh Period in CP/16 Cycles							

Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
TR2	UNIMPLEMENTED			REFRESH RAS PULSE WIDTH				
				CP Cycles				

Register	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
TR3	UNIMPLEMENTED			REFRESH RAS OFF TO REFRESH OFF				
				CP Cycles - 1				

delay between $\overline{RAS}$ negated and the end of a refresh cycle. Because an access cycle could begin immediately after the refresh, some delay may be desired between RASOFF and the end of the refresh cycle to accomodate $\overline{RAS}$ precharge requirements of the DRAMs. The value programmed into these bits should be one less than the number of clock cycle delays desired. Resetting the DIVC will result in these bits being set to ones. **Bits 4 to 7** are ignored during write cycles and read as zeros during read cycles.

Timing Register 4 (TR4)
Bits 5-7 of this register program the DIVC with the ACCESS GRANT TO $\overline{RAS}$ delay of a DRAM access cycle in CP clock cycles. Since the $\overline{REFEN}$ output is asserted during a refresh cycle, it is commonly used as a select signal for address multiplexers that select between a processor address and the refresh row address. If, on the completion of a refresh cycle, the DIVC immediately performs an access cycle, there may be a need to wait until the processor's row address has become stable at the DRAMs, before asserting $\overline{RAS}$. (Since the $\overline{REFEN}$ output is negated at the same time as the refresh $\overline{RAS}$ output, and there is a programmable delay between RASOFF and REFRESHOFF, the problem is associated with the application. See explanation of bits 3-7 in Timing Register 3) These bits can be programmed with the number of clock cycles to wait from the time that an access is granted until $\overline{RAS}$ is asserted. A value of zero will result in no delay between events. **Bits 3 and 4** configure the timing between $\overline{RAS}$ and the MUX output asserted in CP clock cycles. A value of zero in these bits will cause no delay between $\overline{RAS}$ and MUX. **Bits 0 to 2** configure the timing between MUX asserted and $\overline{CAS}$ asserted in CP clock cycles. A value of zero in these bits will cause no delay between MUX and $\overline{CAS}$. Resetting the DIVC sets all bits of this register to ones.

Timing Register 5 (TR5)
Bits 5 to 7 of this register program the delay between the assertion of CAS and the negation of $\overline{RAS}$, in CP clock cycles. A value of zero in these bits results in no delay between these events. **Bits 0 to 4** program the delay beween the assertion of $\overline{RAS}$ and the assertion of $\overline{DTACK}$ back to the processor over the chip's DTACK signal pin. A value of zero in these bits results in no delay between these events. Resetting the DIVC will result in all bits of this register being set to ones.

Interrupt Vector Registers 1 to 7 (VR1-7)
Each of these registers can be programmed to contain the 8-bit vector to be placed on the DIVC's data bus during an Interrupt Acknowledge cycle. When the processor asserts the $\overline{INTACK}$ and $\overline{DS}$ inputs and places the Interrupt Priority on the A_1, A_2, and A_3 inputs, the DIVC will respond by placing the contents of the Interrupt Vector Register addressed by these address inputs on the data bus and asserting $\overline{DTACK}$. In this way, peripheral devices which do not contain the interrupt acknowledging circuitry can be used with a processor which expects these kinds of acknowledge cycles to occur. Resetting the DIVC does not affect the contents of these registers.

TABLE 3. REGISTER BIT FORMATS (Continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	GRANT TO RAS DELAY			RAS TO MUX DELAY		MUX TO CAS DELAY		
TR4	CP Cycles			CP Cycles		CP Cycles		

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	CAS TO RAS OFF DELAY			RAS TO DTACK DELAY				
TR5	CP Cycles			CP Cycles				

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	INTERRUPT VECTOR VALUE							
VR1-VR7								

TABLE 4. CAS DECODING SUMMARY

MODE	$SIZ_0/\overline{LDS}$	SIZ_1	$A_0/\overline{UDS}$	A_1	$\overline{CAS_0}$	$\overline{CAS_1}$	$\overline{CAS_2}$	$\overline{CAS_3}$
8	X	X	0	0	0	1	1	1
8	X	X	1	0	1	0	1	1
8	X	X	0	1	1	1	0	1
8	X	X	1	1	1	1	1	0
16	1	X	1	X	1	1	1	1
16	1	X	0	X	0	1	1	1
16	0	X	1	X	1	0	1	1
16	0	X	0	X	0	0	1	1
32	1	0	0	0	0	1	1	1
32	1	0	1	0	1	0	1	1
32	1	0	0	1	1	1	0	1
32	1	0	1	1	1	1	1	0
32	0	1	0	0	0	0	1	1
32	0	1	1	0	1	0	0	1
32	0	1	0	1	1	1	0	0
32	0	1	1	1	1	1	1	0
32	1	1	0	0	0	0	0	1
32	1	1	1	0	1	0	0	0
32	1	1	0	1	1	1	0	0
32	1	1	1	1	1	1	1	0
32	0	0	0	0	0	0	0	0
32	0	0	1	0	1	0	0	0
32	0	0	0	1	1	1	0	0
32	0	0	1	1	1	1	1	0

NOTE: This table gives the functional decoding of the $\overline{CAS}$ output signals of the DIVC when $\overline{DS}$ is valid and the DRAM timing circuitry asserts $\overline{CAS}$.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-35	mA
I_{OL}	Low-level output current			60	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH2}[3] = -35mA	±10%V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60mA	±10%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC}= MIN, $I_I = I_{IK}$				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]	V_{CC} = MAX, V_O = 2.25V			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC}= MAX				200	220	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low to High transition in a 70Ω transmission line and is specified for the $\overline{RAS}$, $\overline{CAS}_{0-3}$, MUX, and $\overline{REFEN}$ signals.
4. I_{OL2} is the current necessary to guarantee a High to Low transition in a 70Ω transmission line and is specified for the $\overline{RAS}$, $\overline{CAS}_{0-3}$, MUX, and $\overline{REFEN}$ signals.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS $T_A = +25°C$, $V_{CC} = 5V$, $C_L = 300pF$, $R_L = 70\Omega$			LIMITS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1 (1)	100	110		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CS}$ or $\overline{DS}$ to D_n (Read)	Waveform 3 (10) Test Circuit 2		5.0 5.0	8.0 8.0		10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CS}$ or $\overline{DS}$ negated to D_n invalid (Read)	Waveform 3 (11) Test Circuit 2		8.0 8.0	10.0 10.0		12.0 12.0	ns
t_{PHL}	Propagation delay $\overline{CS}$ to $\overline{DTACK}$ asserted	Waveform 3,4 (12) Test Circuit 3		4.0	5.0		6.0	ns
t_{PLH}	Propagation delay $\overline{CS}$ negated to $\overline{DTACK}$ negated	Waveform 3,4 (13) Test Circuit 3		4.0	5.0		6.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n (data in) invalid to $\overline{DS}$ negated (Write)	Waveform 4 (15)		0 0	0 0	0 0		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{DS}$ negated to D_n (data in) invalid (Write)	Waveform 4 (16)		5.0 5.0	3.0 3.0	5.0 5.0		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INTACK}$ or $\overline{DS}$ to D_n (data out)	Waveform 8 (20) Test Circuit 2		5.0 5.0	8.0 8.0		10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{INTACK}$ or $\overline{DS}$ negated to D_n (data out) invalid	Waveform 8 (21) Test Circuit 2		8.0 8.0	10.0 10.0		10.0 10.0	ns
t_{PHH}	Propagation delay $\overline{INTACK}$ asserted to $\overline{DTACK}$ asserted	Waveform 8 (22) Test Circuit 3		4.0	6.0		7.0	ns
t_{PLL}	Propagation delay $\overline{INTACK}$ negated to $\overline{DTACK}$ negated	Waveform 8 (23) Test Circuit 3		4.0	5.0		6.0	ns
t_{PLL}	Propagation delay, Worst case $\overline{REQ}$ negated to $\overline{RAS}$ with 000 IN TR4	Waveform 6 (25)			8.0 +Tcp		11 +Tcp	ns
t_{PHL}	Propagation delay, CP to $\overline{RAS}$ asserted	Waveform 6 (26)		6.0	9.0 [7.0]		11.0 [9.0]	ns
t_{PHH}	Propagation delay, CP to $\overline{RAS}$ negated	Waveform 6 (27)		10.0	14.0 [7.0]		16.0 [9.0]	ns
t_{PHH}	Propagation delay, CP to MUX asserted	Waveform 6 (28) Test Circuit 2		7.0	8.0 (7.0)		10.0 [12.0]	ns
t_{PHL}	Propagation delay $\overline{REQ}$ negated to MUX negated	Waveform 6 (29) Test Circuit 2		5.0	6.0		8.0	ns
t_{PHL}	Propagation delay, CP to $\overline{CAS}$ asserted	Waveform 6 (30)		9.0	12.0 [14.0]		14.0 [16.0]	ns
t_{PHH}	Propagation delay $\overline{REQ}$ negated to $\overline{CAS}$ negated	Waveform 6 (31)		8.0	10.0		12.0	ns
t_{PHL}	Propagation delay CP to $\overline{DTACK}$ asserted	Waveform 6 (34) Test Circuit 3		7.0	9.0 [11.0]		110 [13.0]	ns
t_{PHH}	Propagation delay $\overline{REQ}$ negated to $\overline{DTACK}$ negated	Waveform 6 (35) Test Circuit 3		5.0	7.0		9.0	ns
t_{PHL}	Propagation delay, CP to $\overline{REFEN}$ asserted	Waveform 5 (36) Test Circuit 3		4.0	5.0		6.0	ns
t_{PHH}	Propagation delay, CP to $\overline{REFEN}$ negated	Waveform 5 (38) Test Circuit 3		5.0	10.0		12.0	ns
t_{PHL}	Propagation delay CP to Refresh $\overline{RAS}$ asserted	Waveform 5 (37)		5.0	6.0		7.0	ns
t_{PHH}	Propagation delay CP to Refresh $\overline{RAS}$ negated	Waveform 5 (39)		5.0	11.0		13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INTRQ}$ asserted to $\overline{IPL}$ asserted	Waveform 7 (43) Test Circuit 2		5.0	10.0		12.0	ns

NOTES: 1. Worst case $\overline{REQ}$ to $\overline{RAS}$ assumes that $\overline{REQ}$ did not meet setup time requirements on the last rising edge of CP, that 000 was programmed into the GRANT to $\overline{RAS}$ delay in TR4, and that no refresh request is pending of being executed. Tcp is AC parameter number 1.

2. Numbers in square brackets indicarte propagation delay with 0 programmed into the appropriate delay field.

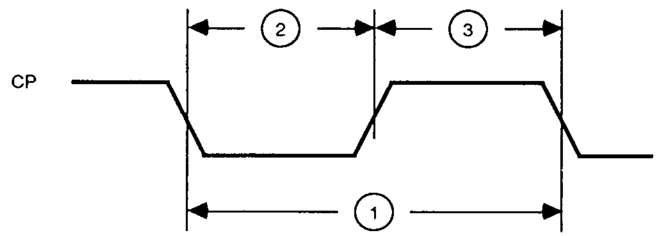
3. Numbers in round brackets in the TEST CONDITION column correspond to numbers (in circles) in AC WAVEFORMS .

AC SETUP REQUIREMENTS

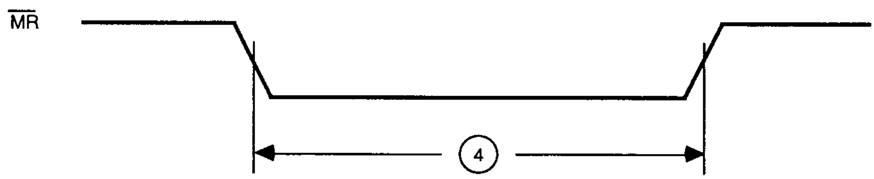
SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω Min	Typ	Max	LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω Min	Max	UNIT
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_1 - A_3 to $\overline{CS}$	Waveform 3,4 (6)	5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_1 - A_3 to $\overline{CS}$	Waveform 3,4 (7)	3.0 3.0	2.0 2.0		3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low R/$\overline{W}$ to $\overline{CS}$	Waveform 3,4,8 (8)	5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low R/$\overline{W}$ to $\overline{CS}$	Waveform 3,4,8 (9)	3.0 3.0	2.0 2.0		3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_1 - A_3 to $\overline{INTACK}$	Waveform 8 (17)	5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_1 - A_3 to $\overline{INTACK}$	Waveform 8 (19)	3.0 3.0	2.0 2.0		3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{INTRQ}$ to ILE	Waveform 7 (40)	8.0 8.0	6.0 6.0		10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{INTRQ}$ to ILE	Waveform 7 (41)	6.0 6.0	8.0 8.0		10.0 10.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low SIZ_0, SIZ_1, A_0, A_1 to $\overline{CAS}$	Waveform 6 (32)	4.0 4.0	3.0 3.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SIZ_0, SIZ_1, A_0, A_1 to $\overline{CAS}$	Waveform 6 (33)	0 0	0 0		0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}$ to CP	Waveform 6 (24)	2.0 2.0	1.2 1.2		2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1 (3,2)	5.0 5.0	4.0 4.0		5.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2 (4)	20	15		20		ns
$t_w(L)$	$\overline{CS}$ Pulse width, Low	Waveform 3,4 (5)	50	40		50		ns
$t_w(L)$	$\overline{DS}$ Pulse width, Low	Waveform 4 (14)	30	25		30		ns
$t_w(L)$	$\overline{INTACK}$ Pulse width, Low	Waveform 8 (17)	30	25		30		ns
$t_w(L)$	ILE Pulse width, Low	Waveform 7 (42)	17	15		12		ns

NOTES:
1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.
2. Numbers in round brackets in the TEST CONDITIONS column correspond to numbers (in circles) in AC WAVEFORMS

AC WAVEFORMS



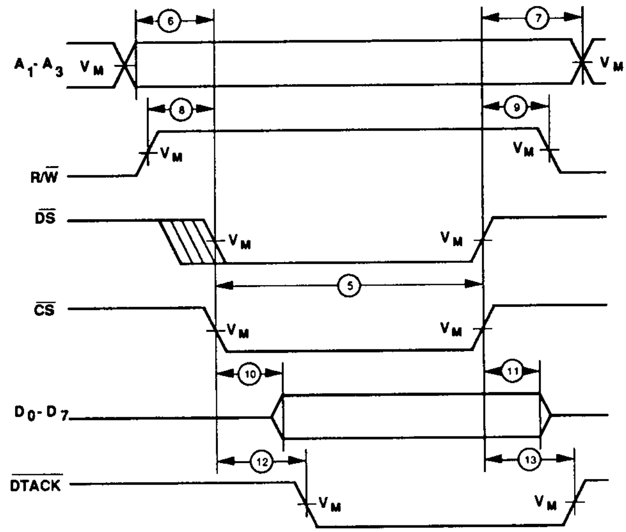
Waveform 1. CP Timing



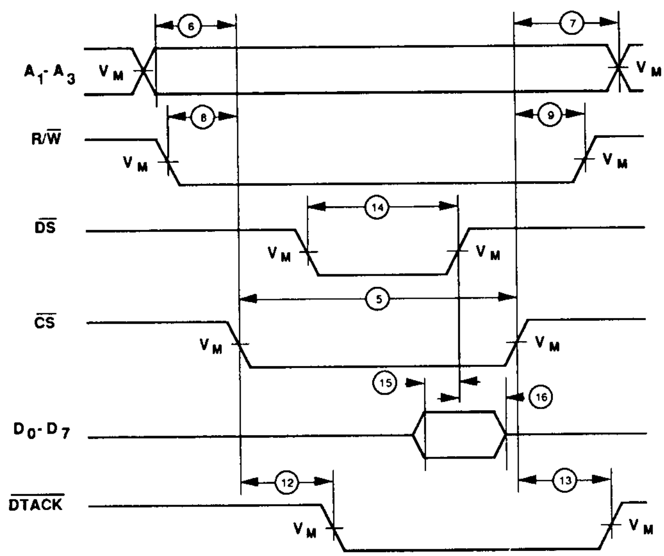
Waveform 2. MR Timing

NOTE: For all waveforms, V_M = 1.5V.

AC WAVEFORMS



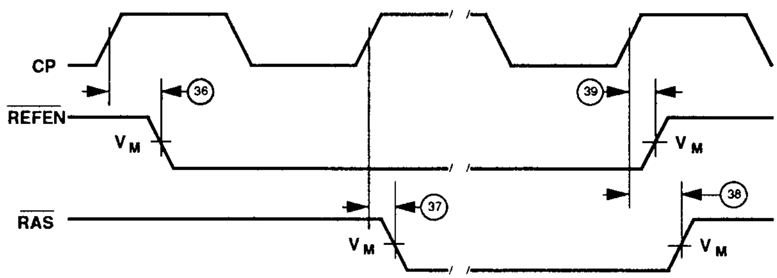
Waveform 3. Bus Timing (Read Cycle)



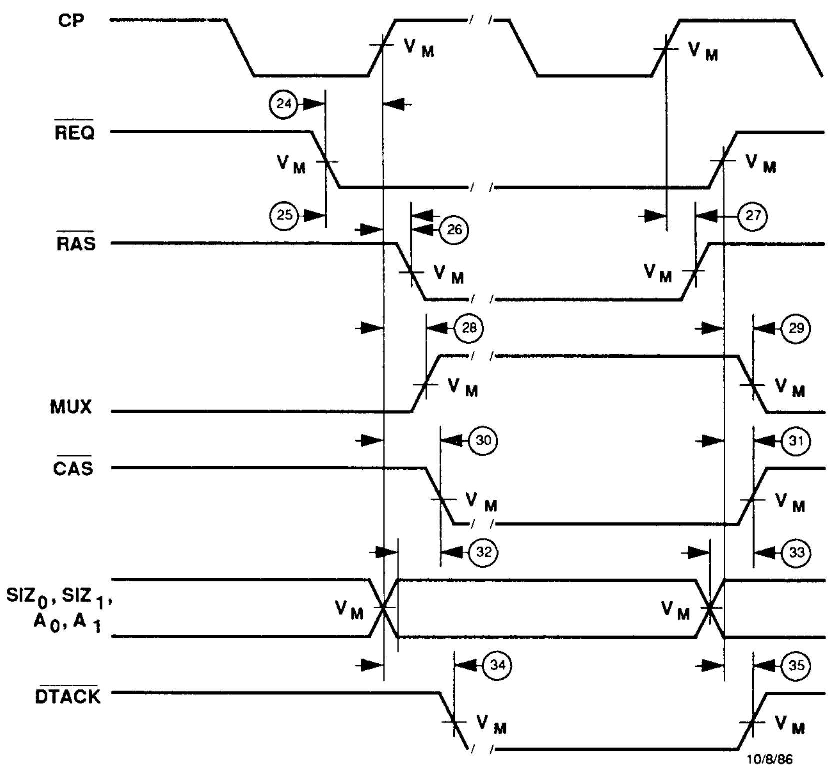
Waveform 4. Bus Timing (Write Cycle)

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



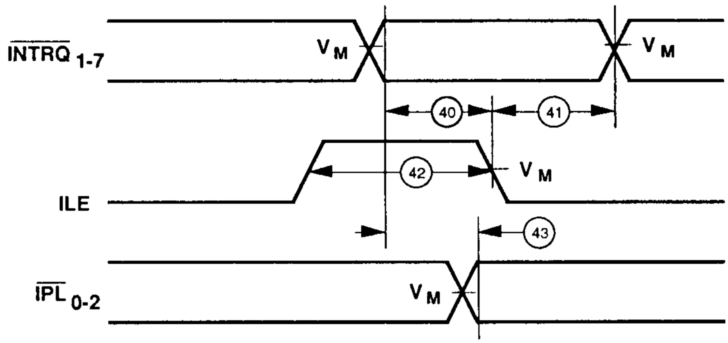
Waveform 5. Refresh Timing



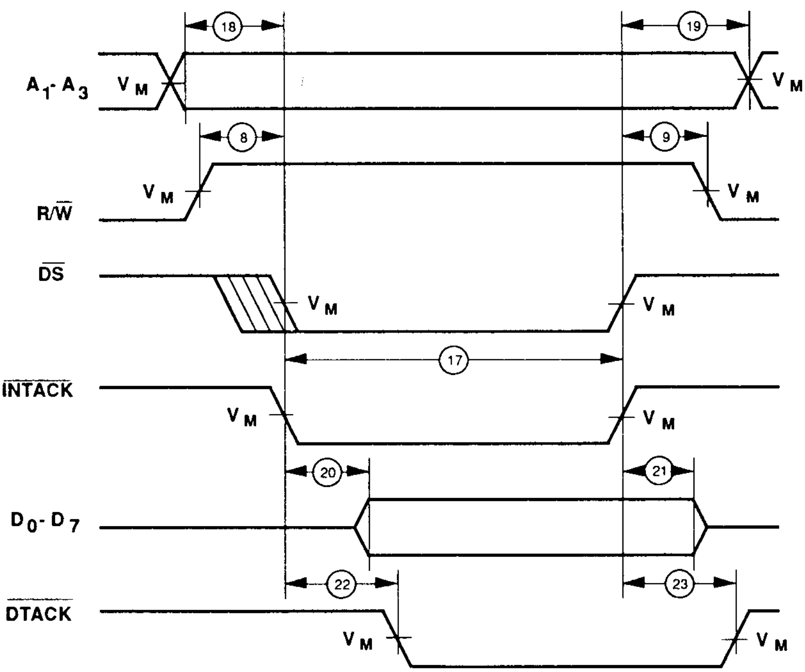
Waveform 6. DRAM Access Timing

NOTE: For all waveforms, $V_M = 1.5V$.

AC WAVEFORMS



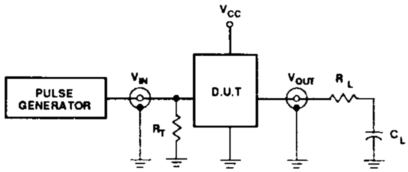
Waveform 7. Interrupt Request Timing



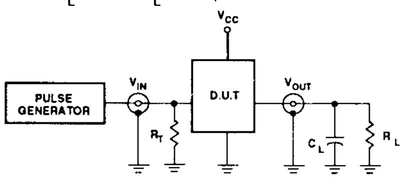
Waveform 8. Interrupt Acknowledge Timing

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

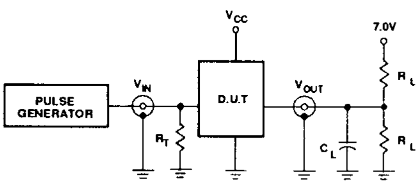
TEST CIRCUITS AND WAVEFORMS



Test Circuit 1 for $\overline{RAS}$ and $\overline{CAS}$ signals
R_L = 70 Ω, C_L = 300 pF



Test Circuit 2 for microprocessor interface signal
R_L = 500 Ω, C_L = 50 pF



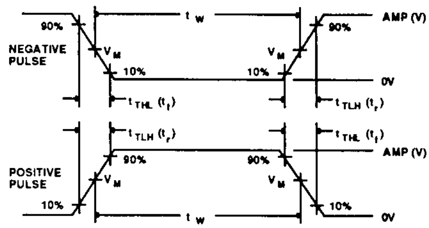
Test Circuit 3 for $\overline{DTACK}$ signal
R_L = 500 Ω, C_L = 50 pF

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns