

TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE MOS

TMM2366P

020666

DESCRIPTION

The TMM2366P is a 65536 bit fully static read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using micro-processor.

The TMM2366P also features an automatic standby power mode. When deselected by Chip Enable (CE/ \overline{CE}), the operating current is reduced from 100mA (MAX) to 25mA (MAX).

The TMM2366P is fabricated with ion implanted N-channel silicon gate technology.

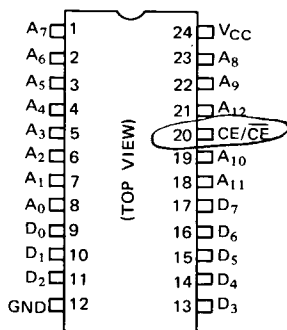
This technology allows a production of high performance.

The TMM2366P is moulded in a 24 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V power Supply
- Access Time: 200ns max.
- Power Dissipation
 - Average Current: 100mA max.
 - Standby Current: 25mA max.
- Input and Output: TTL Compatible
- Three State Outputs: Wired OR Capability
- Programmable Chip Enable: CE/ \overline{CE}
- Compatible with TMS4764

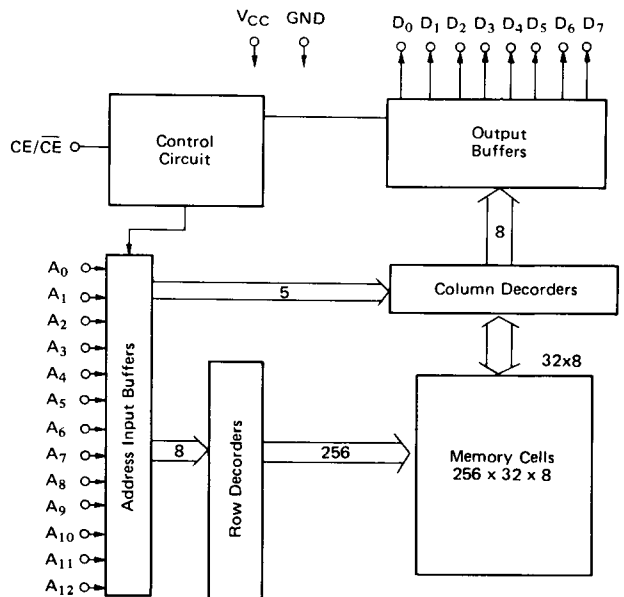
PIN CONNECTION



PIN NAMES

A ₀ ~ A ₁₂	Address inputs
D ₀ ~ D ₇	Data outputs
CE/ \overline{CE}	Chip enable input
V _{CC}	Power supply terminal
GND	Ground

BLOCK DIAGRAM



TMM2366P

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	-0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{SD}	Soldering Temperature Time	260 · 10	°C · sec
P_D	Power Dissipation ($T_a = 70^\circ\text{C}$)	1.0	W

D.C. OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	—	2.0	—	$V_{CC}+1$	V
V_{IL}	Input Low Voltage	—	-0.5	—	0.8	V
V_{CC}	Power Supply Voltage	—	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IH}	Input High Current	$V_{IN} = 5.5\text{V}$	—	10	μA
I_{IL}	Input Low Current	$V_{IN} = \text{GND}$	—	-10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 3.2\text{mA}$	—	0.4	V
I_{LO}	Output Leakage Current	$0\text{V} \leq V_{OUT} \leq V_{CC}$	-10	10	μA
I_{CC1}	Standby Current	$\overline{CE} = 2.0\text{V}, CE = 0.8\text{V}$	—	25	mA
I_{CC2}	Average Current	$t_{CYC} = 200\text{ns}, I_{OUT} = 0\text{mA}$	—	100	mA

A.C. CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	—	200	ns
t_{CE}	Output Delay Time from CE/ \overline{CE}	—	200	ns
t_{OD}	Output Turn off Delay	—	60	ns
t_{CYC}	Cycle Time	200	—	ns

A.C. TEST CONDITIONS

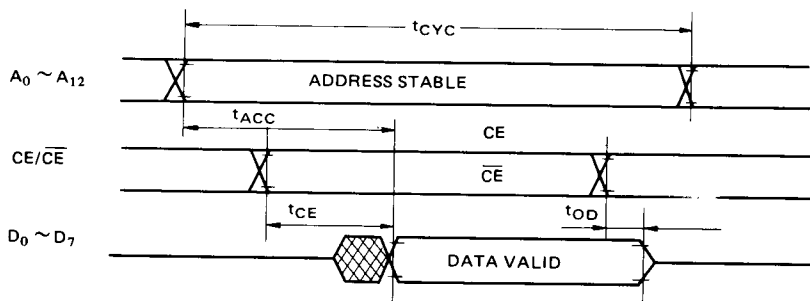
- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5 ns
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Levels : Input; 1V and 2.0V
Output; 0.8V and 2.0V

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{A.C. GND}$	—	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{A.C. GND}$	—	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



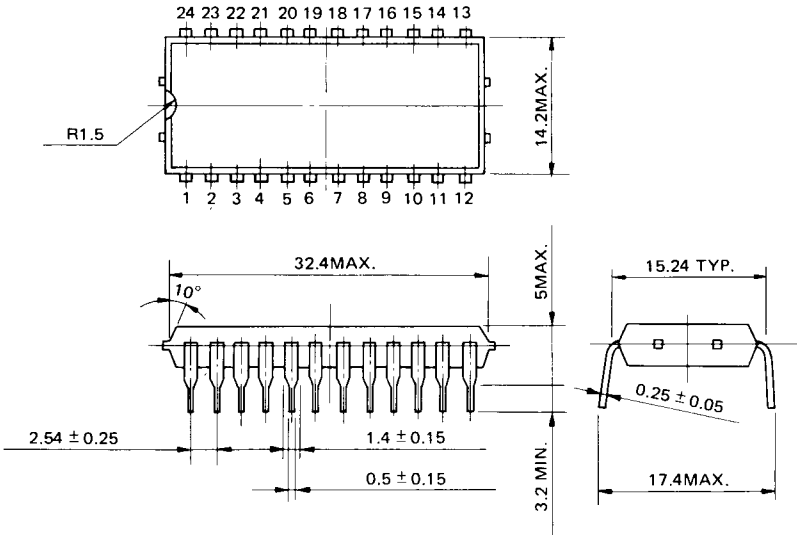
POWER ON

The TMM2366 has a self substrate-bias generator internally. So a minimum 100 μs time delay is

required after the application of V_{CC} (4.5 ~ 5.5V) before proper device operation is achieved.

TMM2366P

OUTLINE DRAWING



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads.