SILICON STACKED GATE CMOS

262,144 WORD x 16 BIT/524,288 WORD x 8 BIT CMOS MASK ROM

Description

The TC534200P/F is a 4,194,304 bit read only memory organized as 262,144 words by 16 bits when $\overline{BYTE}$ is logical high and organized as 524,288 words by 8 bits when $\overline{BYTE}$ is logical low.

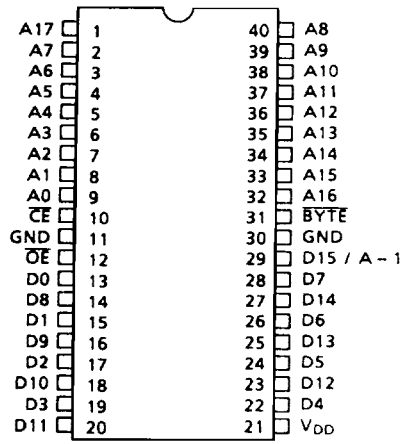
The TC534200P/F is suitable for use as program memory, data memory, or as a character generator.

The TC534200P/F is packaged in a standard 600mil 40-pin DIP or 525mil 40-pin SOP.

Features

- Single 5V power supply
- Access time : 150ns (max.)
- Power dissipation
  - Operating current : 50mA (max.)
  - Standby current : 20μA (max.)
- Fully static operation
- Inputs and outputs TTL compatible
- Three state outputs
- Package
  - TC534200P : DIP40-P-600
  - TC534200F : SOP40-P-525

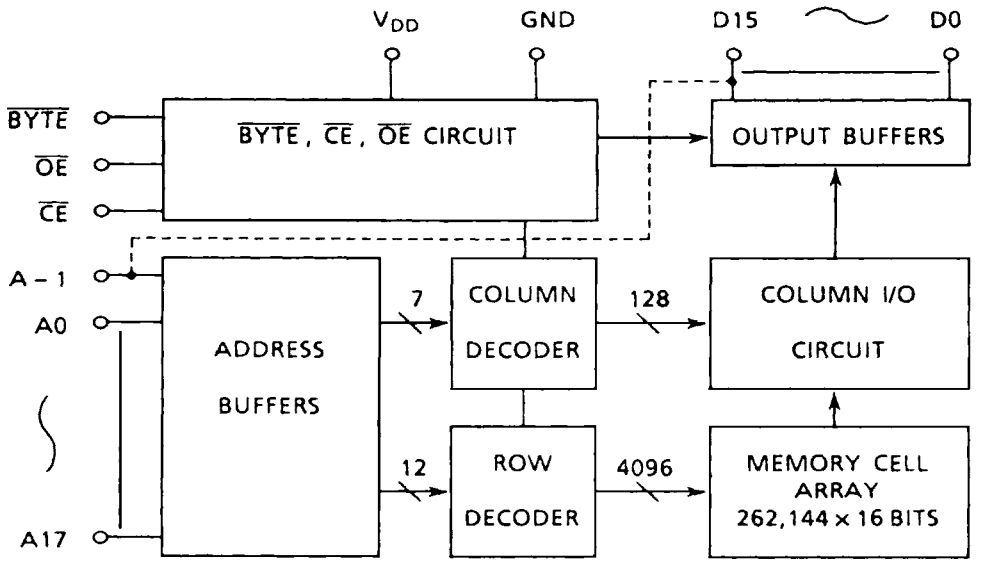
Pin Connection (Top View)



Pin Names

A0 ~ A17	Address Inputs
D0 ~ D14	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
D15/A - 1	Data Output/Address Input
$\overline{BYTE}$	Word, Byte Selection Input
V_{DD}	Power Supply Voltage
GND	Ground

Block Diagram



Operating Mode

MODE	$\overline{CE}$	$\overline{OE}$	BYTE	D0 ~ D7	D8 ~ D14	D15/A - 1	POWER
Read (16 Bits)	L	L	H	Data Out			Active
Read (Lower 8 Bits)	L	L	L	Data Out (Lower 8 Bits)	High Impedance	L	Active
Read (Upper 8 Bits)	L	L	L	Data Out (Upper 8 Bits)	High Impedance	H	Active
Output Deselect	L	H	*	High Impedance			Active
Standby	H	*	*	High Impedance			Standby

H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-0.5 ~ V_{DD}	
V_{OUT}	Output Voltage	0 ~ V_{DD}	
P_D	Power Dissipation	1.0/0.6*	W
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

* SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	-0.3	–	0.8	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	±1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 ~ V_{DD}	–	±5.0	
I_{OH}	Output High Current	V_{OH} = 2.4V	-1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	–	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	2	
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V	–	20	µA
I_{DDO1}	Operating Current	V_{IN} = V_{IH}/V_{IL}, t_{cycle} = 150ns	–	60	mA
I_{DDO2}		V_{IN} = V_{DD} - 0.2V/0.2V, t_{cycle} = 150ns	–	50	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CE}	Chip Enable Access Time	–	150	
t_{BT}	$\overline{BYTE}$ Access Time	–	150	
t_{OE}	Output Enable Access Time	–	70	
t_{CED}	Output Disable Time from $\overline{CE}$	–	60	
t_{OED}	Output Disable Time from $\overline{OE}$	–	60	
t_{BTD}	Output Disable Time from $\overline{BYTE}$	–	60	
t_{OH}	Output Hold Time	5	–	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Times	5ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

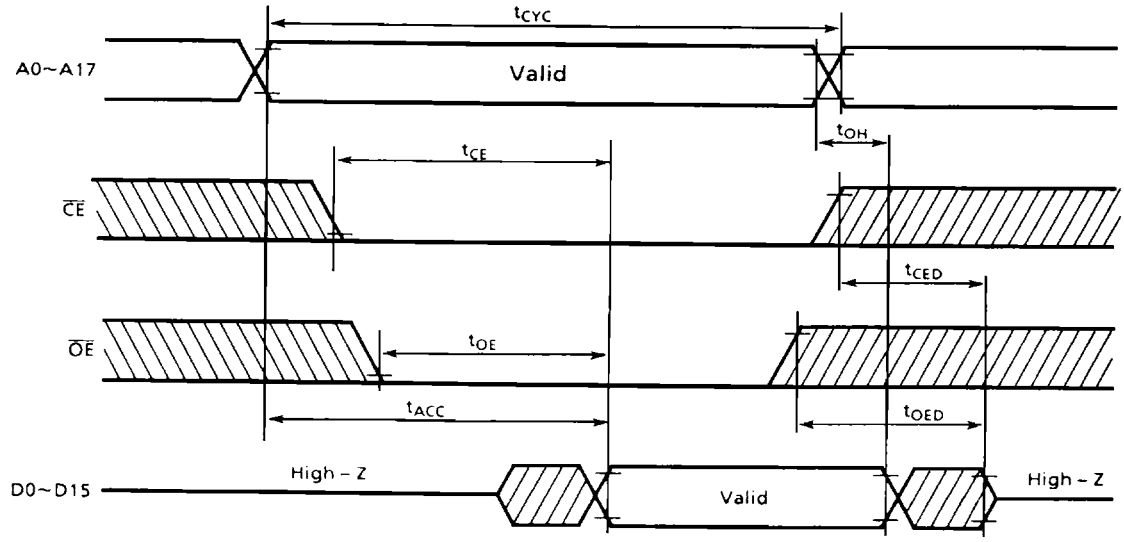
Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	12	

*This parameter is periodically sampled and is not 100% tested.

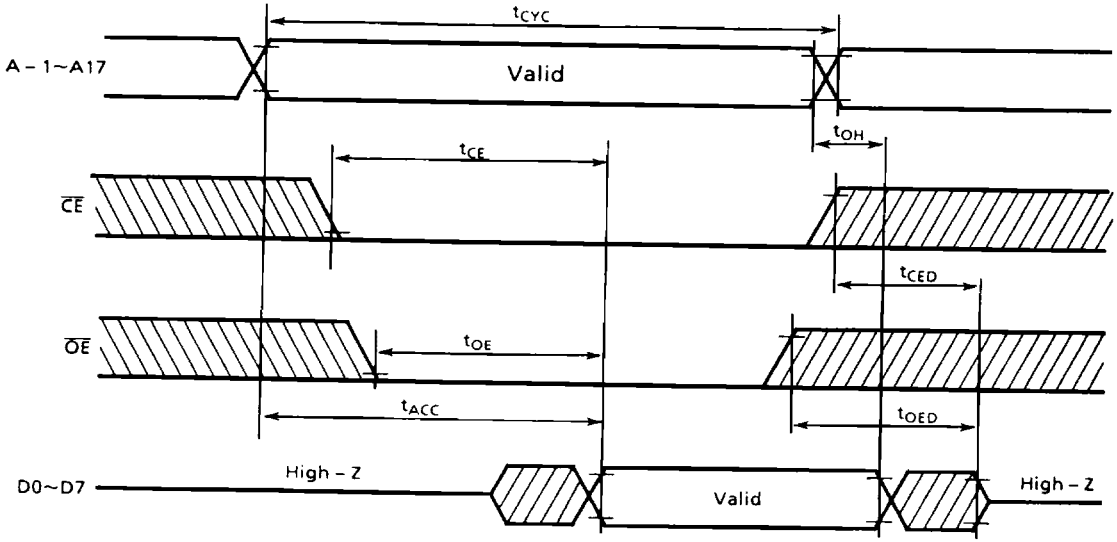
Timing Waveforms

Word-Wide (16 Bit) Read Mode



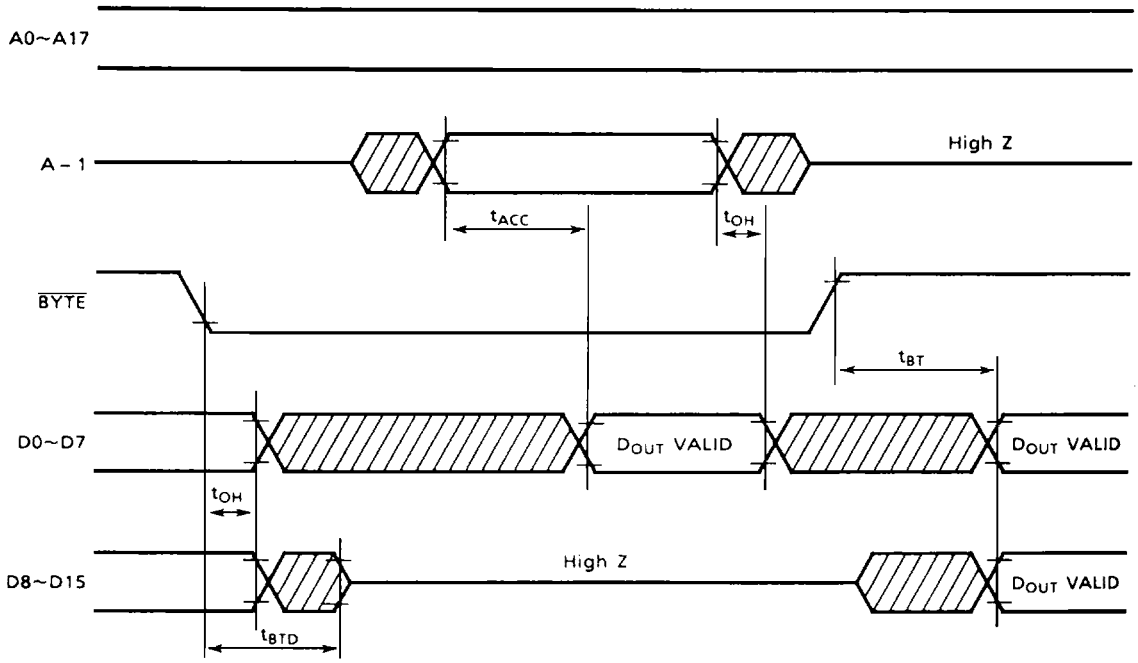
Note: $\overline{BYTE}$ = V_{IH}

Byte-Wide (8 Bit) Read Mode



Note: $\overline{BYTE}$ = V_{IL}

$\overline{\text{BYTE}}$ Transition



Note: $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$