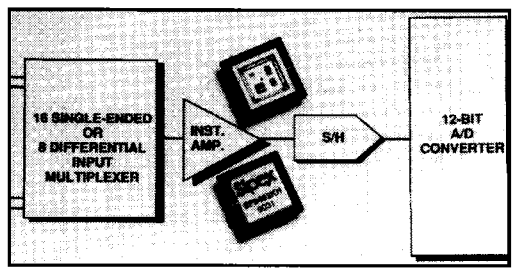
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9462, SP9472, SP9463, SP9473
12–BIT DATA ACQUISITION SYSTEM

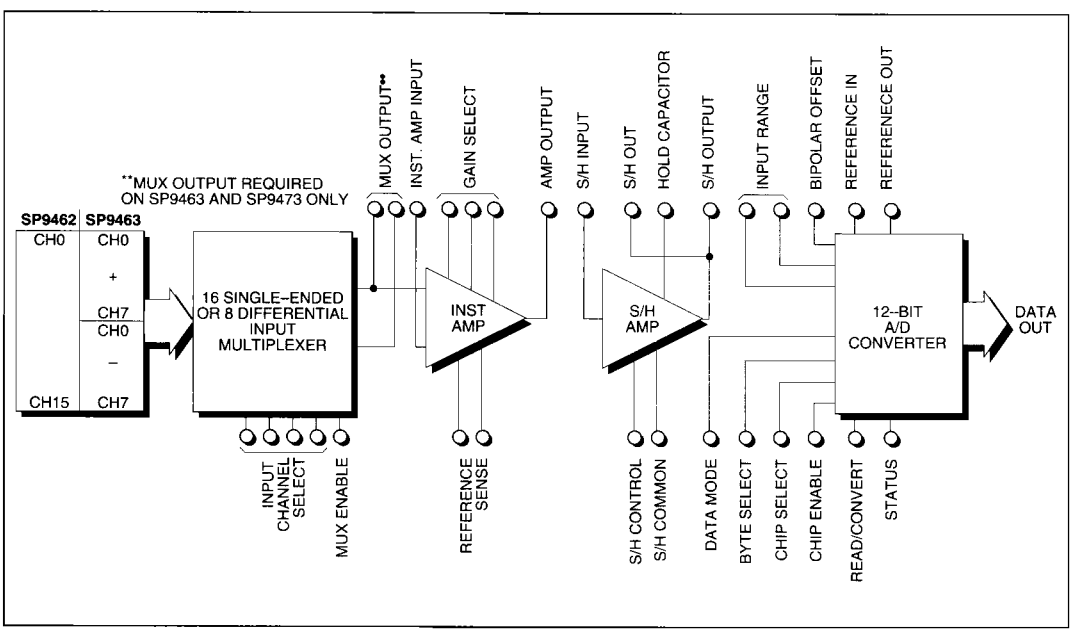
FEATURES

- Complete 12–Bit Data Acquisition System
- Guaranteed No Missing Codes over Temperature
- Three State Output
- 33 KHz or 50KHz Throughput Rate
- Selectable Gains of 1, 10 and 100
- Small Pin Grid Array Package
- Input Ranges Selectable for Unipolar or Bipolar Operation



DESCRIPTION

The **SP9462/9472** and **SP9463/9473** are complete data acquisition systems in a 68–pin grid array package. The **SP9462/9472** include a 16–channel input multiplexer, selectable gain instrumentation amplifier, sample–and–hold amplifier, a single chip 12–Bit Analog to Digital Converter with 3–state output buffers. The **SP9463/9473** are the 8 differential input channel devices equivalent to the **SP9462/9472**. All models accept unipolar or bipolar voltage inputs of 0 to +10V, ±5V and ±10V. The instrumentation amplifier can be selected for gains of 1, 10 and 100 by pin–strapping pins. The **SP9462/9472** and **SP9463/9473** are available in two temperature ranges: 0 to +70°C, and –55 to +125°C, with MIL–STD–883C screening available.



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SPECIFICATIONS

At 25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor at 4700pF. All grades are burned-in at +125°C for 168 hour.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RESOLUTION		**12**		**BITS**	
INPUT CHARACTERISTICS					
ANALOG					
Voltage Ranges:					
Bipolar		±5, ±10		V	
Unipolar		0–10		V	
Input Impedence:					
On Channel		10^{10}		Ω	
Off Channel		10^{10}		Ω	
Input Capacitance:					
On Channel		20		pF	
Off Channel		20		pF	
CMRR[7]	80	85	–80	dB	(20VDC to 1KHz)
Crosstalk[7]		–85	–80	dB	(20VP–P, 1KHz)
Feedthrough[7]		–85	100	dB	(at 1KHz)
Offset[2]		30	5	µV	(channel to channel) G=1
Input Bias Current/Channel		1		nA	
Input Voltage Range[3]	+10	+11		V	
	–10	–15		V	
DIGITAL					
MUX Input Channel Select:					
Logic '1' (4V)		5	30	µA	
Logic '0' (0.8V)		5	30	µA	
S/H Command:					
Logic '1' (2.4V)		0.2		nA	
Logic '0' (0.8V)		5	30	µA	
ADC Section:					
Logic '1' (2.4V)			10	µA	
Logic '0' (0.8V)		10		µA	
TRANSFER CHARACTERISTICS					
ACCURACY					
Integral of Linearity[4]:					
JH, SH			±0.024	%FSR	
KH, TH			±0.012	%FSR	
Differential Linearity[4]:					
JH, SH			±0.024	%FSR	
KH, TH			±0.012	%FSR	
Gain Error[5]					
G=1		0.7		%	
G=100		0.9		%	
Unipolar Offset Error[5]		16		mV	
Bipolar Offset Error[5]		50		mV	
Noise Error[7]		0.5	1	mV P–P	(Measured at S/H Output) G=1
Droop Rate[7]		50	500	µV/mS	
Temperature Coefficients:					
Unipolar Offset					
JH, SH		20		ppm of FSR/°C	
KH, TH		15		ppm of FSR/°C	
Bipolar Offset					
JH, SH		30		ppm of FSR/°C	
KH, TH		25		ppm of FSR/°C	
Full Scale Calibration					
JH, SH		60		ppm of FSR/°C	
KH, TH		35		ppm of FSR/°C	
SYSTEM TIMINGS					
ADC Conversion Time:					
SP9462/SP9463	15	20	25	µS	
SP9472/SP9473	9	12	15	µS	
S/H Aperture Delay		50		ns	
S/H Aperture Uncertainty		2		ns	

SPECIFICATIONS (continued) At 25°C, V_{CC} = ±15V, V_{DD} = 5V, external sample/hold capacitor at 4700pF. All grades are burned-in at +125°C for 168 hour.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
TIMING					
Acquisition Time:					
(to 0.01% of final value					
for full-scale step)		5		µS	
Throughput:					
(Serial Mode)					
SP9462/SP9463[7]			22	KHz	
SP9472/SP9473[7]			22.8	KHz	
(Overlap Mode)					
SP9462/SP9463[7]			31.7	KHz	
SP9472/SP9473[7]			46.5	KHz	
MULTIPLEXER[6]					
Switching Time		1.5		µS	(between channels)
Settling Time		2.5		µS	(10V step to 0.02%)
Enable Time:					
On[7]		1	2	µS	
Off[7]		0.25	0.5	µS	
INSTRUMENTATION AMPLIFIER[6]					
Settling Time:					(20V step to 0.01%)
G=1[7]		5	12.5	µS	
G=10[7]		3	7.5	µS	
G=100[7]		4	7.5	µS	
Slew Rate[7]	12	17		V/µS	
S/H AMPLIFIER[6]					
Acquisition Time		5		µS	(10V step to 0.01%)
Aperture Delay		50		ns	
Hold mode settling time		1.5		µS	
Slew rate		10		V/µS	
DIGITAL OUTPUT DATA					
Output Codes:					
Unipolar	Unipolar Straight Binary (USB)				
Bipolar	Bipolar Offset Binary (BOS)				
Logic Levels:					
Logic 0			+0.4	V	sink = 1.6mA
Logic 1	+2.4			V	source = 500µA
Leakage (Data Bits Only)	–5	+0.1	+5	µA	High-Z State
POWER SUPPLY REQUIREMENTS					
Rated Voltage:					
Analog	14.25	15	15.75	VDC	$\pm V_{CC}$
Digital	4.75	5	5.25	VDC	V_{DD}
Supply Drain:					
+15V		20	27	mA	
–15V		10	18	mA	
+5V		10	14	mA	
Power Dissipation		500	750	mW	
TEMPERATURE RANGE					
Operating Temperature Range:					
JH, SH	0		70	°C	
SH, TH	–55		+125	°C	
Storage Temp. Range	–65		+150	°C	

NOTES: (1) Measured at the sample-and-hold output. (2) Measured with all input channels grounded. (3) The range of voltage on any input with respect to common over which accuracy and leakage current is guaranteed. (4) Applicable over full temperature range. NO MISSING CODES GUARANTEED OVER TEMPERATURE RANGE. (5) Adjustable to zero using external potentiometer or select-on-test resistor. (6) Specifications are at +25°C and measured at 50% level of transition. (7) Parameter guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to A COM ..... –0.5V to +16V	Analog Input Signal Range ..... ($+V_{CC}$+20V) to ($-V_{CC}$–20V)
$-V_{CC}$ to A COM ..... +0.5V to –16V	Digital Input Signal ..... –0.5V to $+V_{DD}$
$+V_{DD}$ to D COM ..... –0.5V to +5.5V	A COM to D COM ..... ±1V

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OPERATING INSTRUCTIONS

OPERATING MODES

The DAS can operate in one of two modes, namely serial and overlap, as shown in Figure 1. In serial mode, control of the device is such that the multiplexer channel X is first selected, time is then allowed for the instrumentation amplifier to settle, the sample/hold amplifier is set to HOLD mode and finally a conversion is carried out. This procedure is then repeated for channel Y. Faster throughput can be obtained using overlap mode. While a conversion is being carried out by the ADC on a voltage from channel X held on the sample/hold, channel Y is selected and the multiplexer and instrumentation amplifier allowed to settle. In this way, the total throughput time is limited only by the sum of the sample/hold acquisition time and the ADC conversion time.

CALIBRATION – UNIPOLAR

If adjustment of unipolar is offset and gain are not required, then the gain set potentiometer in Figure 2a (Unipolar operation) may be replaced with a 50Ω, 1% metal film resistor, and the offset network replaced with a connection from pin 23 to ground.

CALIBRATION – BIPOLAR

If adjustment of bipolar offset and gain are not required, then the gain set and offset potentiometers in Figure 2b (Bipolar operation) may both be replaced with 50Ω, 1% metal film resistors.

CALIBRATION – GENERAL

The input voltage ranges of the ADC are 0–10V, ±5V and ±10V. Calibration in all ranges is achieved by adjusting the offset and gain potentiometers (indicated in Figure 2a and b) such that the 000 to 001 code transition takes place at +1/2LSB from full-scale negative (–FS) and the FFE to FFF transition takes place at –3/2LSB from full-scale positive (+FS). The procedure is therefore to select the required range and apply the specified (–FS+1/2LSB) voltage to any selected input channel and adjust the offset potentiometer for the 000 to 001 transition. The (+FS–3/2LSB) voltage should then be applied to the same channel and the gain potentiometer adjusted for the FFE to FFF transition. The offset should always be made before the gain adjustment.

STAND–ALONE OPERATION

The stand–alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and BYTE SELECT are connected to LOW and CE and DATA MODE are connected to HIGH. The output data are presented as 12–bit words.

Conversion is initiated by a High–to–Low transition of R/$\overline{C}$. The three–state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In each case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 5 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes

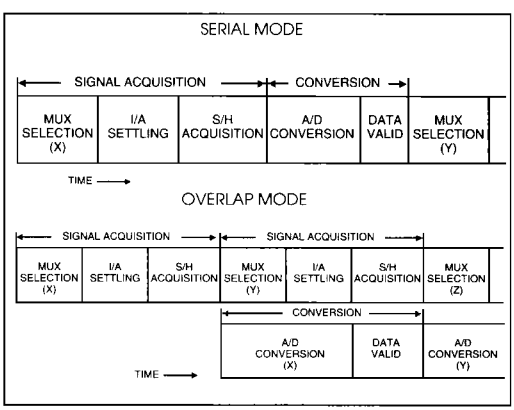

FIGURE 1. Operating Modes

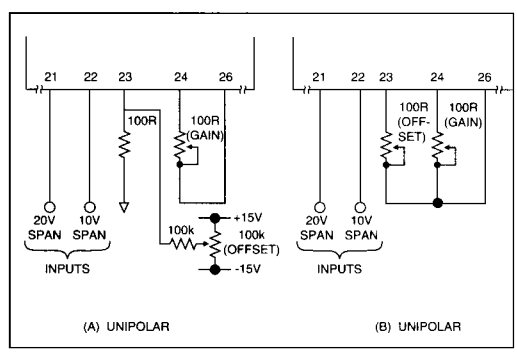

FIGURE 2. Calibration

low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/C and are enabled for external access of the data after completion of the conversion. Figure 6 illustrates the timing when conversion is initiated by a positive R/C pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/C. A new conversion is started on the falling edge of R/C, and the three-state outputs return to the high impedance state until the next occurrence of a high R/C pulse. Table 1 lists timing specifications for stand-alone operation.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the BYTE SELECT input, which is latched upon receipt of a conversion start transition. BYTE SELECT is latched because it is also involved in enabling the output buffers. No other control inputs are latched. If BYTE SELECT is latched high, the conversion continues for 8-bits. The full 12-bit conversion will occur if BYTE SELECT is low. If all 12 bits are read following an 8-bit conversion, the 3LSB's (DB_0-DB_2) will be low (logic 0) and DB_3 will be high (logic 1).

Conversion Start

A conversion is initiated by a transition on any of three logic inputs (CE, CS and R/C) -refer to Figure 8. The last of the three to reach the required state start the conversion and thus all three may be dynamically controlled. If necessary, they may change state simultaneously, and the nominal delay time is independent of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Conversion Cycle Timing of Digital Specifications.

The STATUS output indicates the state of the converter by being high only during a conversion. During this time the three-state buffers remain in a high-impedance state, and therefore, data is not valid. During this period additional transitions of the three control inputs will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if BYTE SELECT chanes state after the beginning of conversion, any additional start conversion transition will latch the new state of BYTE SELECT, possibly resulting in an incorrect conversion length (8-bit versus 12-bits) for that conversion.

READING OUTPUT DATA

After a conversion is initiated, the output data buffers remain in a high-impedance state until the following four conditions are met: R/C high, STATUS low, CE high, and CS low. In this condition the data lines are enabled according to the state of the inputs DATA MODE and

CE	CS	R/C	DATA MODE	BYTE SELECT	OPERATION
0	X	X	X	X	NONE
X	1	X	X	X	NONE
↓	0	0	X	0	INITIATE 12-BIT CONVERSION
↓	0	0	X	1	INITIATE 8-BIT CONVERSION
1	↓	0	X	0	INITIATE 12-BIT CONVERSION
1	↓	0	X	1	INITIATE 8-BIT CONVERSION
1	0	↓	X	0	INITIATE 12-BIT CONVERSION
1	0	↓	X	1	INITIATE 8-BIT CONVERSION
1	0	1	1	X	ENABLE 12-BIT OUTPUT
1	0	1	0	0	ENABLE 8 MSB's ONLY
1	0	1	0	1	ENABLE 4 LSB's PLUS 4 TRAINING ZEROS

FIGURE 3. Control Input Truth Table

SP9462/9472						SP9463/9473				
MUX ADD3	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Selected	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Pair Selected
X	X	X	X	L	NONE	X	X	X	L	NONE
L	L	L	L	H	0	L	L	L	L	0
L	L	L	H	H	1	L	L	H	H	1
L	L	H	L	H	2	L	H	L	H	2
L	L	H	H	H	3	L	H	H	H	3
L	H	L	L	H	4	H	L	L	H	4
L	H	L	H	H	5	H	L	H	H	5
L	H	H	L	H	6	H	H	L	H	6
L	H	H	H	H	7	H	H	H	H	7
H	L	L	L	H	8			–		
H	L	L	H	H	9			–		
H	L	H	L	H	10			–		
H	L	H	H	H	11			–		
H	H	L	L	H	12			–		
H	H	L	H	H	13			–		
H	H	H	L	H	14			–		
H	H	H	H	H	15			–		

FIGURE 4. Channel Select Truth Table

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BYTE SELECT. See Read Cycle Timing for timing relationships and specification. In most applications the DATA MODE input will be hardwired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When DATA MODE is high, all 12 outputs lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus and the state of the BYTE SELECT is ignored.

When DATA MODE is low, the data is presented in the form of two 8-bit bytes, with the selection of each byte by the state of BYTE SELECT during the read cycle.

SYMBOL		PARAMETER[7]	MIN	TYP	MAX	UN
T_{HRL}		Low R/C Pulse Width	50			nS
T_{DS}		STS Delay from R/C			200	nS
T_{HDR}		Data Valid after R/C Low	25			nS
T_{HS}	946X	STS Delay After Data Valid	300	500	1000	nS
T_{HS}	947X		100	300	600	nS
T_{HRM}		High R/C Pulse Width	150			nS
T_{DDR}		Data Access Time			150	nS

The BYTE SELECT input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.
When BYTE SELECT is low, the byte addressed contains the 8 MSBs. When BYTE SELECT is high, the byte addressed contains the 4 LSBs from the conversion

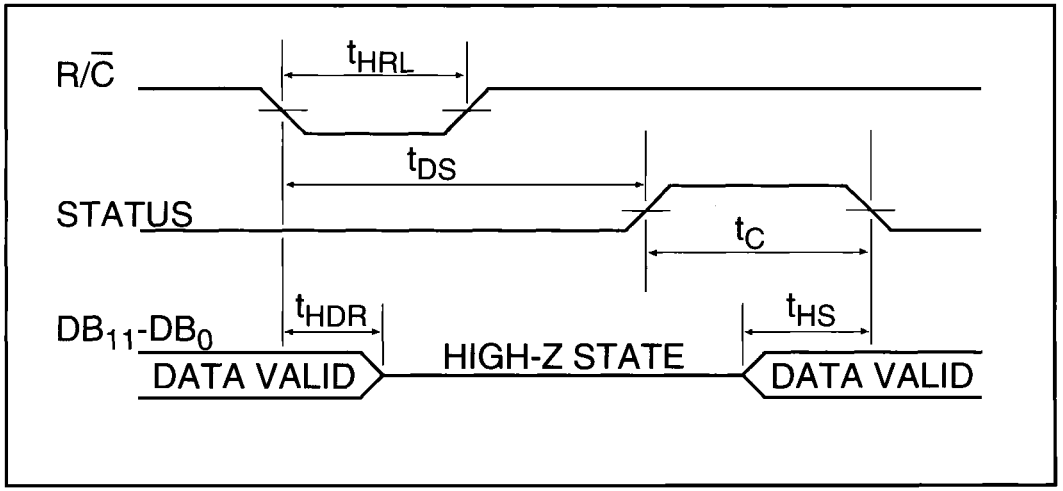


FIGURE 5. Low R/C Pulse Conversion Timing

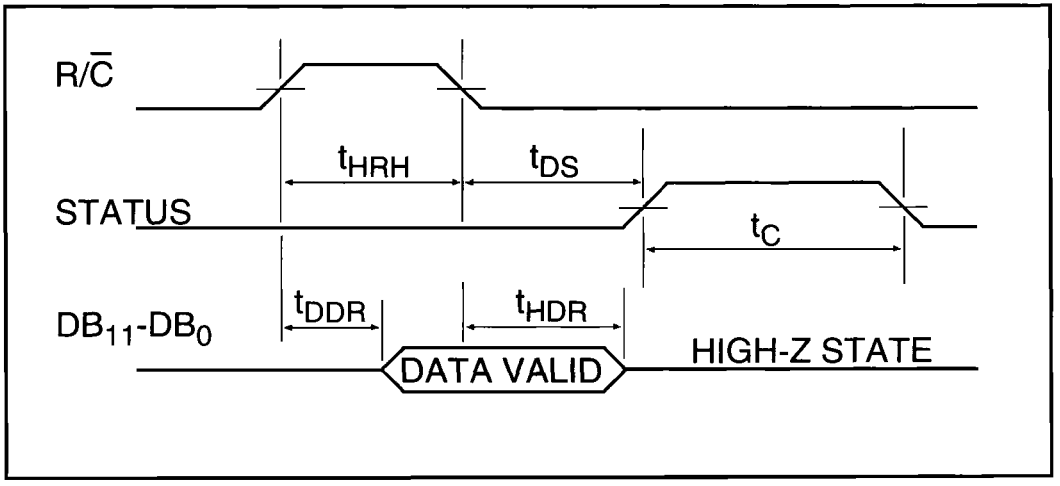


FIGURE 6. High R/C Pulse Conversion Timing

followed by four zeros that have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 7. The design of the DAS guarantees that the BYTE SELECT input may be toggled at any time without damage to the output buffers occuring.

In the majority of applications, the read operation will be attempted only after the conversion is complete and the status output has gone low. In those situations requiring the fastest possible access to the data, the read may be started as much as (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Read Cycle Timing for these timing relationships.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

It should be noted that the multiplexer/instrumentation amplifier section and sample/hold plus ADC section of the DAS have separate power connections. This is to enable more flexible grounding

	WORD 1								WORD 2							
PROCESSOR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DAS	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

DIGITAL TIMING					
SYMBOL	PARAMETER[7]	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	Status delay from CE		100	200	nS
t_{HEC}	CE Pulse width	50	30		nS
t_{SSC}	$\overline{CS}$ to CE setup	50	20		nS
t_{HSC}	$\overline{CS}$ low during CE high	50	20		nS
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		nS
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		nS
t_{SAC}	Byte select to CE setup	0	0		nS
t_{HAC}	Byte selected valid during CE high	50	20		nS
t_C 946X	Conversion time:				
	12-bit cycle	15	20	25	µS
	8-bit cycle	10	13	17	µS
t_C 947X	Conversion time:				
	12-bit cycle	9	12	15	µS
	8-bit cycle	6	8	10	µS
READ MODE					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data valid after CE low	25	35		nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50	0		nS
t_{SRR}	R/$\overline{C}$ to CE setup	0	0		nS
t_{SAR}	Byte select to Ce setup	50	25		nS
t_{HSR}	$\overline{CS}$ valid after CE low	0	0		nS
t_{HRR}	R/$\overline{C}$ high after CE low	0	0		nS
t_{HAR}	Byte select valid after CE low	50	25		nS
t_{HS} 946X	Status delay after data valid	300	500	1000	nS
t_{HS} 947X	Status delay after data valid	100	300	600	nS

techniques to be implemented as shown in Figure 8. It also facillitates the use of independent decoupling of the analog front-end power supply, and the ADC plus associated digital circuitry power supply if desired. In this way, a separately decoupled analog front-end can be made to be substantially more immune to power supply noise generated by the ADC circuitry than if the power supplies to the two sections were directly connected. This feature is important where low-level signals are in use or high input signal noise immunity is desired.

The output section has three grounds:
Pin 25 Analog Common, A/D Converter
Pin 34 A/H Amp digital input reference
Pin 19 Digital Common, A/D Converter

The input section has one ground:
Pin 53 Common for digital MUX inputs and power suypply decoupling.

All grounds have to be interconnected externally to the DAS, and it is recommended that all grounds are connected via one track to a single point as close as possible to the DAS. To check that the grounding structure is correct, the ground tracking should be sketched and a grounding "tree" should result whereby all grounds route to a central point.

In general, layout should be such that analog and digital tracks are sparated as much as possible with coupling between analog and digital lines minimized by careful layout. For instance, if the lines must cross they should do so at right angles to each other. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

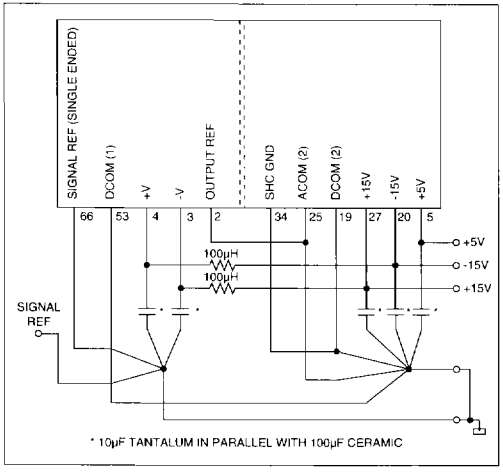


FIGURE 8. Recommended Decoupling of Power Supplies

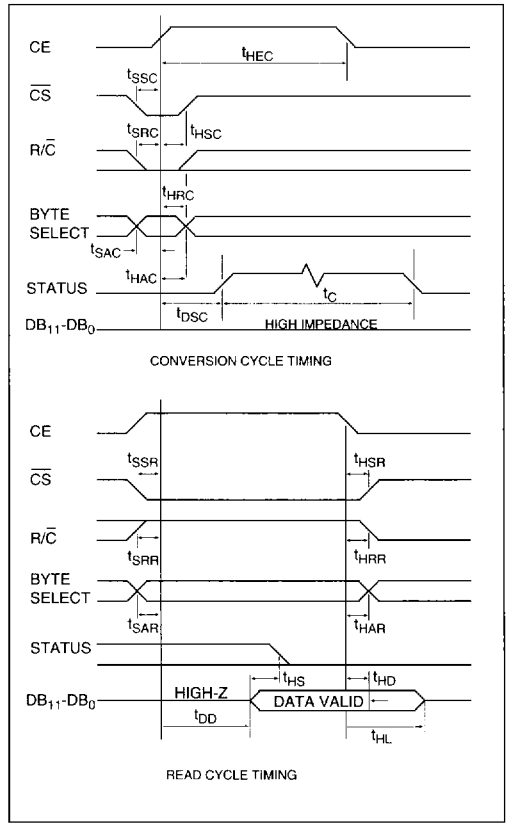
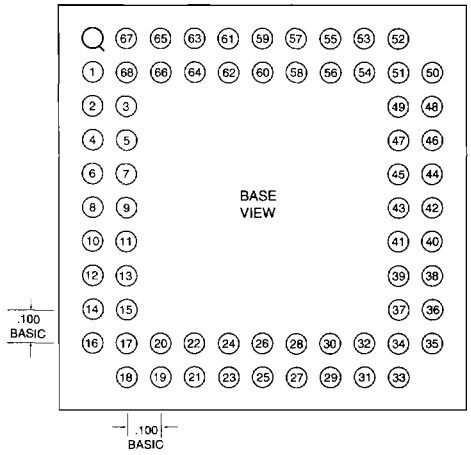


FIGURE 9. Conversion and Read Cycle Timing

PIN DESIGNATION	PIN NOS	DEFINITION	COMMENTS
CH_0 to CH_{15} CH_0 to CH_7(+,–)	40 - 47 54 – 61	Channel Inputs	Analog inputs (total 16) for single–ended and differential operation. Unused inputs must be connected to analog common.
MUX OUT + / AMP IN +	65	Multiplexer "HI" Output	On the 94X2, this is the multiplexer output. On the 94X3, it is the output of the positive selected inputs. It is connected internally to the positive input of the instrumentation amplifier.
MUX OUT	67	Multiplexer "LO" Output	This pin is used on the 94X3 only. It should be connected to the negative input of the instrumentation amplifier.
AMP IN	66	Negative Input of the Instrumentation Amplifier	On the 94X2, this should be connected to analog common. On the 94X3, it should be connected to MUX OUT – (Pin 67).
AMP OUT	1	Output of the Instrumentation Amplifier	This pin should be connected to the input of the S/H amplifier (Pin 39).
AMP SENSE	68	Output sense line of the Instrumentation Amplifier	This pin will normally be connected directly to AMP OUT (Pin 1).
AMP REF	2	Reference for Amplifier Output	This pin will normally be connected to analog common. Care should be taken to minimize tracking and contact resistance to analog common to optimize system accuracy.
S/H OUT	35, 37	Output of Sample/Hold Amplifier	Two Pins are provided to facilitate a guard ring around the hold capacitor pin. These pins should be connected to either ADC IN (20V) or ADC IN (10V) depending on the desired range.
HOLD CAP	36	Connection for the Hold Capacitor on the S/H Amplifier	The tracking to the hold capacitor should be as short as possible and a guard ring employed using (Pins 35 and 37).
ADC IN (20V); ADC IN (10V)	21,22	Output of the Instrumentation Amplifier	This pin should be connected to the input of the S/H amplifier (Pin 39).
RG, G10, G100	62,63,64	Gain Setting Pins on the Instrumentation Amplifier	Gain=1, no connections. Gain=10, connect G10 to RG. Gain=100, connect G100 to RG.
REF OUT	26	10V Reference Voltage	This is the reference voltage for the A/D converter.
REF IN, BIP OFF	24, 23	Reference Input and Offset input to the A/D Converter	Connect trim potentiometers (or select–on–test resistors) to these pins for unipolar or Bipolar operation as shown in Figures 2A and 2B.
S/H IN	39	Input to the Sample/Hold Amplifier	Connect to AMP OUT (Pin 1).
MUX ENABLE	48	Multiplex Enable/Disable	Logic '1' on this pin will enable a selected channel on the internal multiplexer. Logic '0' de–selects all channels.
MUX ADD_0 TO MUX ADD_3	49 – 52	Address Inputs for Channel Selection	These address lines select a particular channel as specified in Figure 4.
S/H CONT	33	Track/Hold Control on the Sample/Hold Amplifier	Logic '1' holds an analog value for conversion by the A/D converter. This line may be controlled by the status (Pin 6) of the converter to simplify external timing control.
S/H COM	34	Reference for Sample/Hold Logic Control	Connect to digital common.
D_0 to D_{11}	7 – 18	3–State Digital Outputs	The 12– or 8–bit result of a conversion is available as output on these pins (D_0–LSB, D_{11}–MSB).

PIN DESIGNATION	PIN NOS	DEFINITION	COMMENTS
STATUS	6	Status of the A/D Conversion	This output is at logic '1' while the internal A/D converter is carrying out a conversion. This may be used to directly control the S/H amplifier.
CE	28	Chip Enable	This input must be at logic '1' to either initiate a conversion or read oputput data.
CS	31	Chip Select	This input must be at logic '0' to either initiate a conversion or read output data.
R/C	29	Read/Convert	Data can be read when this pin is logic '1' or a conversion can be initiated when this pin is logic '0'. This pin is typically connected to the R/W control line of a microprocessor-based system.
DATA MODE	30	Select 12 or 8 Bit Data	When data mode is at logic '1' all 12 output data bits are enabled simultaneously. When data mode is at logic '0' MSBs and LSBs are controlled by byte select (Pin 32).
BYTE SELECT	32	Byte Address, Short Cycle	When reading output data, byte select at logic '0' enables the 8 MSBs. Byte select at logic '1' enables the 4 LSBs. The 4 LSBs can therefore be connected to four of the MSB lines for interconnection to an 8-bit bus. In start convert mode, logic '0' enables a 12 bit conversion while logic '1' will short cycle the conversion to 8 bits.
+15V(1), +15V(2)	3, 27	Power Supply	Connect to +15V supply using decoupling as indicated in Figure 1.
-15V(1), -15V(2)	4, 20	Power Supply	Connect to -15V supply using decoupling as indicated in Figure 1.
A COM(2)	25	Analog Common	Analog common connection. Note that a common (including digital common) should be connected together at one point closesss to the device.
D COM(1)	53	Reference for MUX Logic Control	Connect to digital Common.
+5V	5	Logic Power Supply Amplifier	Connect to +5V digital supply line with decoupling as in Figure 1.
D COM(2)	19	Reference for A/D Converter Control Lines	Connect to S/H common at one point close to the device.
NC	38	No Internal Connection	

PIN ASSIGNMENTS

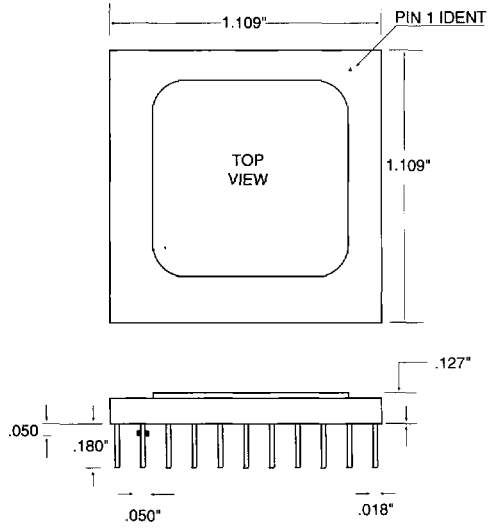


PIN	FUNCTION
1	Amp Out
2	Amp Ref
3	+15V(1)
4	−15V(1)
5	+5V
6	Status
7	D11
8	D10
9	D9
10	D8
11	D7
12	D6
13	D5
14	D4
15	D3
16	D2
17	D1
18	D0
19	ADC DCOM
20	−15V (2)
21	ADC in (20V)
22	ADC in (10V)
23	Bipolar Offset
24	Ref In
25	ACOM (2)
26	Ref Out
27	+15V (2)
28	CE
29	R/C
30	Data Mode
31	CS
32	Byte Select
33	S/H Control
34	S/H Common

PIN	FUNCTION
35	S/H Out
36	Hold Cap
37	S/H Out
38	NC
39	S/H In
40	CH7 (CH7+)*
41	CH6 (CH6+)*
42	CH5 (CH5+)*
43	CH4 (CH4+)*
44	CH3 (CH3+)*
45	CH2 (CH2+)*
46	CH1 (CH1+)*
47	CH0 (CH0+)*
48	MUX Enable
49	MUX Address 0
50	MUX Address 1
51	MUX Address 2
52	MUX Address 3 (NC)*
53	ACOM (1)
54	CH8 (CH0–)*
55	CH9 (CH1–)*
56	CH10 (CH2–)*
57	CH11 (CH3–)*
58	CH12 (CH4–)*
59	CH13 (CH5–)*
60	CH14 (CH6–)*
61	CH15 (CH7–)*
62	RG (Gain Range)
63	G10
64	G100
65	MUX Out+/Amp In+
66	Amp In–
67	NC (MUX Out–)*
68	Amp Sense

* Applicable to the SP9463/9473

PACKAGE OUTLINE



TOLERANCES ARE ±0.010"

ORDERING INFORMATION

Model	Input	Accuracy (% FSR)	Throughput	Temp. Range (°C)	Model	Input	Accuracy (% FSR)	Throughput	Temp. Range (°C)
SP9462JH	16SE	±0.024	33KHz	0 to +70	SP9463JH	8DIF	±0.024	33KHz	0 to +70
SP9462KH	16SE	±0.012	33KHz	0 to +70	SP9463KH	8DIF	±0.012	33KHz	0 to +70
SP9462SH	16SE	±0.024	33KHz	−55 to +125	SP9463SH	8DIF	±0.024	33KHz	−55 to +125
SP9462TH	16SE	±0.012	33KHz	−55 to +125	SP9463TH	8DIF	±0.012	33KHz	−55 to +125
SP9472JH	16SE	±0.024	50KHz	0 to +70	SP9473JH	8DIF	±0.024	50KHz	0 to +70
SP9472KH	16SE	±0.012	50KHz	0 to +70	SP9473KH	8DIF	±0.012	50KHz	0 to +70
SP9472SH	16SE	±0.024	50KHz	−55 to +125	SP9473SH	8DIF	±0.024	50KHz	−55 to +125
SP9472TH	16SE	±0.012	50KHz	−55 to +125	SP9473TH	8DIF	±0.012	50KHz	−55 to +125

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